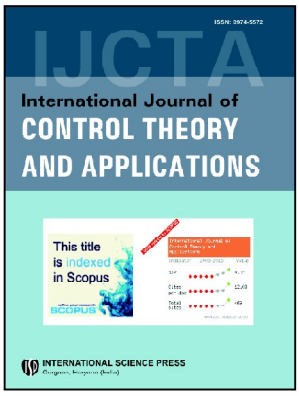

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An Area Efficient Crossbar Switch Scheduler for System-On Chip (SOC) Using Quantum Dot Cellular Automata (QCA) Technology

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Abstract: Objective: This paper presents the design of an on-chip crossbar scheduler for implementation in Quantum Dot Cellular Automata (QCA) technology. ***Methods/ Analysis:*** Crossbar switches are replacing traditional buses as the communication architecture in System-On-Chip (SoC) networks. It performs contention free operation and has higher bandwidth. The major challenge while implementing large SoC network is to keep the area of the crossbar schedulers at minimum level. QCA is an emerging nano scale technology and presently considered as an alternative to current CMOS devices. ***Findings:*** The proposed crossbar scheduler has been designed and simulated using QCA Designer tool. Further, we also synthesized the proposed on-chip scheduler in CMOS technology in order to perform the comparison of area and power consumption. ***Novelty/ Improvements:*** The comparison results show that the QCA technology occupies smaller area and less power consumption than the conventional CMOS devices.

Keywords: System-On-Chip; Contention; Crossbar; QCA

1. INTRODUCTION

Crossbar switches are considered as the key building blocks in System-On-Chip (SoC) network for on-chip interconnections. These switches are highly popular for communication between the components because of its simplicity and non-blocking feature. The core function of the switch is to perform the arbitration of incoming data such that it reaches the appropriate destination output. The major challenge while implementing large SoCs is the area occupied by the entire switch fabric including the crossbar core and the scheduler although efforts have been made for the optimization of area of on-chip schedulers through various scheduling algorithms and architectures [1-5]. Techniques such as On-chip serialization[6] has also been implemented for area reduction but has not shown much effect on the scheduler area and also increases the power consumption.

The main objective of our work is to reduce the area and power consumption of on-chip schedulers. In this paper we have proposed the design of a crossbar scheduler for implementation in Quantum Dot Cellular Automata (QCA) technology. QCA is an emerging nano technology with attractive features such as extremely low power

consumption, high speed operation and ultra-dense structure. This makes it suitable for next generation high performance switching circuits.

The proposed scheduler has been designed & simulated using the QCA Designer tool. Further, the simulation results acquired from the QCA Designer tool has been compared with CMOS technology. It has been observed that QCA technology occupies smaller area and less power consumption.

The rest of the paper is organized as follows: Section II explains the basic QCA mechanism. Section III and IV describes the proposed work and QCA implementation of the crossbar scheduler respectively. Section V discusses the results of the comparison between the two technologies.

Quantum Dot Cellular Automata (QCA) technology has been considered as one of the most promising approach to overcome the limitations of CMOS technology [7]. A QCA device has the potential to perform the logical computation at the nano-scale level.

In recent years QCA has gained significant attention towards the design and implementation of high performance digital circuits such as arithmetic circuits [7,13], sequential circuits [9-12] and memory devices [14, 15]. Less work has been done towards the application of QCA in switching circuits for communication. In this paper we have focussed on the design and implementation of a crossbar scheduler using QCA technology. Our aim is to minimize the area and power consumption of the scheduler which makes it suitable for on-chip communication.

1.1. Basic QCA Device

In QCA devices the computation is performed by the coulombic interaction between neighbouring cells in order to influence the polarization of each other. A QCA cell consists of four quantum dots positioned at the corners of a square and two mobile electrons [8]. Owing to mutual repulsion these electrons will always occupies the corners of the square diagonally opposite to each other [16]. This leads to two different polarization states, P=+1 and P=-1 as shown in Figure 1.

The interconnection within the cells are accomplished by the reorganization of the position of electrons and thus no physical wires are needed between the cells [9]. A three-input majority gate is used to perform logic computation in QCA devices as shown in Figure 2.

2. METHODS AND ANALYSIS

This paper presents the design of a crossbar switch scheduler for QCA implementation. At first, the crossbar scheduler has been implemented by Verilog HDL (Hardware Description Language) in the Xilinx environment. The scheduler works in Round Robin (RR) fashion and has a rotating priority. The RR scheduler guarantees fairness among various input ports.

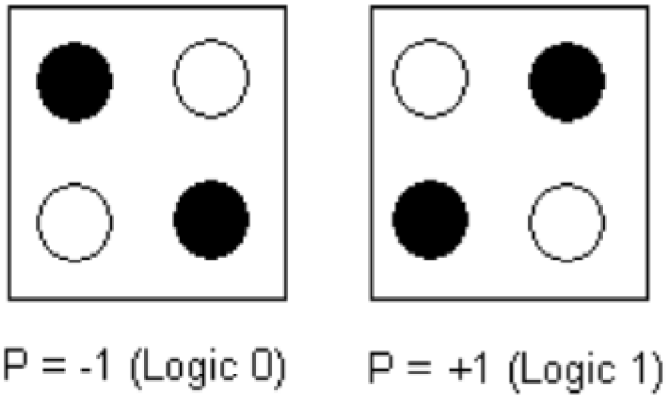

Figure 1: A Basic QCA Cell [8]

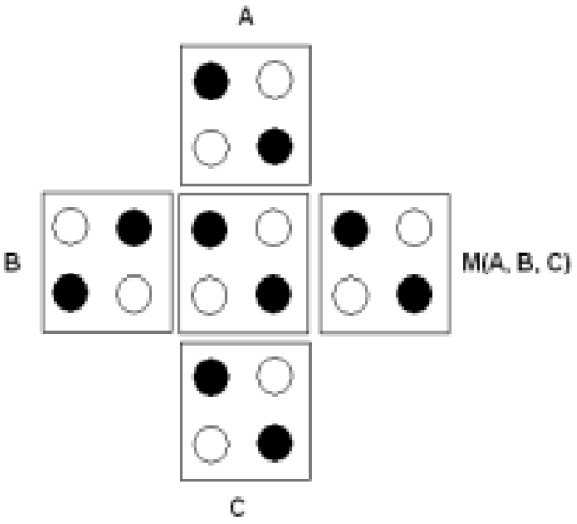

Figure 2 (a): QCA cell arrangement [8]

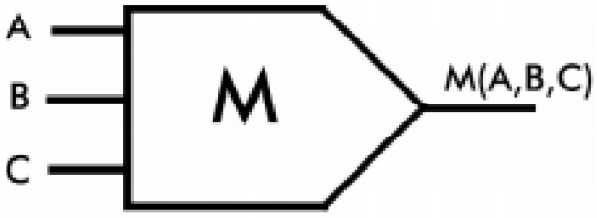

Figure 2(b): Majority gate symbol [8]

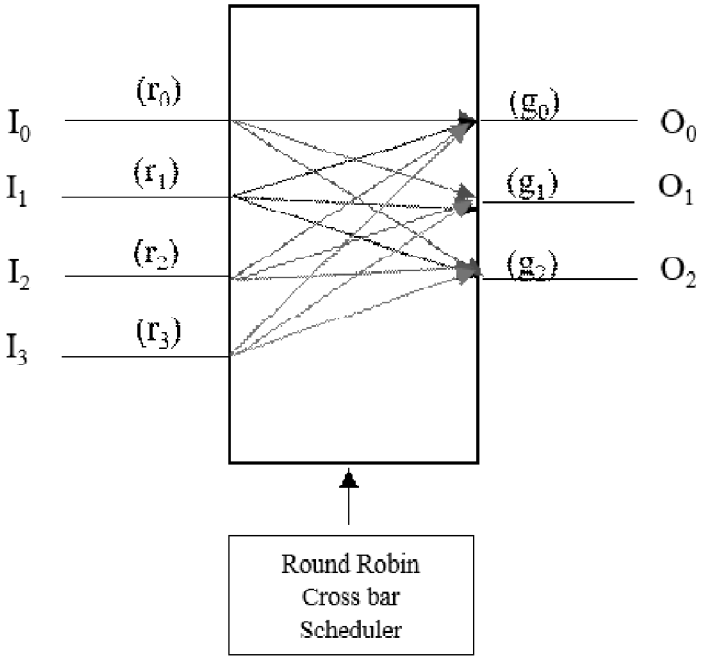

Figure 3: N X M Crossbar Switch (N=4 & M=3)

2.1. Design of Crossbar Switch

Consider a crossbar switching architecture with N input ports and M output ports (NXM) as shown in Figure 1. The request signals arriving at each input port (I_0, I_1, I_2,I_3) can be destined to any of the output ports O_0, O_1& O_2. When the output port receives request signals from input, it selects the one that has highest priority. The process allows to establish a connection in order to perform the desired communication. The scheduler also maintains/ensures fairness among various input ports by selecting the one with the least priority as the highest priority in the next cycle.

Figure 4 & 5 shows the RTL schematic and circuit diagram for the proposed Round Robin (RR) scheduler respectively.

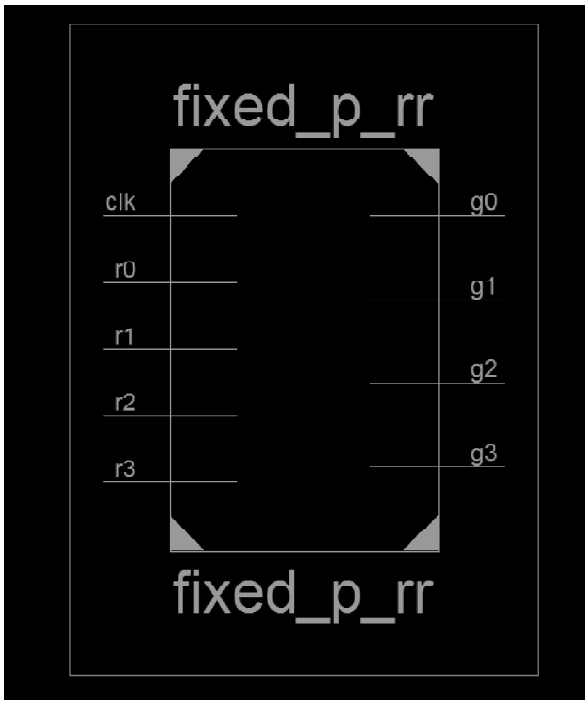

Figure 4: RTL Schematic of RR Scheduler

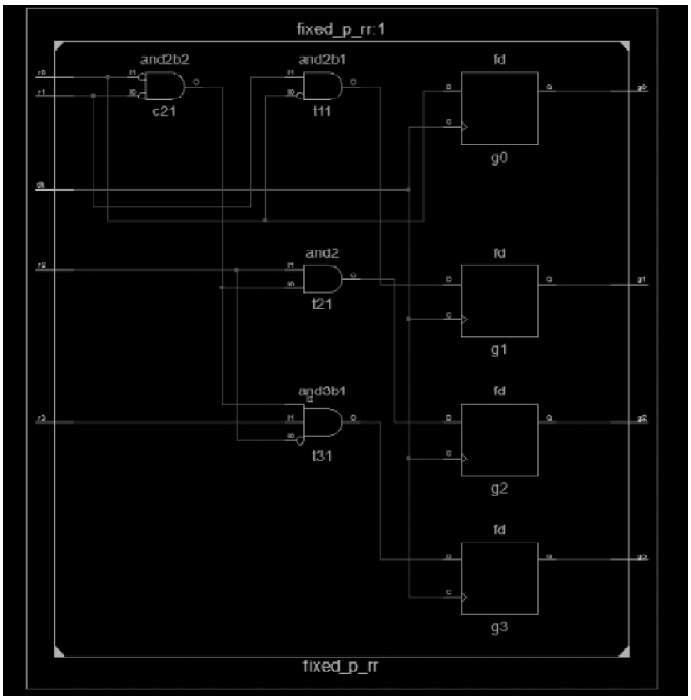

Figure 5: Circuit Diagram of RR Scheduler

Figure 6 represents the simulation waveform for the Round Robin (RR) scheduler. The results obtained from the simulation justifies the functionality of the circuit as represented in the truth table (Table 1 - Truth Table for RR Scheduler). It says that during the first clock edge both r0 and r1 are active. As I0is having highest priority, so only the request signal r_0 will be acknowledged by g_0 signal. During the second clock edge a request from r_1 is acknowledged by g_1 signal.

Table 1
Truth Table for RR Scheduler

	Input				*Output*		
Clk	r_0	r_1	r_2	r_3	g_0	g_1	g_2
↑	1	1	0	0	1	0	0
↑	0	1	0	0	0	1	0

Table 2
Comparison Table

Parameters	*Proposed Round Robin Scheduler*	
	QCA Technology	*CMOS Technology*
Area (μm^2)	0.017	67.0
Power (Watts)	$0.77X10^{-15}$	$984.7X10^{-9}$

2.2. QCA Implementation of Crossbar Switch

Quantum Dot Cellular Automata (QCA) is a technology where computation is performed at nano-scale level and has extremely low power consumption. Our aim is to minimize the area of the scheduler in order to make it

efficient for on-chip communication. The proposed crossbar scheduler has been implemented using the QCA Designer software tool version 2.2.Figure 7 shows the QCA implementation of the Round Robin scheduler. The scheduler presented in QCA has cells and occupies an area of 0.017 μm^2.

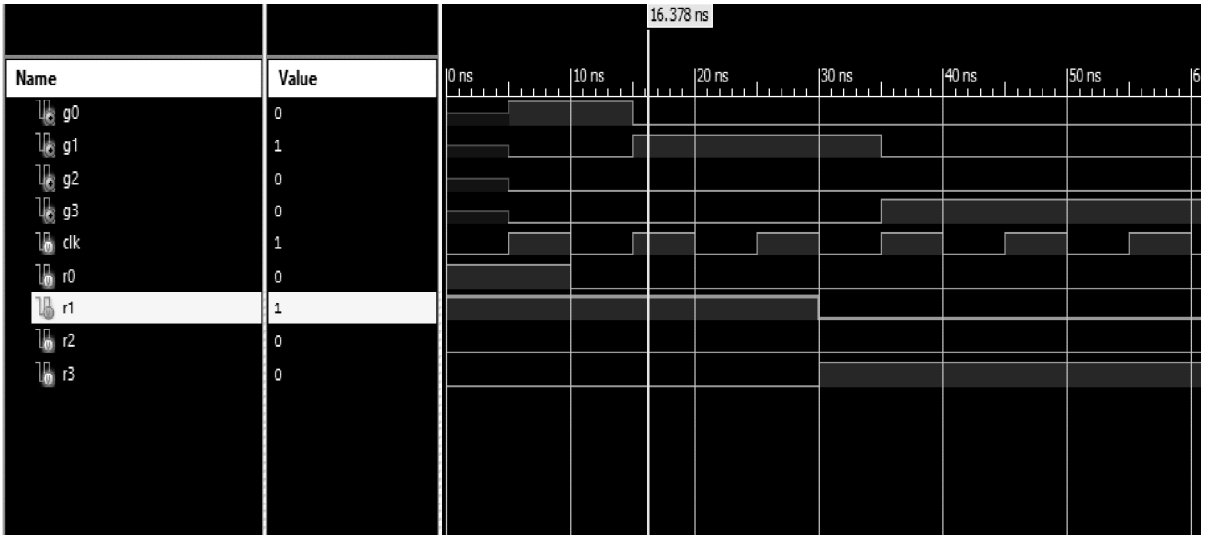

Figure 6: Simulation Waveform of the RR Scheduler

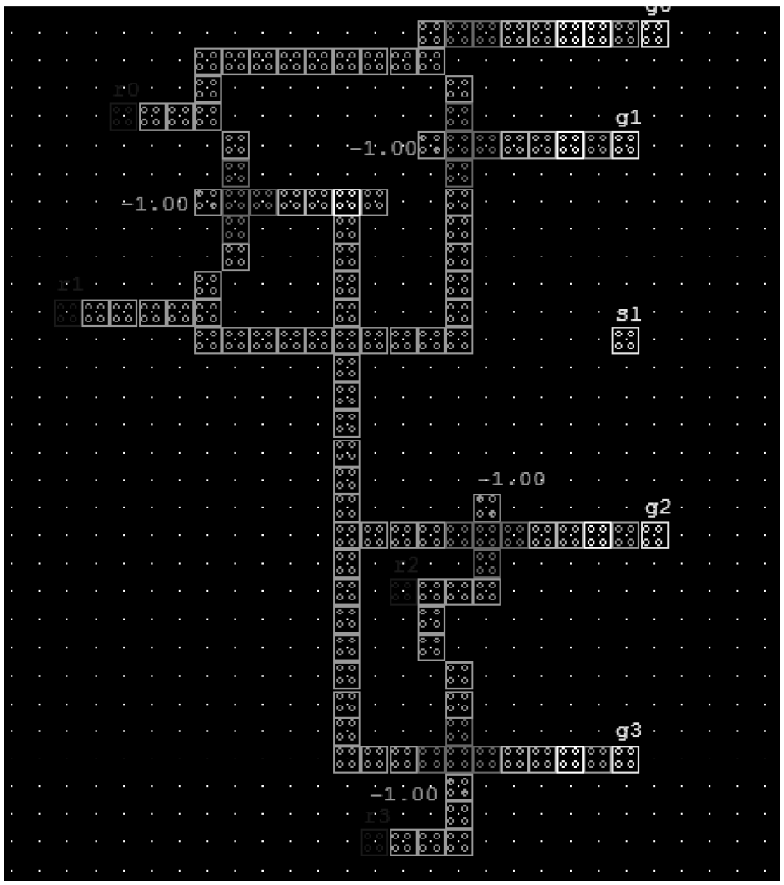

Figure 7: QCA implementation of RR Scheduler

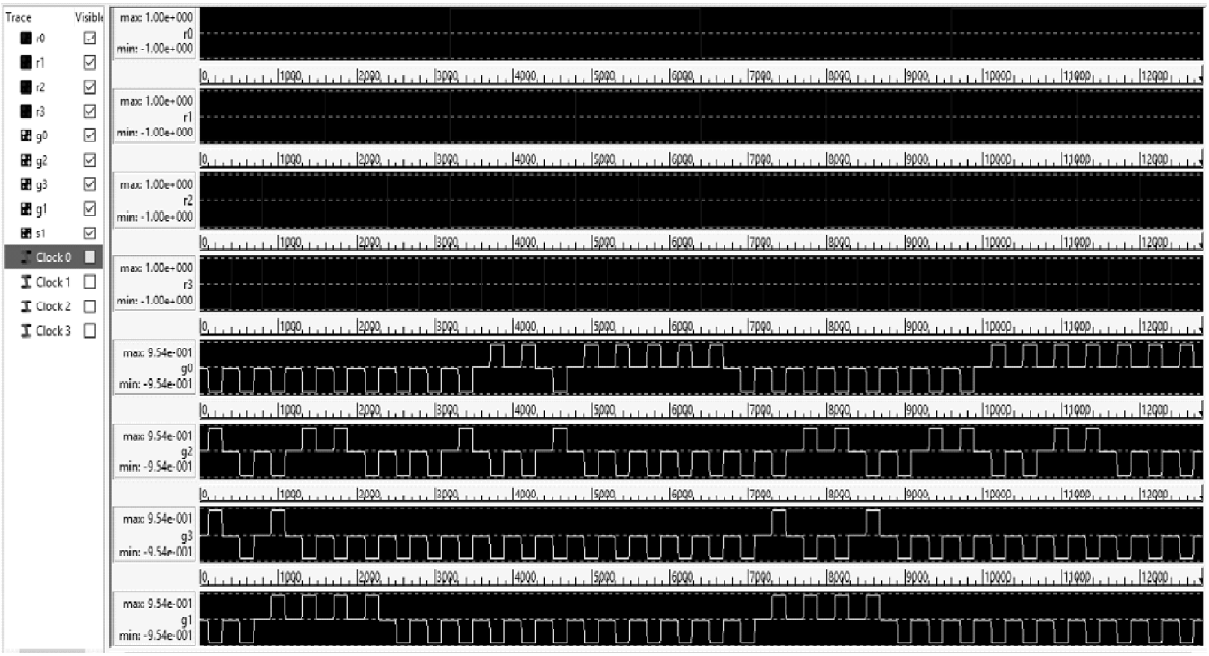

Figure 8: Simulation Waveform of QCA implementation

2.2.1. Power Calculation

With the size of CMOS transistor continue shrinking, it will eventually hit its physical limitation[8]. The consequences such as power dissipation and leakage current are becoming bottleneck for the further scaling of CMOS devices. Hence, QCA technology has been introduced as an alternative approach for next generation devices.

To perform the power and energy calculations we have considered four cases and the energy dissipation equation says that:

$$Ediss \leq \left[\frac{2\gamma new}{Ek} \left(\frac{P0}{Pold} \gamma old - \frac{Pn}{Pnew} \gamma new \right) + \frac{EkPnew}{2} (P0 - Pn) \right] \quad (1)$$

Where, Ek=255.351x10^{-29} J

CASE 1

Pn=Po=1, Pold=-1, Pnew=1

By substituting these values in equation 1, we get

Ediss=0.78x10^{-15} J

CASE 2

Pn=Po=-1, Pold=-1, Pnew=1

By substituting these values in equation 1, we get

Ediss = $0.78x10^{-15}$ J

CASE: 3

Pn=Po=-1, Pold=1, Pnew=-1

By substituting these values in equation 1, we get

Ediss=$0.78x10^{-15}$ J

CASE: 4

Pn=Po=1, Pold=1, Pnew=1

By substituting these values in equation 1, we get

Ediss = $0.725x10^{-15}$ J

Power Dissipation: Pdissd" ($0.77x10^{-15}$) watts

3. RESULT AND DISCUSSION

The simulation results obtained from QCA implementation has been compared with CMOS technology using Cadence RTL Compiler.

It can be observed from the above comparison table (Table 2) that the QCA implementation of the proposed scheduler occupies smaller area and less power consumption as compared to the CMOS technology.

4. CONCLUSION

Weproposed the crossbar switch scheduler for communication in SoC network. The proposed scheduler has been implemented in QCA technology. We also synthesized the proposed crossbar scheduler in CMOS technology.The results of QCA implementation has been compared with CMOS technology. It can be concluded that the QCA technology occupies less area and power consumption than the conventional CMOS devices. This makes QCA devices suitable for on-chip communication.

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