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# Power optimization in test pattern generator techniques for BIST applications

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**ABSTRACT**

Built in self test (BIST), as the name reveals, is an on board testing technique employed for testing of Very Large Scale Integration (VLSI) circuits using the circuit components itself. BIST has emerged as good solution to the VLSI test environment eliminating the use of expensive external automatic test equipment (ATE) for testing the circuit. In BIST, a pseudo random test pattern generator is used to feed the test vectors required to test the circuit under test for various faults. This paper discusses various techniques for designing test pattern generator and various optimization techniques for the reduction of switching activity within the consecutive test vectors which in turn reduces the power consumption in test mode. Different optimized designs for TPG are compared and power reduction of 15.625% is achieved.

***Keywords:*** Built-in-self test (BIST), Device under Test (DUT), automatic test equipment (ATE), Very Large Scale Integration (VLSI), power.

## 1. INTRODUCTION

In Built in self testing (BIST), test vector generator is usually a LFSR to provide random test patterns for primary inputs and the actual response received from device under test (DUT) are compared with signature stored ina signature register (SR)[7]. Random test vectors generated by test pattern generator has transitions between consecutive patterns and these patterns applied to a device under test (DUT) results in more power dissipation because of the switching activity than in normal operation. The reason is the switching activity between different test patterns generated by LFSR[7]. More is the randomness between the consecutive patterns generated, more is the switching activity, and more is the power dissipated. Increase in this average and peak power dissipation results in the increased heat up and reliability issues. There are two types of

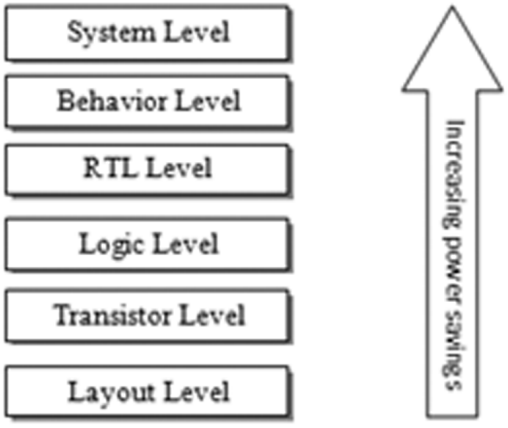


**Figure 1: Power optimization at different levels of design.**

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power dissipation in VLSI circuits, one is because of the leakage current in transistors during steady state and is named as static power, and another is because of the switching activity and is named as dynamic power[4]. So to reduce the power consumed the switching activity must be controlled amongst the different architectures.

There are different levels of optimization for reducing power in VLSI designs:

In this paper, Section II briefs about different components of built in self test (BIST), Section III explains about various test pattern generator architectures, Section IV lists power optimization techniques available for TPG, in Section V results are been obtained and compared for various topologies of TPGs with different optimizations and then in Section VI conclusion is obtained.

## 2. BUILT-IN-SELF TEST

BIST is an on-board testing technique employed in testing the VLSI circuits that in eliminates the requirement of automatic test equipment to be used for testing[4]. But BIST introduces certain overhead on the device under test as it uses a shift register for generating the pseudo random test patterns which introduces more switching activities in the device under test (DUT) during the test mode than in the normal operation[8]. That in turns consumes more power in testing thereby resulting in introduction of undesirable delay into the system. So, selecting the proper configuration for automatic test pattern generator (ATPG) among various possible architectures is of at most importance. There are several parameters that must be considered while formulating architecture for BIST for the desired device under test (DUT)[6] [7].Many techniques have been presented in literature based on optimizing BIST functionality by controlling its parameters. In this paper, four TPG architectures with three different optimization techniques have been simulated and analyzed for power dissipation.

BIST architecture consists of the following main components:

a) Test Pattern Generator (TPG): Test pattern generator portion forms the main part of Built in self test as it provides pseudo random test vectors to be supplied to device under test for detecting different faults [8].

b) Device under test (DUT): Device under test is the circuit to be tested for faults and it can be a sequential or a combinational circuit. It generates the actual response taking in the test patterns from TPG and is further compared with the expected outcome [7] [8].

c) BIST Controller: As the name reveals, this is the control unit of built in self test. It manages the data flow between TPG, ORA and reconfigures the DUT[7]. It is enabled by a mode selection bit (Normal mode/Testing mode) and gives out an error / no error signal.

d) Output response analyzer (ORA): In this portion of BIST, the comparison is being done between the actual and expected output[7] [8]. It comprises of signature register (that stores the expected responses) and comparator (To compare the sequence on primary outputs (PO) with the expected outcomes).

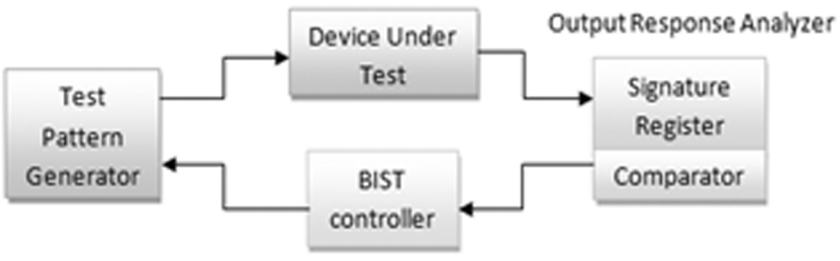


**Figure 2: BIST Architecture**

Different architectures can be implemented for built in self testing (BIST) using the above listed components[4]. As they will comprise of different TPGs and ORAs so, different architectures consume different power even for same polynomial.

## 3. TEST PATTERN GENERATOR ARCHITECTURES

Design of Test Pattern Generator (TPG) is very important step in BIST as the random test vectors generated decides the test length and switching activity (WSA) [1] [7]. Alinear feedback shift register is used as an automatic test pattern generator(ATPG)to generate the pseudo random patterns. But other techniques like gray counter, cellular automata and genetic algorithm can also be used as a test pattern generator [8]. Different test pattern generators are:

i) Linear feedback shift register (LFSR):
   - Internal LFSR
   - External LFSR

ii) Linear Hybrid Cellular Automata (LHCA):
   - CA Rule 90
   - CA Rule 150

### 3.1. Internal LFSR

In an internal feedback shift register, the feedback from the last flip flop's output goes to the first flip flop's input and all the taps are XORed with the feedback path to feed the next successive inputs to flip flops in the shift register [4] [9].

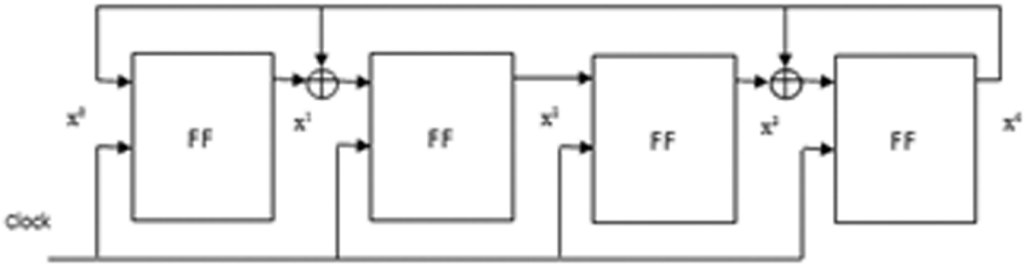


**Figure 3: Internal LFSR**

### 3.2. External LFSR

In an external feedback LFSR, the feedback from the last flip flop's output goes to the first flip flop's input and the taps are used only in the feedback path and XOR of all such taps is given to the input of successive flip flops in shift register [4] [9].

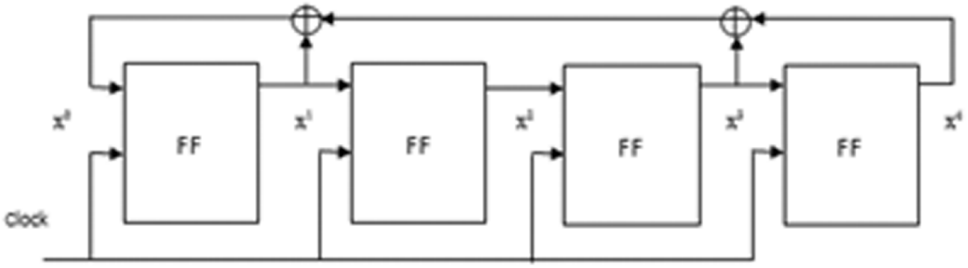


**Figure 4: External LFSR**

### 3.3. Linear Hybrid Cellular Automata (LHCA)

A cellular automata (CA) register is a bio inspired technique in which there is a logical relation of each node with its neighbors. The different rules denote the relations and they define the characteristic behavior of that every CA rule. Linear hybrid cellular automata consist of group of logically connected nodes formed by flip-flops and the logical relation is the result of XOR taps within the structure [9]. Here in this paper CA rule 90 and CA rule 150 are implemented which fall under one dimensional linear CA as the value of a node is determined only by preceding and succeeding neighboring cells.

### 3.4. CA Rule 90

The next state $x(t + 1)$ of node $x_i$ is determined by the current state $x(t)$ of the neighboring nodes $x_{i-1}$ and $x_{i+1}$ for rule 90 [8] [9].

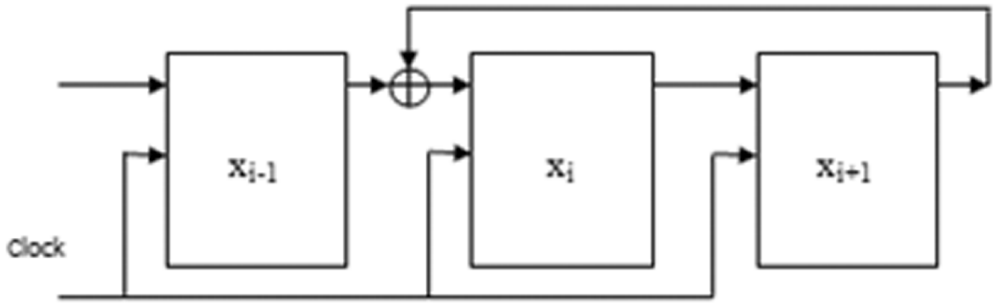


**Figure 5: CA rule 90**

### 3.5. CA Rule 150

The next state $x(t + 1)$ of node $x_i$ is determined by the current state $x(t)$ of the neighboring nodes $x_i$, $x_{i-1}$ and $x_{i+1}$ for rule 150 [8].

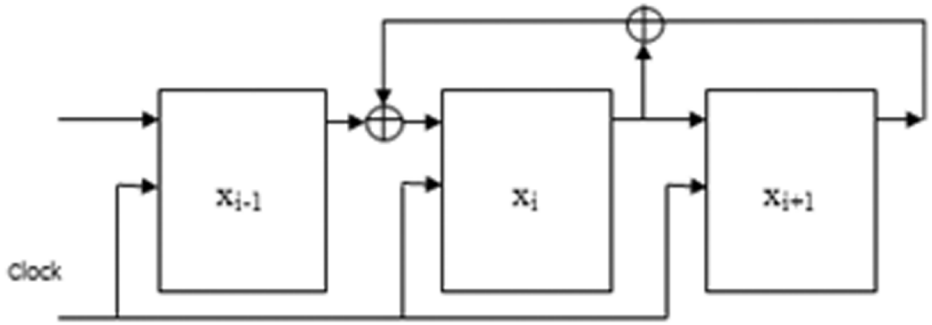


**Figure 6: CA rule 150**

## 4. POWER OPTIMIZATION TECHNIQUES

Different optimization techniques can be used to reduce the transitions in test vectors generated by automatic test pattern generator (ATPG) [3]. As these transitions are the main sources of switching activity in the circuit. So, reduction of these transitions will control the switching activity (WSA) which can further reduce the power consumed while testing a VLSI circuit.

Optimization rules that can be implied on TPG are:

- Bit Invert
- Bit Swap
- Biprate Matching

## 5. RESULTS

BIST architectures are implemented using Xilinx 14.1. Switching activity and dynamic power is been calculated using Xpower Analyzer for first ten vectors generated by different TPGs. Table IV defines the comparison of different LFSRs and LHCAs in all the above stated configurations. The results are compared only for first 10 patterns generated by each TPG and 8-bit Booth multiplier is taken as CUT.

**Table 1**
**Comparison of Different LFSR and LHCA Registers**

| *Optimization* / *TPG* | *Normal Operation* | *Biprate Matching* | *Bit invert* | *Bit Swap* |
|---|---|---|---|---|
| LFSR Internal | 95* | 94 | 87 | 87 |
| LFSR External | 96 | 90 | 85 | 86 |
| LHCA Rule 90 | 86 | 86 | 85 | 85 |
| LHCA Rule 150 | 88 | 89 | 81 | 83 |

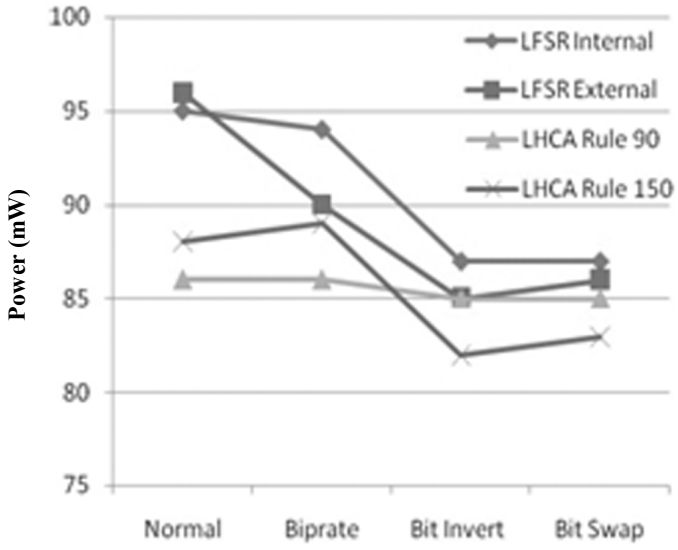


**Figure 7: Comparison of different TPGs**

## 6. CONCLUSION

Different LFSR and LHCA configurations are implemented and three optimizations are tested onto them for power consumption. Further they are compared with the normal design as well as the optimized design. The lowest power consumption is obtained in case of LHCA Rule 150 but the patterns generated by the CA 150 register are lesser so for sufficient fault coverage architecture can be designed to increase the number of patterns as well as the randomness within the patterns generated. Considering the present analysis between normal LFSR and CA rule 150 based LHCA, 15.625% power reduction is obtained. Further, the present analysis is done on 8-bit BIST application. The same can be applied to optimize the power in 16-bit, 32-bit, 64-bit BIST architectures depending upon the bit width and output characteristics of circuit under test (CUT).

## ACKNOWLEDGMENT

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## REFERENCES

[1] Basturkmen N., Reddy S. and Pomeranz I., "A Low power Pseudo- Random BIST Technique," in Proc. *Int. Conf. on Computer Design(ICCD'02)*, pp. 468-473, 2002.

[2] Ghosh Debjyoti, Bhunia Swarup and Roy Kaushik, " A Technique to Reduce Power and Test Application Time in BIST", in *Proceedings of the 10th IEEE International On-Line Testing Symposium (IOLTS'04),* 2004.

[3] Kilic Hurevren and Oktem Levent, "Low-Power Test Pattern Generator Design for BIST via Non Uniform Cellular Automata" in *IEEE*, pp. 212-215, 2005.

[4] Prasada Rao R. Vara, Varaprasad N. Anjaneya, Babu G. Sudhakar and Mohan C. Murali, "Power Optimization of Linear Feedback Shift Register (LFSR) for Low Power BIST implemented in HDL" in*International journal of modern engineering research*, Volume 3, pp. 1523-1528, 2013.

[5] Sato Yasuo, Wang Senling, Kato Takaaki, Miyase Kohei and Kajihara Seiji," Low Power BIST for Scan-Shift and Capture Power" in *IEEE 21st Asian Test Symposium*, pp. 173-178, 2013.

[6] Shakya Mayank and K.K. Soundra Pandian, "A Power Reduction Technique for BIST using Modified LFSR" in *World Academy of Science, Engineering and Technology*, pp.1117-1120, 2009.

[7] Singh Amandeep, Kumar P. Mohan and Bassi Mohinder, "Strategies and Techniques for optimizing power in BIST: A Review" in *International journal of computer applications*, pp. 38-42, 2014.

[8] Singh Amandeep, Kumar P. Mohan and Singh Amandeep, "Low power Hybrid CA register design for BIST applications" in *International Journal of Advanced Research in Electronics and Communication Engineering*, Issue 3, pp. 617-620, 2014.

[9] Singh Balwinder, Narang Sukhleen Bindra and Khosla Arun, "Analysis of Cellular Automata and Genetic Algorithm based Test Pattern Generators for Built in Self Test" in *Proceedings of Seventh International Conference on Bio-Inspired Computing: Theories and Applications,* 2012.