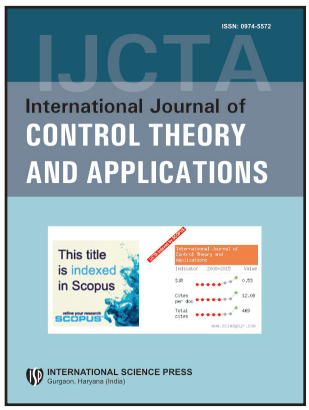

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A Modified H - Bridge Multilevel Inverter with Reduced Number of Switches

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Abstract: In this paper, the design and implementation of new topology in a single phase five level cascaded H-bridge multilevel inverter by using only a five switches and two DC power source. The main objective of this paper is to increase number of levels with a low number of switches and sources at the output without adding any complexity to the power circuit. The main merit of the new topology is to reduce the lower total harmonic distortion, lower electromagnetic interference generation and high output voltage. Various carrier pulse width modulation techniques are proposed, which can minimize the total harmonic distortion. Thus the smooth sinusoidal wave is obtained with reduced harmonics.

Keywords: Casecade H Bridge multilevel inverter, pulse width modulation, Matlab – Simulink, Keil software, Flash magic.

1. INTRODUCTION

An inverter is an electric apparatus that changes direct current (DC) to alternating current (AC). It is not the same thing as an alternator, which converts mechanical energy (e.g. movement) into alternating current. The advantages of inverter is provide quality output, smaller in size, requires less maintenance. The disadvantages of inverter is less efficiency, high cost, high switching loss. To overcome the disadvantages of inverter we are using multilevel inverter. The concept of multilevel converters has been introduced since 1975 [4]. The term multilevel began with the three-level converter [5]. Subsequently, several multilevel converter topologies have been developed [6-13]. However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected.

2. CASCADED MULTILEVEL INVERTER TOPOLOGY

A cascaded multilevel inverter made up of from series connected single full bridge inverter, each with their own isolated dc bus. This multilevel inverter can generate almost sinusoidal waveform voltage from several separate dc sources, which may be obtained from solar cells, fuel cells, batteries, ultra capacitors, etc. This type of converter does not need any transformer or clamping diodes or flying capacitors [16]. Each level can generate five different voltage outputs +2Vdc, +Vdc, 0, –2Vdc and –Vdc by connecting the dc sources to the ac output side by different combinations of the four switches. The output voltage of an M-level inverter is the sum of all the individual inverter outputs. Each of the H-Bridge's active devices switches only at the fundamental frequency, and each H-bridge unit generates a quasi- square waveform by phase-shifting its positive and negative phase legs switching timings. Further, each switching device always conducts for 180° (or half cycle) regardless of the pulse width of the quasi-square wave so that this switching method results in equalizing the current stress in each active device [17]. This topology of inverter is suitable for high voltage and high power inversion because of its ability of synthesize waveforms with better harmonic spectrum and low switching frequency. Considering the simplicity of the circuit and advantages, Cascaded H-bridge topology is chosen for the presented work. A multilevel inverter has four main advantages over the conventional bipolar inverter. First, the voltage stress on each switch is decreased due to series connection of the switches. Therefore, the rated voltage and consequently the total power of the inverter could be safely increased. Second, the rate of change of voltage (dv/dt) is decreased due to the lower voltage swing of each switching cycle. Third, harmonic distortion is reduced due to more output levels. Fourth, lower acoustic noise and electromagnetic interference (EMI) is obtained.[4].

3. SYSTEM DESCRIPTION

The cascade multilevel inverter was first proposed in 1975 [1]. In recent years multi level inverters are used high power and high voltage applications .Multilevel inverter output voltage produce a staircase output waveform, this waveform look like a sinusoidal waveform. The multilevel inverter output voltage having less number of harmonics compare to the conventional bipolar inverter output voltage. If the multilevel inverter output increase to N level, the harmonics reduced to the output voltage value to zero. The multi level inverters are mainly classified as Diode clamped, Flying capacitor inverter and cascaded multi level inverter. The cascaded multilevel control method is very easy when compare to other multilevel inverter because it doesn't require any clamping diode and flying capacitor [2]. There are two PWM methods mainly used in multilevel inverter control strategy. One is fundamental switching frequency and another one is high switching frequency. For high switching frequency classified as space vector PWM, Selective Harmonics Elimination PWM and SPWM. Among these PWM methods SPWM is the most used for the multilevel inverter, because it has very simple and easy to implemented. In this paper present SPWM method with the different carrier based disposition PDPWM, PODPWM and APODPWM has been analyzed. It is generally accepted that the PD strategy gives rise to the lowest harmonic distortion for the line-to-line voltage [13] [14]. Its reduced the total harmonics distrotation and improvement of power quality. Increase the No. of levels to obtained the pure sinusoidal wave form and reduced the lower order harmonics. Any semiconductor switches have already been proposed .In this proposed concept uses the MOSFETs semiconductor switches. MOSFETs are preferred in: High frequency applications (1MHZ), Wide line or load variations, Long duty cycles, and Low-voltage applications (500V). Mainly selected the MOSFET switches are used because of its fast switching capability [15].

1. Proposed System

The Figure 1 shows the proposed system circuit diagram with less No. of switches and sources compared to the exiting five level multilevel H-bridge inverter. The circuit diagram of operation mode with proposed method

of single phase five level cascaded H-Bridge multilevel inverter. It consists of a full-bridge inverter, capacitor voltage divider, an auxiliary circuit comprising four POWER MOSFET switches. The inverter produces output voltage in five levels: zero, Vdc, 2Vdc, 0, –Vdc and –2Vdc.The advantages of the inverter topology are: Improved output voltage quality, Smaller filter size, Lower Electromagnetic interferences, Lower total harmonics distortion compared with conventional five level pulse width modulation ,Reduced number of switches compared to the conventional 5-level inverter.

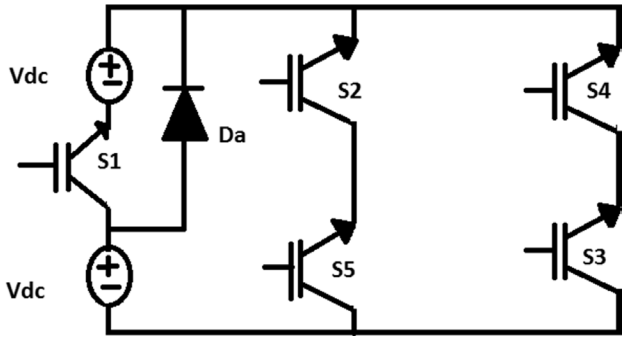


Figure 1: Proposed method of multilevel cascade inverter by using five switches and two source

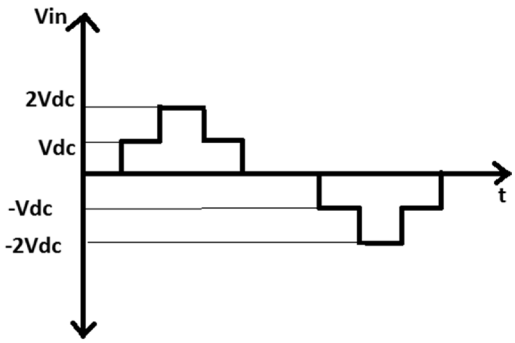


Figure 2: Output waveform of five level multi level inverter

The Figure 2 shows the output wave form of five level multilevel inverter. The cascaded H-bridges multilevel inverter introduces the idea of using separate dc sources to produce an ac voltage waveform. Each H-bridge inverter is connected to its own dc source Vdc. By cascading the ac outputs of each H bridge inverter, ac voltage waveform is produced. By closing the appropriate switches, each H-bridge inverter can produce five different voltages: When a switch S2 and S4 of one particular H-bridge inverter are closed, the output voltage is 0. When a switch S2 and S5 are closed, the output voltage is +Vdc. When a switch S1, S2 and S5 are closed, the output voltage is +2Vdc. When a switch S3 and S5 are closed, the output voltage is 0 when a switch S4 and S5 of one particular H-bridge inverter are closed, the output voltage is –Vdc. When a switch S4 and S5 are closed, the output voltage is +2Vdc. .Where the *i* stands for one particular H-bridge inverter. Therefore, to obtain the total ac voltage produced by the multilevel inverter, these five distinct ac voltages are added together. The one notices that five distinct dc sources can produce a maximum of 5 distinct levels in the output phase voltage of the multilevel inverter. More generally, a cascaded H-bridges multilevel inverter using separate dc sources can produce a maximum of $S' = 4 + (N - 1)$ distinct levels in the output phase voltage. The exciting system used more No. of DC sources while increasing the No. of levels. The proposed system reduced the No. of DC sources and switches also.

2. Modes of Operation

The circuit diagram of proposed method of multilevel cascade inverter. The circuit diagram of operation mode with proposed method of single phase five level cascaded H-Bridge multilevel inverter. It consists of a full-bridge inverter, capacitor voltage divider, an auxiliary circuit comprising four POWER MOSFET switches. The inverter produces output voltage in five levels: zero, Vdc, 2Vdc, 0, –Vdc and –2Vdc.The advantages of the inverter topology are: Improved output voltage quality, Smaller filter size, Lower Electromagnetic interferences, Lower total harmonics distortion compared with conventional five level pulse width modulation, Reduced number of switches compared to the conventional 5-level inverter. The level increased obtain the pure sinusoidal signal and reduced the harmonics. The additional used the diode for the way of path to reduced the switching stress of the circuit. The cascaded H-bridges multilevel inverter introduces the idea of using separate dc sources to produce an ac voltage waveform.

Each H-bridge inverter is connected to its own dc source Vdc. By cascading the ac outputs of each H bridge inverter, ac voltage waveform is produced. By closing the appropriate switches, each H-bridge inverter can produce five different voltages: When a switch S2 and S4 of one particular H-bridge inverter are closed, the output voltage is 0 .When a switch S2 and S5 are closed, the output voltage is +Vdc. When a switch S1, S2 and S5 are closed, the output voltage is +2Vdc. When a switch S3 and S5 are closed, the output voltage is 0 when a switch S4 and S5 of one particular H-bridge inverter are closed, the output voltage is –Vdc. When a switch S4 and S5 are closed, the output voltage is +2Vdc. Where the i stands for one particular H-bridge inverter. Therefore, to obtain the total ac voltage produced by the multilevel inverter, these five distinct ac voltages are added together. The one notices that five distinct dc sources can produce a maximum of 5 distinct levels in the output phase voltage of the multilevel inverter. More generally, a cascaded H-bridges multilevel inverter using separate dc sources can produce a maximum of $S' = 4 + (N - 1)$ distinct levels in the output phase voltage.

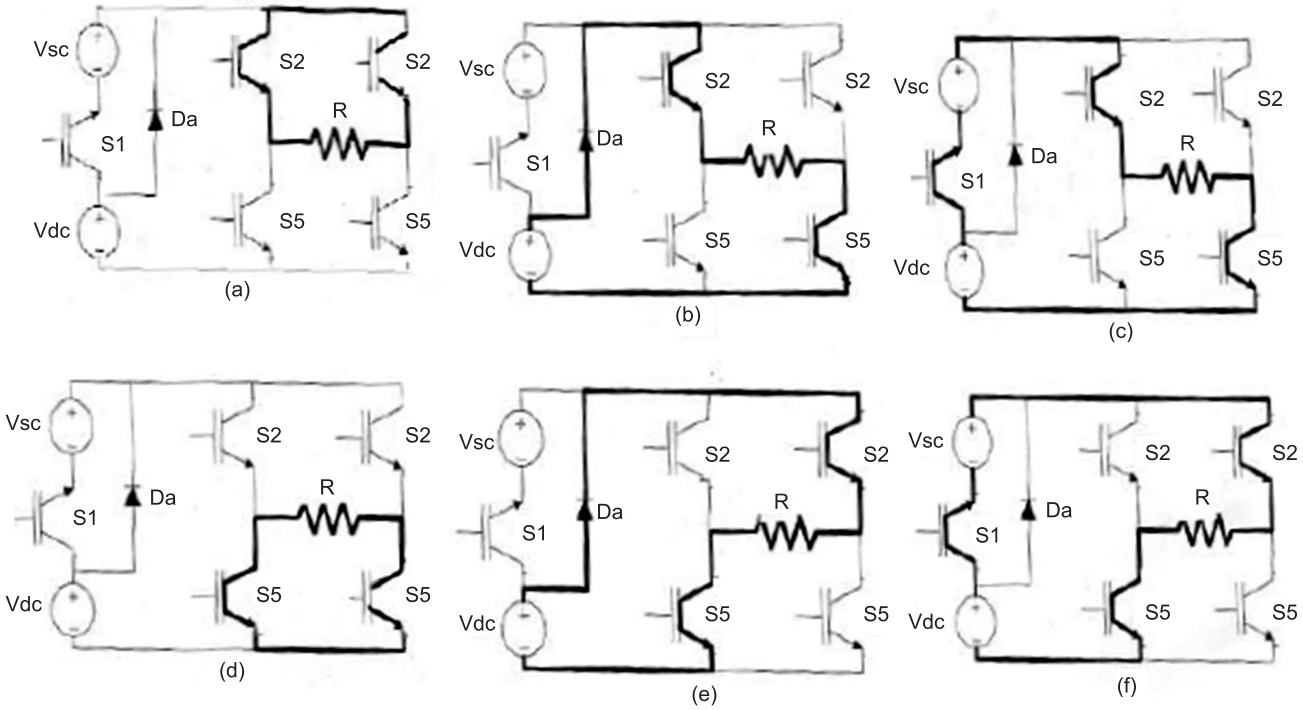


Figure 3: Multilevel cascade inverter operation modes:
(a) 0, (b) Vdc, (c) –2Vdc, (d) 0, (e) –Vdc, (f) –2Vdc

Table 1
Switching sequence of modes of operation

Operation	*DF*	*S1*	*S2*	*S3*	*S4*	*S5*
0	OFF	OFF	ON	OFF	ON	OFF
Vdc	ON	OFF	ON	ON	OFF	OFF
2Vdc	OFF	ON	ON	ON	OFF	OFF
0	OFF	OFF	OFF	ON	OFF	ON
–Vdc	ON	0FF	OFF	OFF	ON	ON
–2Vdc	OFF	ON	OFF	OFF	ON	ON

4. MODULATION TECHNIQUES FOR MULTILEVEL INVERTER

Definition of Modulation Mainly the power electronic converters are operated in the "switched mode". This means the switches within the converter are always in either one of the two states - turned off or turned on. Any operation in the linear region, other than for the unavoidable transition from conducting to non-conducting, incurs an undesirable loss of efficiency and an unbearable rise in switch power dissipation. To control the flow of power in the converter, the switches alternate between these two states. This happens rapidly enough that the inductors and capacitors at the input and output nodes of the converter average or filter the switched signal. The switched component is attenuated and the desired dc or low frequency ac component is retained. This process is called Pulse Width Modulation, since the desired average value is controlled by modulating the width of the pulses. For maximum attenuation of the switching component, the switch frequency fc should be high- many times the frequency of the desired fundamental ac component f1 seen at the input or output terminals. In large converters, this is in conflict with an upper limit placed on switch frequency by switching losses. For POWER MOSFET converters, the ratio of switch frequency to fundamental frequency fc/f1 may be as low as unity, which is known as square wave switching. Another application where the pulse number may be low is in converters which are better described as amplifiers ,whose upper output fundamental frequency may be relatively high. These high power switch-mode amplifiers find application in active power filtering, test signal generation, servo and audio amplifiers. These low pulse numbers place the greatest demands on effective modulation to reduce the distortion as much as possible. The low pulse numbers place the greatest demands on effective modulation to reduce the distortion as much as possible. In these circumstances, multi-level converters can reduce the distortion substantially, by staggering the switching instants of the multiple switches and increasing the apparent pulse number of the overall converter.

1. Pulse Width Modulation

The fundamental methods of pulse-width modulation are divided into the traditional voltage-source and current-regulated methods. Voltage-source methods more easily lend themselves to digital signal processor or programmable logic device implementation. However, current controls typically depend on event scheduling and are therefore analog implementations which can only be reliably operated up to a certain power level. In discrete current-regulated methods the harmonic performance is not as good as that of voltage-source methods. The carrier-based modulation schemes for multilevel inverters can be generally classified into two categories: phase-shifted and level-shifted modulations. Both modulation schemes can be applied to the cascaded H-bridge New Cascaded H-Bridge Multilevel Inverter Topology with Reduced Number of Switches and Sources inverters. Total harmonics distortion of phase-shifted modulation is much higher than level-shifted modulation. Therefore we have considered level-shifted modulation. An m-level multilevel inverter using level-shifted multicarrier modulation scheme requires $(m-1)$ triangular carriers, all having the same frequency and amplitude. The $(m-1)$ triangular carriers are vertically disposed such that the bands they occupy are contiguous. There are three alternative Pulses with different phase relationships for the level-shifted multicarrier modulation three alternative carrier

disposition Pulse width modulation strategies are commonly referenced, viz:

(i) Alternative phase opposition disposition, where each carrier is phase shifted by π from its adjacent Carrier [12].

(ii) Phase opposition disposition where the carriers above the sinusoidal reference zero point are π Out of phase with those below the zero point [12].

(iii) Phase disposition, where all carriers are in phase [12].

(i) Alternate Phase Opposition Disposition (APOD)

In case of alternate phase disposition (APOD) modulation, every carrier waveform is in out of phase with its neighbor carrier by 1800. Since APOD and POD schemes in case of five-level inverter are the same, a five level inverter is considered to discuss about the APOD scheme. The rules for APOD method, when the number of level N = 5, are

1. The N – 1 = 4 carrier waveforms are arranged so that every carrier waveform is in out of phase with its carrier by 180. The converter switches to +I vdc when the reference is greater than all the carrier waveforms.
2. The converter switches to 2Vdc when the reference is less than the uppermost carrier waveform and greater than all other carriers
3. The converter switches to 0 when the reference is less than the two uppermost carrier waveform and greatest than lowermost carrier.
4. The converter switches to –1Vdc when the reference is greater than the lowermost carrier waveform and lesser than all other carriers
5. The converter switches to –2Vdc when the reference is lesser than all the carrier waveforms : Switching pattern produced using the APOD carrier-based PWM scheme for a five-level inverter: Four triangles and the modulation signal

(ii) Phase Opposition Disposition

For phase opposition disposition (POD) modulation all carrier waveforms above zero reference are in phase and are 180° out of phase with those below zero. The rules for the phase opposition disposition method, when the number of level N = 5

1. The N – 1 = 4 carrier waveforms are arranged so that all carrier waveforms above zero are in phase and are 180 out of phase with those below zero
2. The converter is switched to +Vdc when the reference is greater than both carrier waveforms.
3. The converter is switched to zero when the reference is greater than the lower carrier waveform but less than the upper carrier waveform.
4. The converter is switched to +2Vdc when the reference is less than both carrier waveforms.
5. When the modulation signal is greater than both the carrier waveforms, S1 and S2 are turned on and the converter switches to positive node voltage and when the reference is less than the upper carrier waveform but greater than the lower carrier, S2 and S1 are turned on and the converter switches to neutral point. When the reference is lower than both carrier waveforms, S1 an and S2 an are turned on and the converter switches to negative node voltage.

(iii) In Phase Disposition

There in, the a-phase modulation signal is compared with two triangle waveforms. The rules for the in phase disposition method, when the number of level N = 5, are

1. The N – 1 = 5 – 1 = 4 carrier waveforms are arranged so that every carrier is in phase.
2. The converter is switched to +Vdc when the reference is greater than both carrier waveforms.
3. The converter is switched to zero when the reference is greater than the lower carrier waveform but less than the upper carrier waveform.
4. The converter is switched to 2Vdc when the reference is less than both carrier waveforms

5. SIMULATION RESULT

1. Cascade Multilevel Inverter

The Figure 4 shows the simulink diagram of cascade multilevel inverter for five level switching used H bridge circuit. The gate signal generated by the open loop system for the each switching.

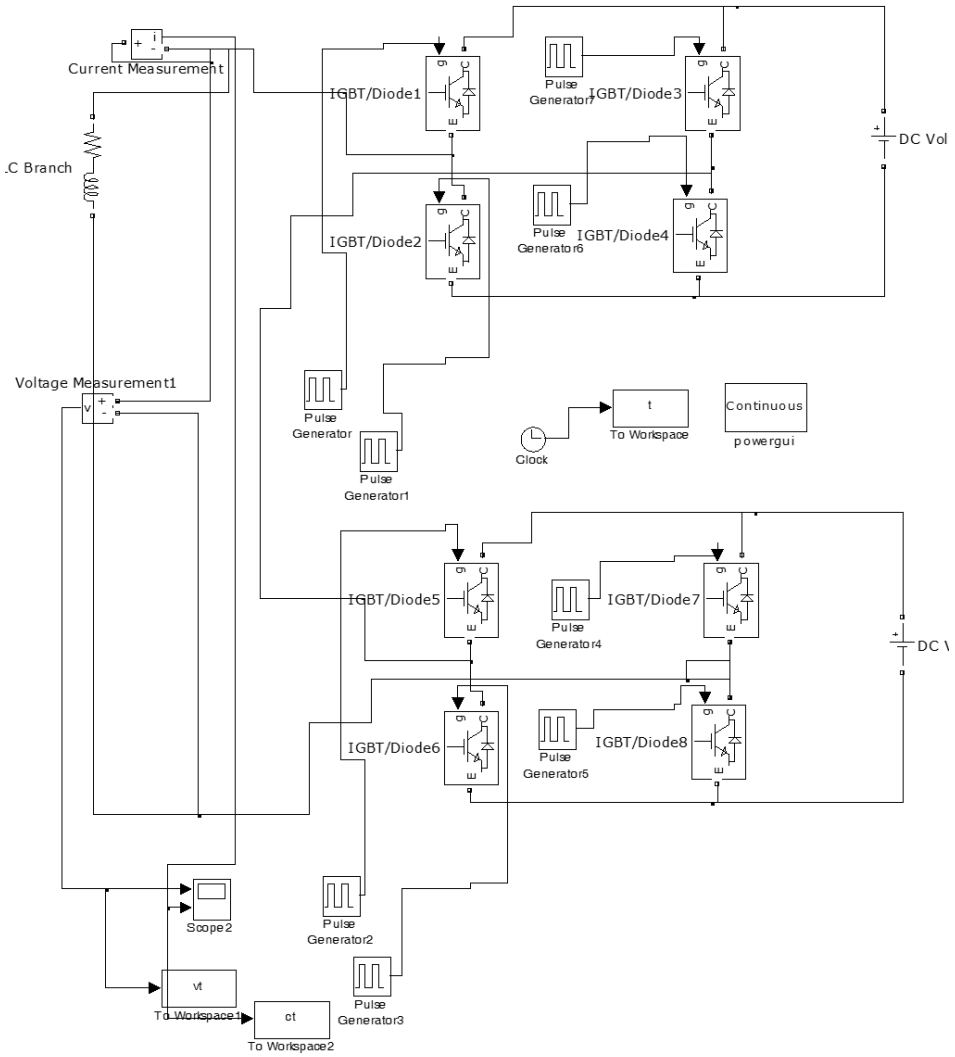


Figure 4: Simulink diagram of Cascade multilevel Inverter

2. Output Waveform

The Figure 5 and 6 shows the output waveform for the cascaded multilevel inverter. Figure shows the voltage, current waveform for both R and RL load. The R load achieve the pure pulse waveform and RL load achieve the some distortion obtained.

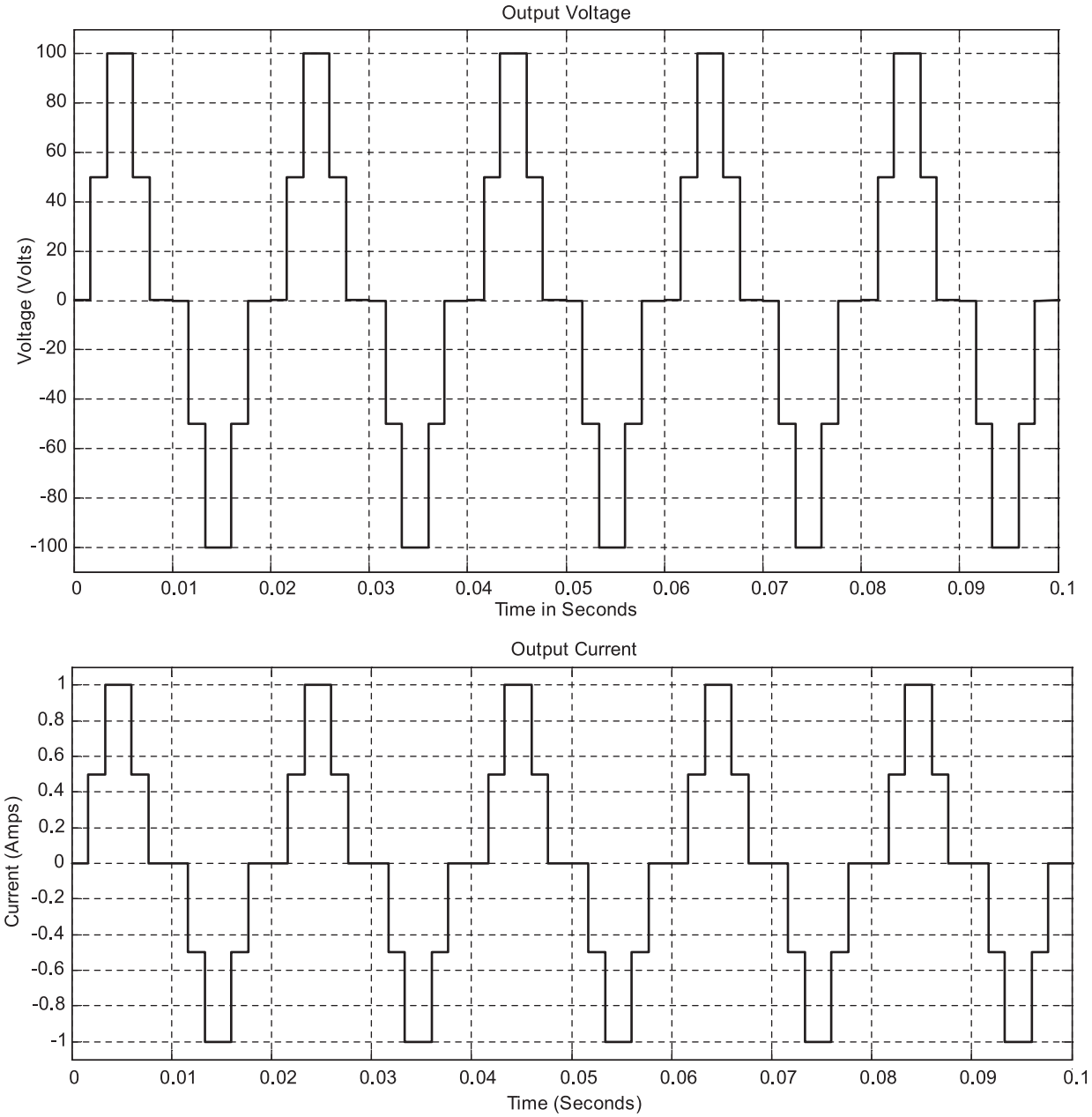


Figure 5: Output Waveform for Voltage and Current– R Load

3. Proposed System Simulation Diagram for Multilevel Inverter

The Figure 7 shows the proposed multilevel inverter simulink diagram. The switches used the five MOSFETs and one diode, the load used for resistive load. Base on the switching sequence generate the wave forms. The

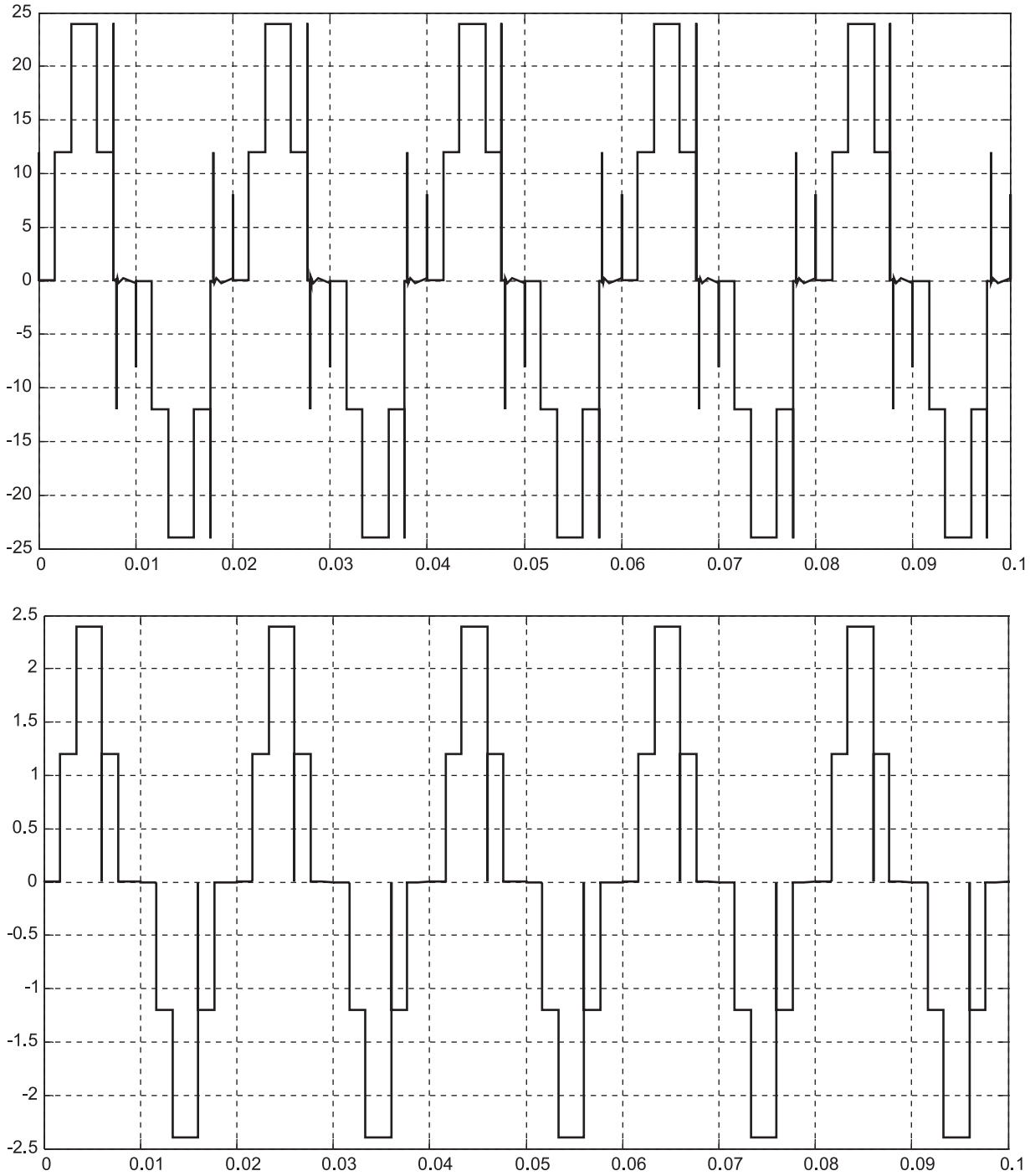


Figure 6: Output Waveform for Voltage and Current–RL Load

circuit has five switches and two sources, the switches reduced the switching stress and losses, reduced the No. of components compare to the H-bridge multilevel inverter. The each arm connected with the two switches and one switch connected in between the two DC sources. Use the pulse generator to generate the various pulse across the various switches. The diode used for the switching sequence in the various level obtained in the output wave form.

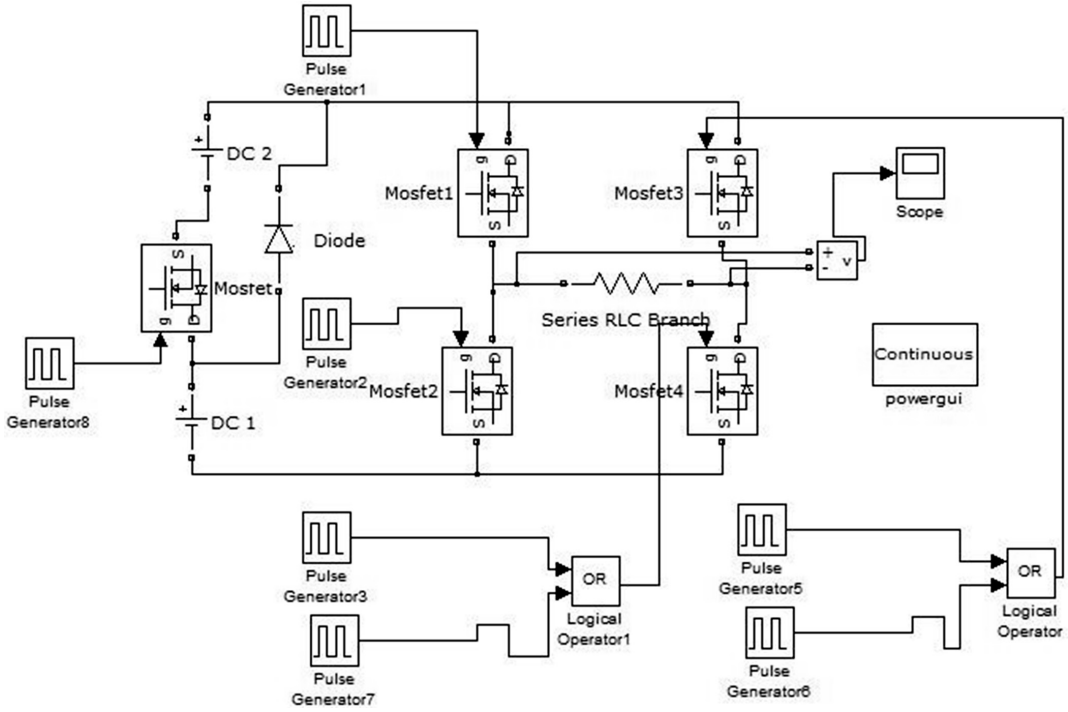


Figure 7: Simulink Diagram of Proposed Multilevel Inverter

4. Switching Waveform

The switching pulses are shown in Figure 8, the switches are S1, S2, S3, S4, S5. The third and fourth switches are generated by the comparative with two signals. The switch 5 has fifty percentage of on and off condition. The switch 2 has invert of the switch 5 sequence. The switching sequence generate the based on the expression given on the Table 1. In the hardware implementation used as a driver circuit for strengthening the controller signal.

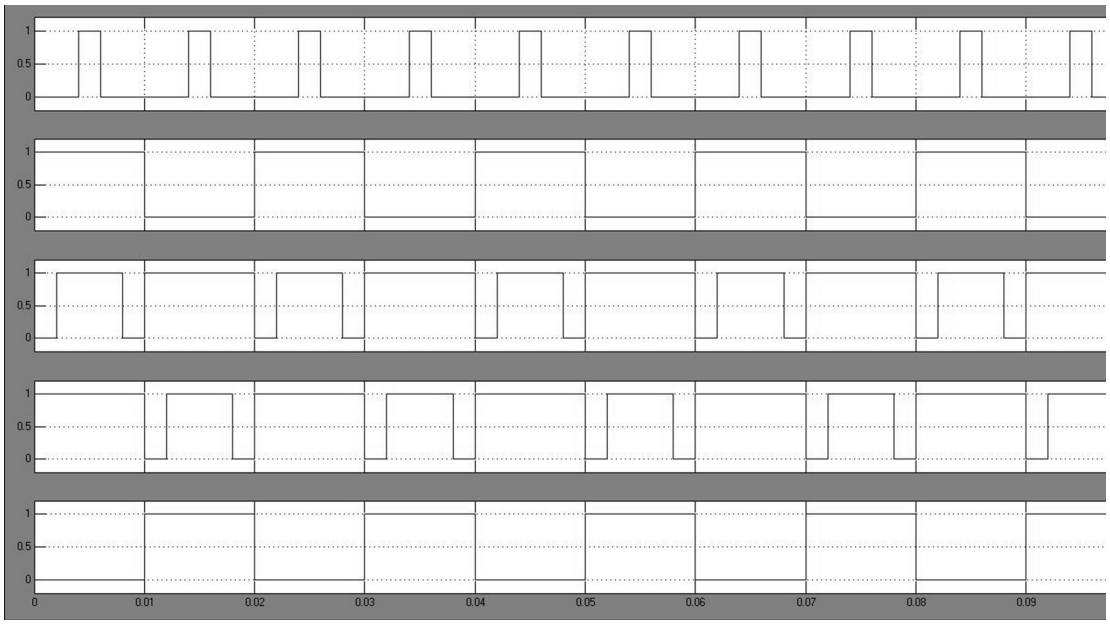


Figure 8: Switching Waveform for proposed system

5. Output Waveform

The Figure 9 shows the output waveform for the proposed multilevel inverter. They shows the voltage, current waveform for both R and RL load. The R and RL load achieve the pure pulse waveform. Compare to the H bridge cascade multilevel inverter the proposed waveform has get pure five level waveform. The power factor also get the unity value.

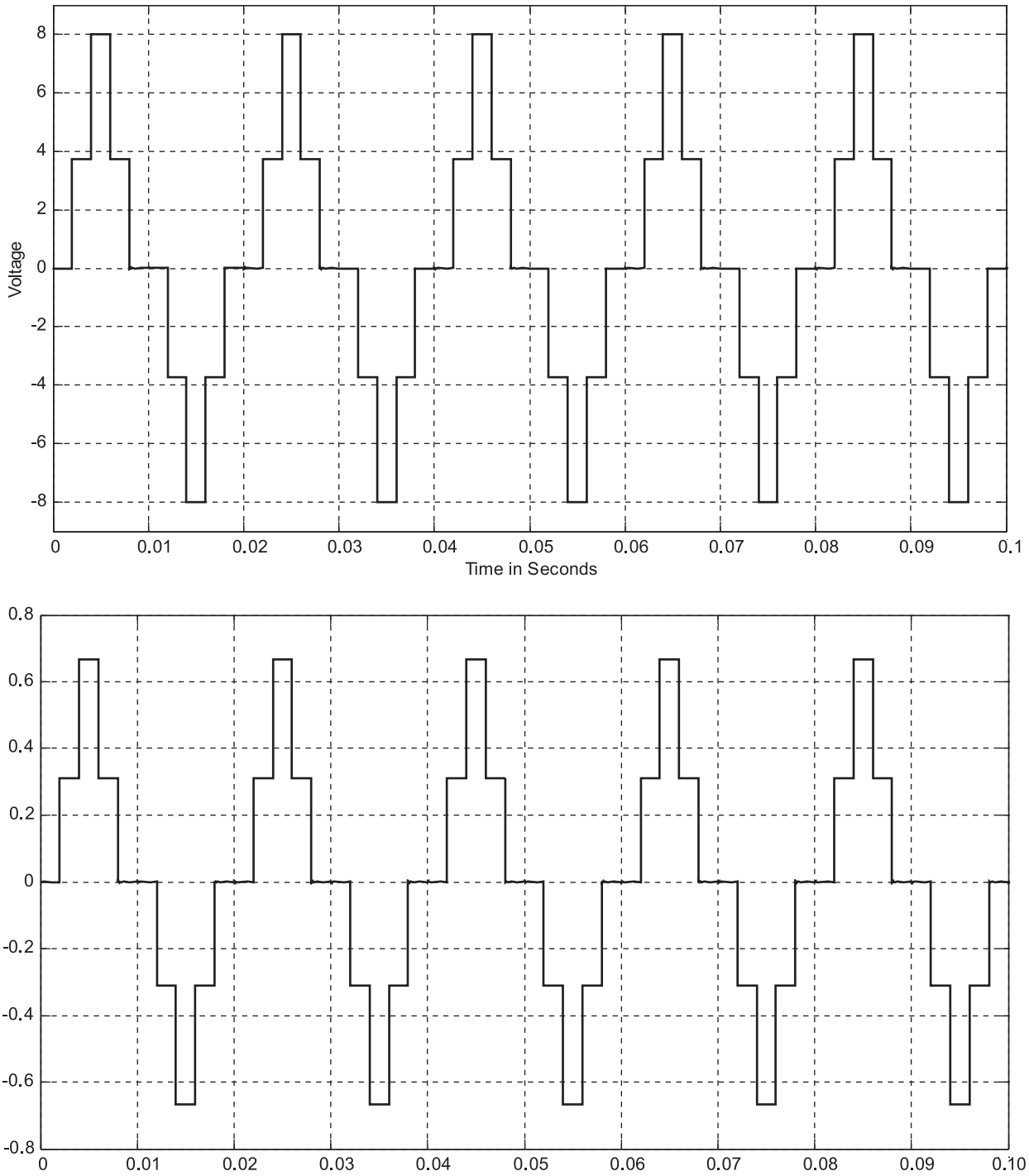


Figure 9: Output Waveform for Voltage and Current–R Load

6. PWM PULSE USING P89V51RD2 MICROCONTROLLER

1. Introduction

Digital controllers for DC-DC converters have been verified as having many advantages as compared to the analog controllers. A high resolution digital pulse-width modulator (DPWM) is required to achieve precise output voltage regulation and eliminate errors to the quantization effects of the ADC and the DPWM. In recent years, several methods are proposed for PWM generation .

2. Pulse Width Modulation

Pulse-width modulation (PWM) is a commonly used technique for controlling power to inertial electrical devices, made practical by modern electronic power switches.

The average value of voltage (and current) fed to the load is controlled by turning the switch between supply and load on and off at a fast pace. The longer the switch is on compared to the off periods, the higher the power supplied to the load is. The term duty cycle describes the proportion of 'on' time to the regular interval or 'period' of time; a low duty cycle corresponds to low power, because the power is off for most of the time. Duty cycle is expressed in percent, 100% being fully on.

The main advantage of PWM is that power loss in the switching devices is very low. When a switch is off there is practically No. current, and when it is on, there is almost No. voltage drop across the switch. Power loss, being the product of voltage and current, is thus in both cases close to zero. PWM also works well with digital controls, which, because of their on/off nature, can easily set the needed duty cycle.

3. Trainer Kit Hardware Details

The Figure 10 shows the trainer kit. Use this trainer kit to generate the various PWM pulses. It have a seven segment display and liquid crystal oscillator are available for display purpose.

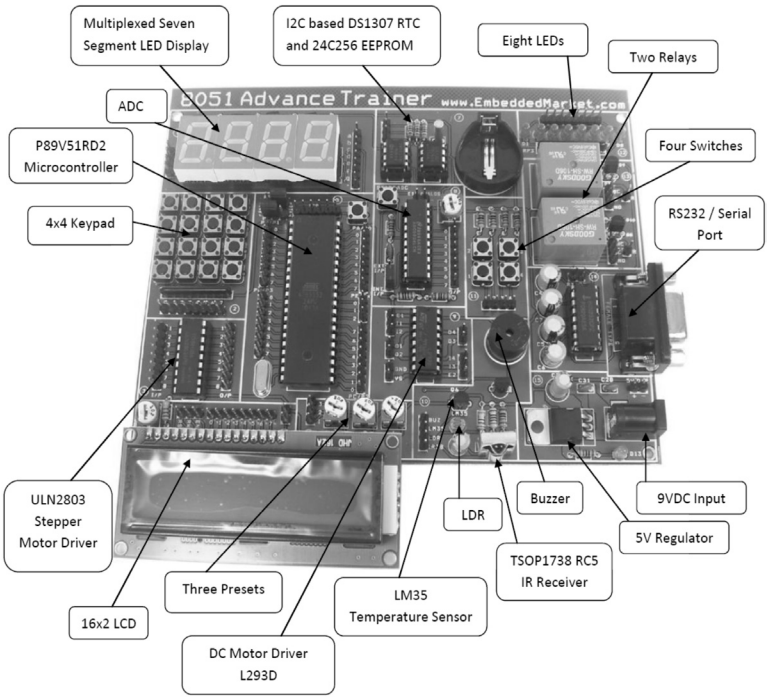


Figure 10: Hardware Trainer Kit

Features

- Floating channel designed for bootstrap opera
- Fully operational to +500 V or +600 V
- Tolerant to negative transient voltage, dV/dt imm
- Gate drive supply range from 10 V to 20 V
- Under voltage lockout for both channels
- 3.3 V logic compatible

4. Keil Software

Using the keil software to generate the pulse waveform. The keil software has used to convert the assembly language program to hex code. The Figure 11 shows the pulse output wave form by using the keil software. Write the program for generate the control signal for all five switches.

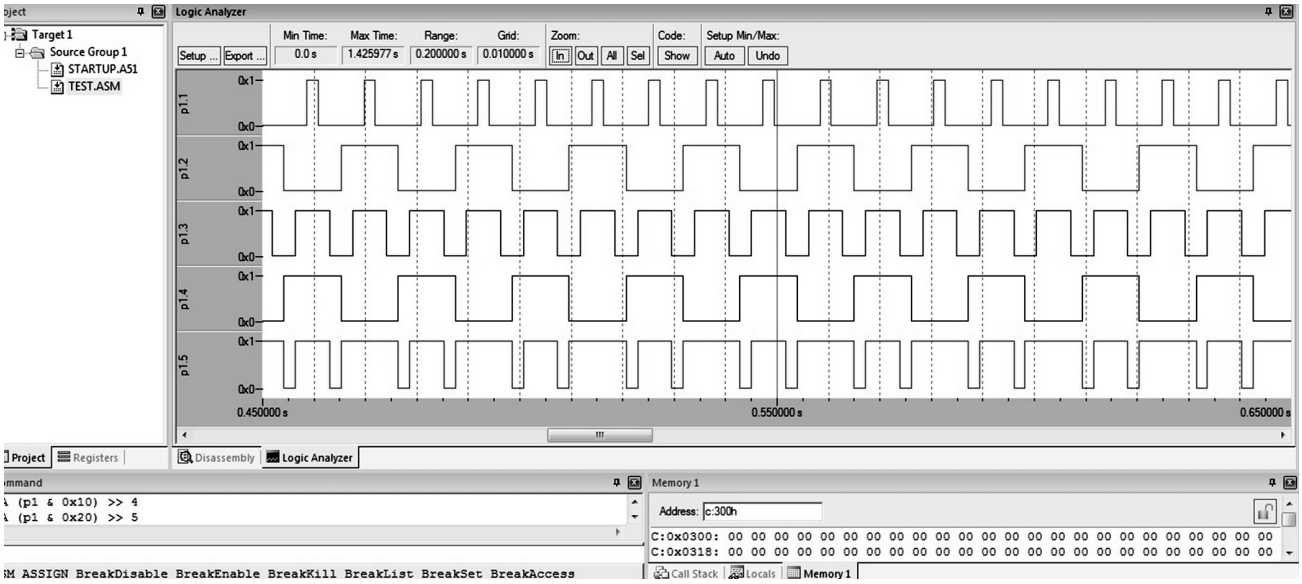


Figure 11: Switching waveform from Keil Software

5. Flash Magic Software

The Figure 12 shows the burning of the IC by using the Flash Magic software. The hex code burn to the controller IC. This software has used for the convert the high level language to hardware level language program. The microcontroller has easily adopt this conversions.

7. HARDWARE IMPLEMENTATION

1. Proposed Multilevel Inverter

The new cascaded five level multilevel Inverter circuit is designed as shown in Figure.13. It consists of a full-bridge inverter, capacitor voltage divider, an auxiliary circuit comprising four POWER MOSFET switches. The inverter produces output voltage in five levels: zero, Vdc, 2Vdc, 0, –Vdc and –2Vdc. The figure shows the including the driver circuit for the proposed system.

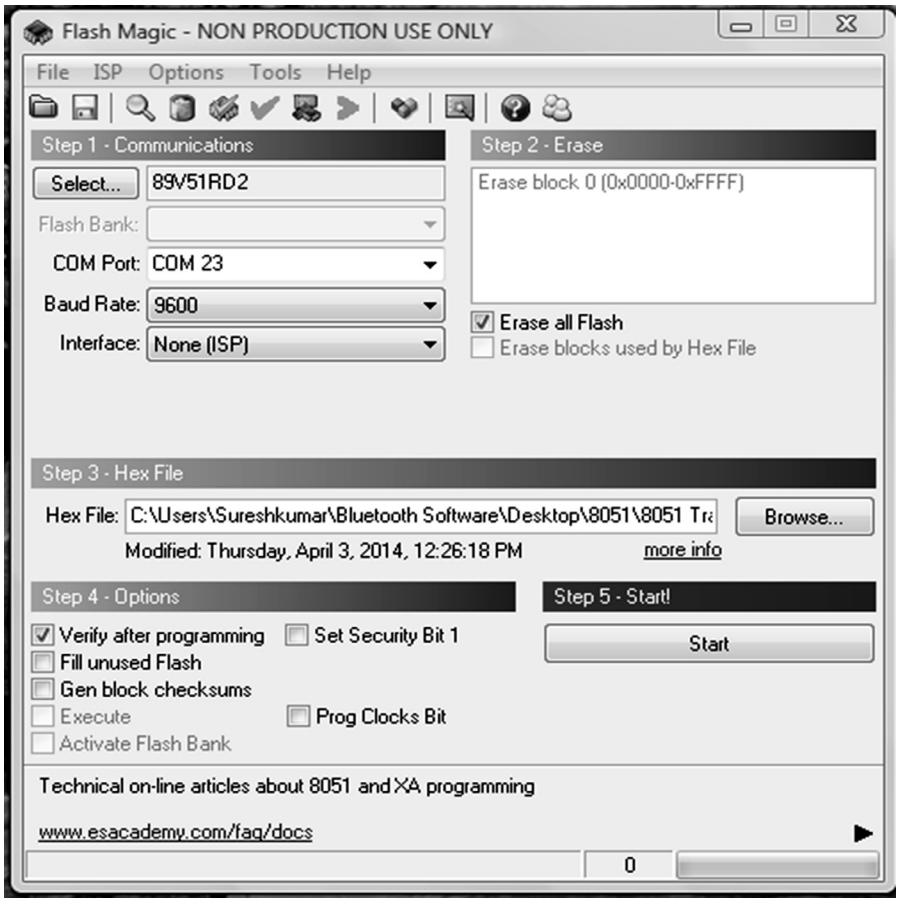


Figure 12: Burn program using Flash Magic Software

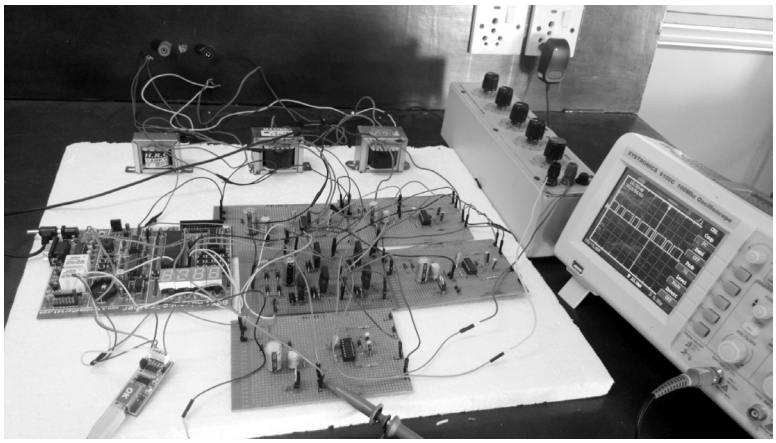


Figure 13: Proposed Inverter Hardware Circuit

2. Driver Circuit

The driver circuit for the multilevel inverter circuit is designed with the help of a 8051 Microcontroller and driver IC (IRS2110). The 8051 Microcontroller is used to develop the PWM pulses for triggering the MOSFET in the Inverter Circuit to obtain the desired output voltage. The driver IC is used to develop the high voltage and high speed for the MOSFET device.

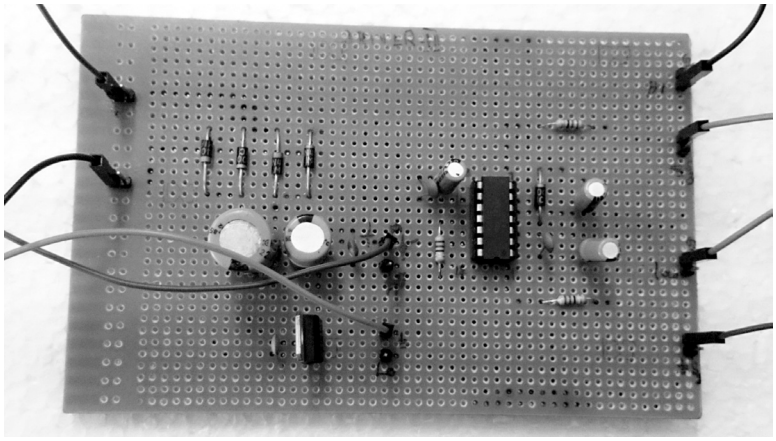


Figure 14: Hardware of Driver Circuit

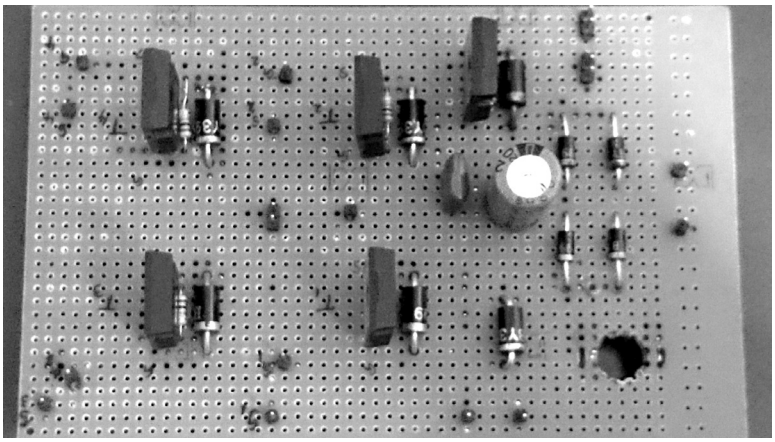
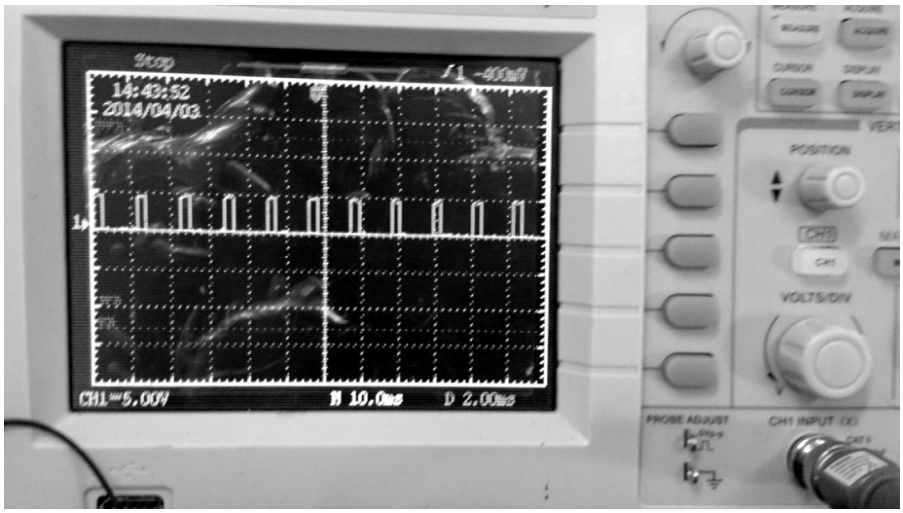


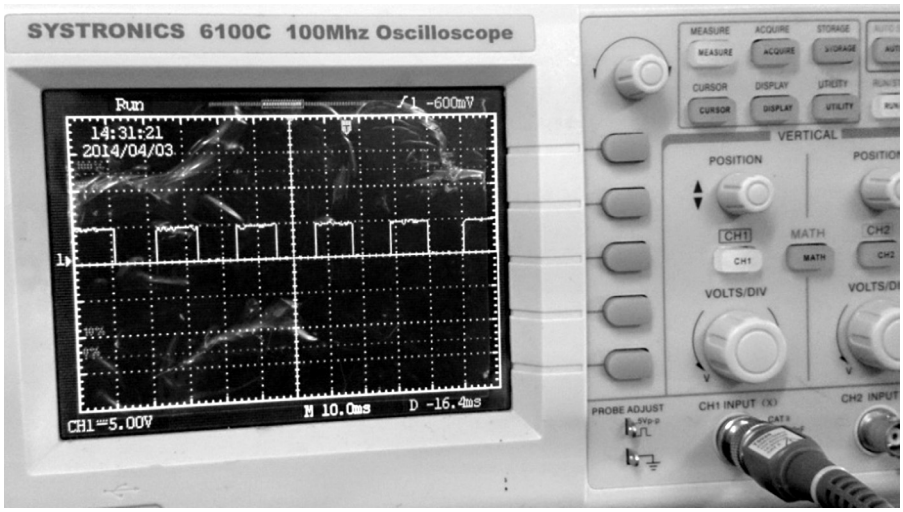
Figure 15: Proposed Multilevel Inverter Circuit

3. Switching Output Waveform

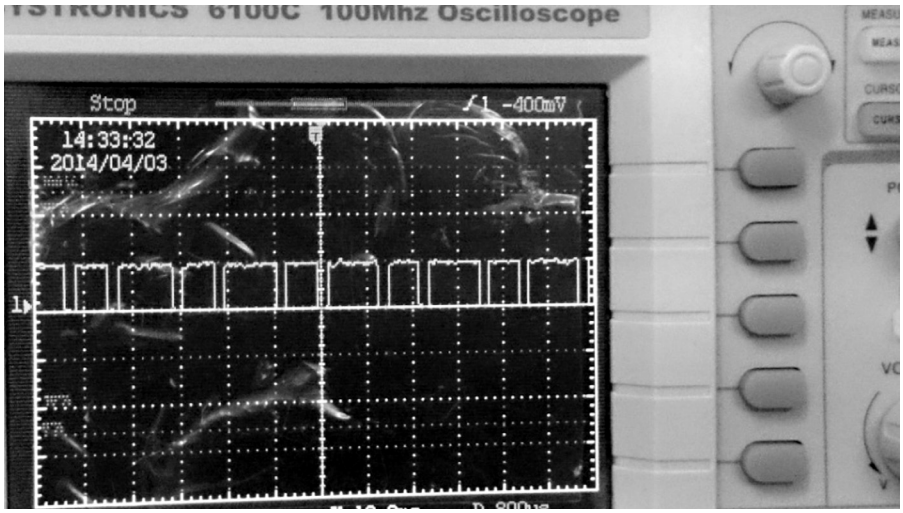
The Figure 16 shows the output wave form for the various switches.



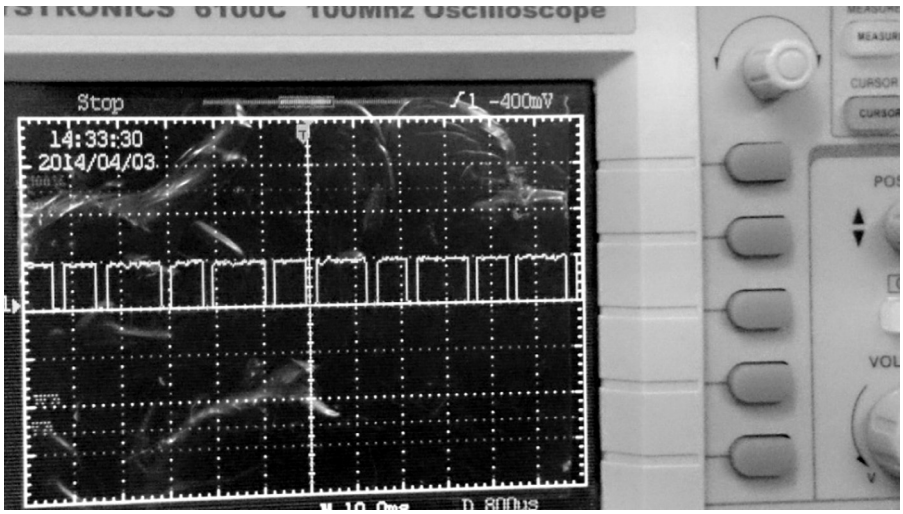
(a)


SYSTRONICS 6100C 100Mhz Oscilloscope
Run
14:31:21
2014/04/03
CH1 5.00V
M 10.0ms
D -16.4ms
VERTICAL
POSITION
MATH
VOLTS/DIV
PROBE ADJUST
CH1 INPUT
CH2 INPUT

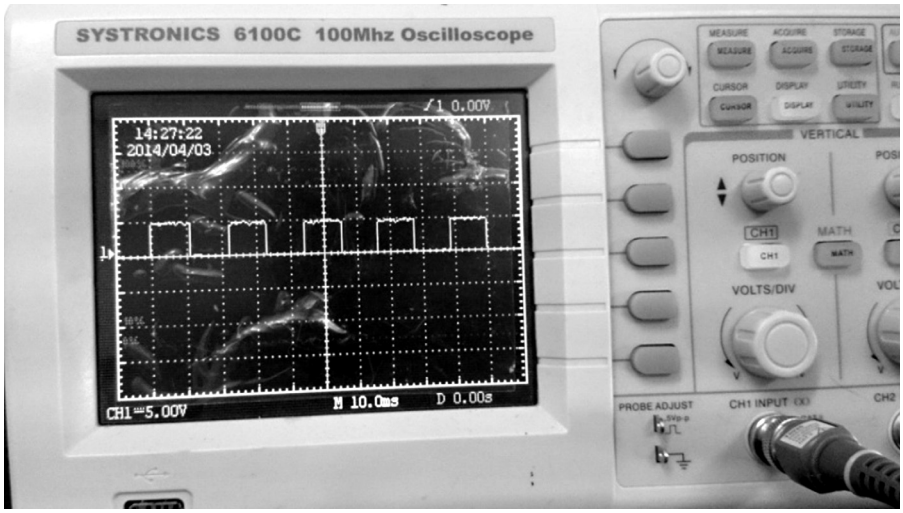
(b)


Stop
14:33:32
2014/04/03

(c)


Stop
14:33:30
2014/04/03

(d)



(e)

Figure 16: Output Waveform of Multi Level Inverter:
(a) S1 Switch, (b) S2 Switch, (c) S3 Switch, (d) S4 Switch, (e) S5 Switch

8. CONCLUSION

The 5-level single-phase multilevel cascaded inverter consists of a single-phase inverter and single H-bridge inverters that it uses separate dc power sources. The control signals for power electronic switches are by using different pulse width modulation modulated technique. In this paper both simulation results and hardware prototype model results are correlated. Harmonic analysis carried out using Mat Lab 8.0 version software. It is proved that proposed work of Single phase five level multilevel cascade inverter output voltage total harmonics distortion is reduced and improve the efficiency of system compare with different topologies of single phase five level multilevel cascade inverter. It is also proved that low total harmonics distortion in phase disposition pulse modulation compared to Phase opposition disposition pulse width modulation and Alternate phase opposition disposition pulse width modulation of multilevel cascade inverter. Future plan is to implementated both simulation and hardware prototype model of the closed loop of single phase five level multilevel cascade Inverter.

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