**I J C T A**, 9(16), 2016, pp. 8313-8323


# Grid Connected Reduced Switch Inverter For Solar Photovoltaic Systems

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**ABSTRACT**

Multilevel Inverters have made another rush of enthusiasm for industry and exploration. This paper focuses the framework associated PV based multilevel inverter that goes for the enhancing the nature of the vitality accessible at the inverter terminals by embracing the split capacitor based topology that utilizations just single dc supply to produce the required yield levels. The split capacitors are considered to acquire ventured yield by time period exchanging plan. The no of semiconducting switches are diminished with a change in consonant variable. The force yield is then separated and synchronized to network power framework. The proposed plot in this manner results in critical decrease in THD and empowers the inverter to work under unhinged PV conditions. The effects of the proposed topology are checked utilizing MATLAB recreation and equipment utilizing dsPIC30F4011 controller.

***Keywords:*** Multi Level Inverter, Grid Connected Inverter, Time Frme based Switching Scheme

## 1. INTRODUCTION

Renewable Energy is characterized as vitality that is gathered from assets which are actually recharged on a human timescale, for example, daylight, wind, downpour, tides, waves, and geothermal warmth. Photovoltaic (PV) power structure is involving a critical part in the progression of appropriated electric force frameworks a Micro lattices. So as to accomplish minimal effort and smallness, and also expanded dependability and proficiency, the idea of the transformer less PV network associated inverter was proposed. The possibility of new Multi Level Inverter (MLI) is to utilize the accessible dc voltage sources to produce a different yield voltage level discussed in [1]. In this paper another decreased switch topology form of MLI by supplanting dc sources with split capacitors is proposed. The arrangement capacitors are associated with a solitary dc source. It performs taking into account a Time Frame Switching Scheme (TFSS) that will attempt to copy the predefined parameter of a reference sine wave (i.e., adequacy and recurrence) or the network voltage (Vg) .The possibility of Multi Level Inverter (MLI) is to utilize the accessible dc voltage sources to create a various yield voltage level discussed in [2]. Subsequently enhances symphonious twisting element by diminishing the lower request sounds. In this paper another decreased switch topology variant of MLI by supplanting dc sources with split capacitors is proposed. The arrangement capacitors are associated with a solitary dc source. It performs in view of a Time Frame Switching Scheme (TFSS) that will attempt to mirror the predefined parameter of a reference sine wave (i.e., adequacy and recurrence) or the framework voltage (Vg).The proposed topology receives decreased number of semiconductor exchanging gadgets and symphonious element is enhanced when contrasted and the traditional strategies discussed in [2]&[3]. The reproduction results are confirmed by equipment execution utilizing a dsPIC30F4011 controller. A solitary stage seven-level inverter for matrix associated photovoltaic frameworks, with a novel heartbeat width-adjusted (PWM) control plan presented in [4]. In [5] another multilevel converter topology that has numerous progressions with less power electronic switches. The circuit comprises of arrangement associated sub multilevel converters squares. The ideal structures of this topology are examined for different destinations,

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for example, least number of switches and capacitors, and least standing voltage on switches for delivering most extreme yield voltage steps. Another calculation for determination of dc voltage source extents has likewise been introduced in [6]. In [7] expressed a novel multilevel inverter with a little number of exchanging gadgets. It comprises of a H-span and an inverter which yields multilevel voltage by exchanging the dc voltage sources in arrangement and in parallel. In [8] &[9] expressed a control strategy connected to a three-stage shunt dynamic channel taking into account a NPC inverter, demonstrating the displaying method expected to complete the proposed control. The inverter advancements for interfacing photovoltaic (PV) modules to a solitary stage framework examined in [10]. In [11] expressed that another unbiased point-clipped heartbeat width regulation (PWM) inverter made out of primary exchanging gadgets which work as switches for PWM and helper changing gadgets to cinch the yield terminal potential to the impartial point potential has been produced. In [12] & [13] expressed that the multilevel inverter innovation has developed as of late as a critical option in the range of high-power medium-voltage vitality control. This paper exhibits the most imperative topologies like diode-braced inverter (nonpartisan point cinched), capacitor-clipped (flying capacitor), and multi cell with isolated DC sources. Developing topologies like awry half and half cells and delicate exchanged multilevel inverters are additionally talked about. In [14] & [15] expressed another topology for multilevel converter in light of sub-multilevel converter units and full-connect converters is proposed. The proposed topology fundamentally decreases the quantity of dc voltage sources and switches as the quantity of yield voltage levels increments. This paper is organized as follows. The solar pv systems and the design parameters of the proposed topology are described in section 2. The concept of the proposed Time Frame Switching Scheme (TFSS) is described in section 3. The simulated and experimental results of the proposed topology are discussed in section 4. Finally, the conclusion is discussed in 5

## 2. SOLAR PV SYSTEMS

A solar cell is essentially a p-n intersection which is produced using two distinctive layers of silicon doped with a little amount of polluting influence particles. The subsequent equal circuit of a sunlight based cell is appeared in figure 1.

Sun based modules utilize light vitality (photons) from the sun to produce power through the photovoltaic impact. The dominant part of modules uses wafer-based crystalline silicon cells or slender film cells taking into account cadmium telluride or silicon. Electrical associations are made in arrangement to accomplish a sought yield voltage and/or in parallel to give a wanted current capacity. The phones must be associated electrically to each other and to whatever is left of the framework. Remotely, well known physical use photovoltaic modules use MC3 (more seasoned) or MC4 connectors to encourage simple weatherproof associations with whatever is left of the framework. In [16] sidestep diodes might be fused or utilized remotely, if there should be an occurrence of incomplete module shading, to amplify the yield of module areas still lit up. Some late sun oriented module outlines incorporate concentrators in which light is engaged

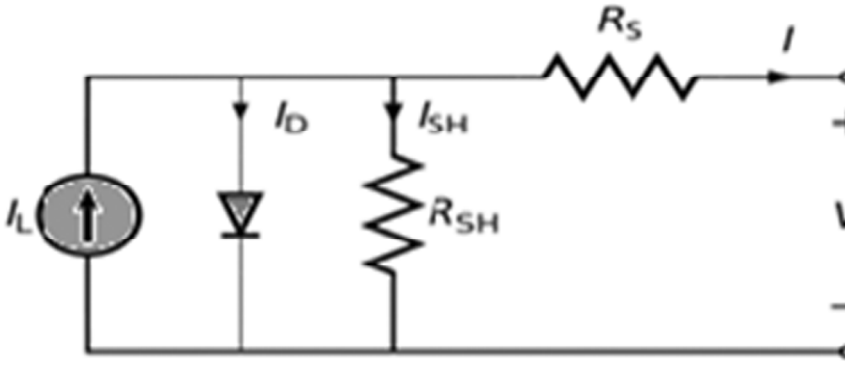


**Figure 1: Equivalent circuit of solar cell**

by lenses or mirrors onto a variety of littler cells. This empowers the utilization of cells with a high cost for each unit territory discussed in [17]&[18].

### 2.1. Maximum Power Point Tracking

Most extreme force point following (MPPT) is a strategy utilized with wind turbines and photovoltaic (PV) heavenly bodies to boost power output appeared in figure 2.In this arrangement, power streams straightforwardly to a battery bank. A minor departure from these setups is that rather than stand out single inverter, smaller scale inverters are sent, one for each PV board presented in [19]. The fill variable abridged FF, is a parameter which describes the non-straight electrical conduct of the sunlight based cell. Fill element is characterized as the proportion of the most extreme force from the sunlight based cell to the result of Open Circuit Voltage Voc and Short-Circuit Current Isc. In arranged information it is regularly used to appraise the greatest force that a cell can furnish with an ideal burden under given conditions,

$$P = FF \times Voc \times Isc \quad (1)$$

For any given arrangement of operational conditions, cells have a solitary working point where the estimations of the present (I) and voltage (V) of the cell result in a most extreme force yield. These qualities compare to a specific burden resistance, which is equivalent to V/I as determined by Ohm's Law. The force P is given by P = V*I. A photovoltaic cell, for the dominant part of its valuable bend, goes about as a

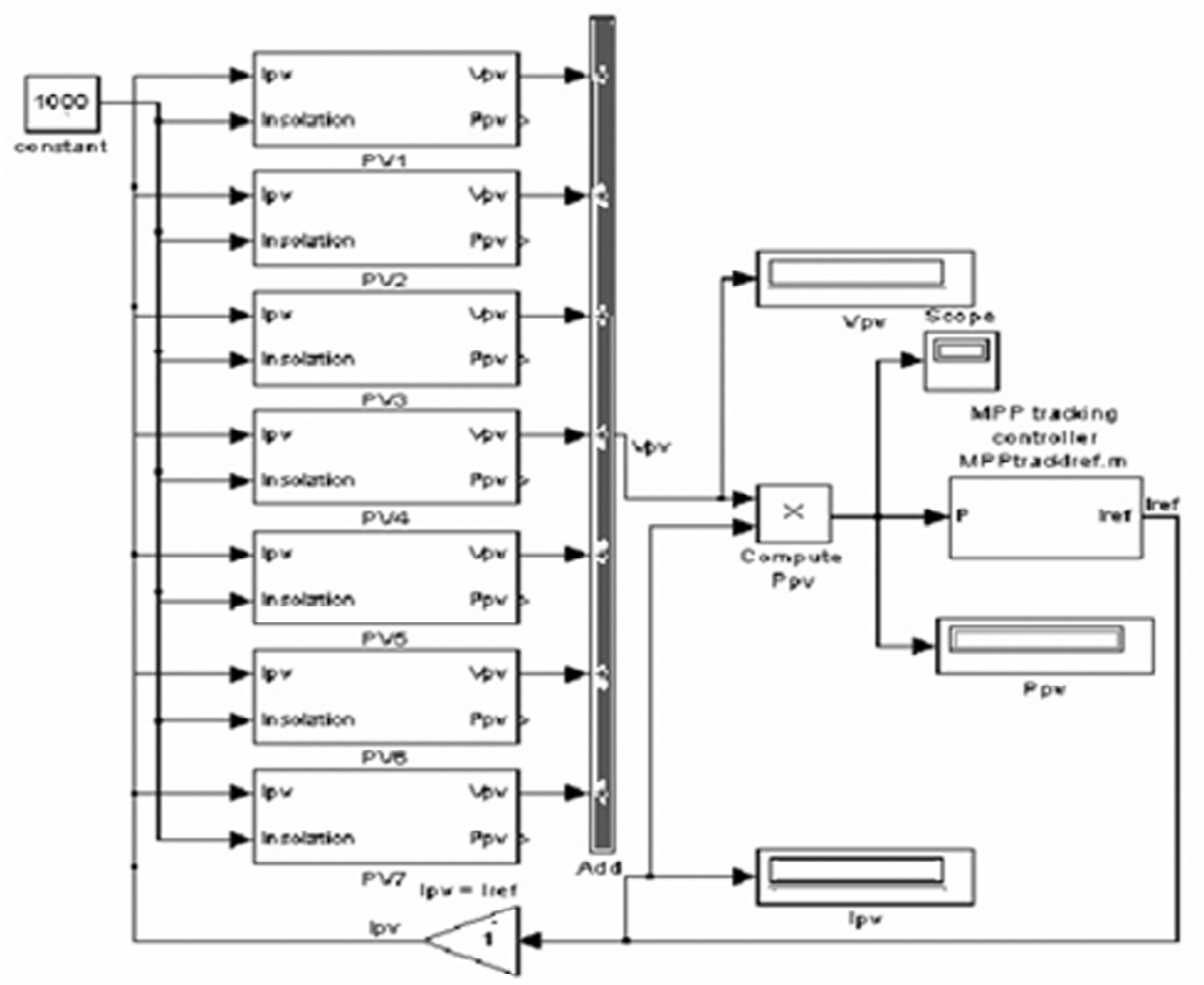


**Figure 2: MPPT for PV module**

consistent current source. Be that as it may, at a photovoltaic cell's MPP area, its bend has a roughly reverse exponential relationship amongst current and voltage. From fundamental circuit hypothesis, the force conveyed from or to a gadget is advanced where the subsidiary (graphically, the slant) dI/dV of the I-V bend is equivalent and inverse the I/V proportion (where dP/dV = 0). This is known as the greatest force point (MPP) and relates to the "knee" of the bend.

## 3. SYSTEM

The proposed topology embraces diminished number of semiconductor Switching gadgets and consonant variable is enhanced when contrasted and the established strategies as appeared in figure 3. The force yield from inverter is then sifted utilizing inactive inductor part and after that synchronized to nourish the network power framework. The reenactment results are confirmed by equipment usage utilizing a dsPIC30F2010 controller. The proposed lattice interfacing strategy utilizes ZCD to discover the recurrence of the framework and to keep up the brace voltage and inverter current stage point. In this way, it is not required to apply extraordinary or palindrome capacities for the count of the limit points to interface the inverter to network. Subsequently straightforward microcontroller is sufficient to interface the MLI to framework.

The proposed topology comprises of 6 capacitors, 6 source switches and 4 H bridge switches. It is supplied with a solitary dc source. The proposed topology is appeared in Figure 4. It comprises of single dc Source (Vdc) associated over a progression of capacitors (CN). The voltage over the information supply is symmetrically dropped over these capacitors (VCN). The disseminated voltages are then delivered over the heap in rising stride style by successive exchanging of source switches (SN). The H Bridge switches (IGN) are utilized to invert the extremity over the heap. The quantity of capacitors (CN) is resolved taking into

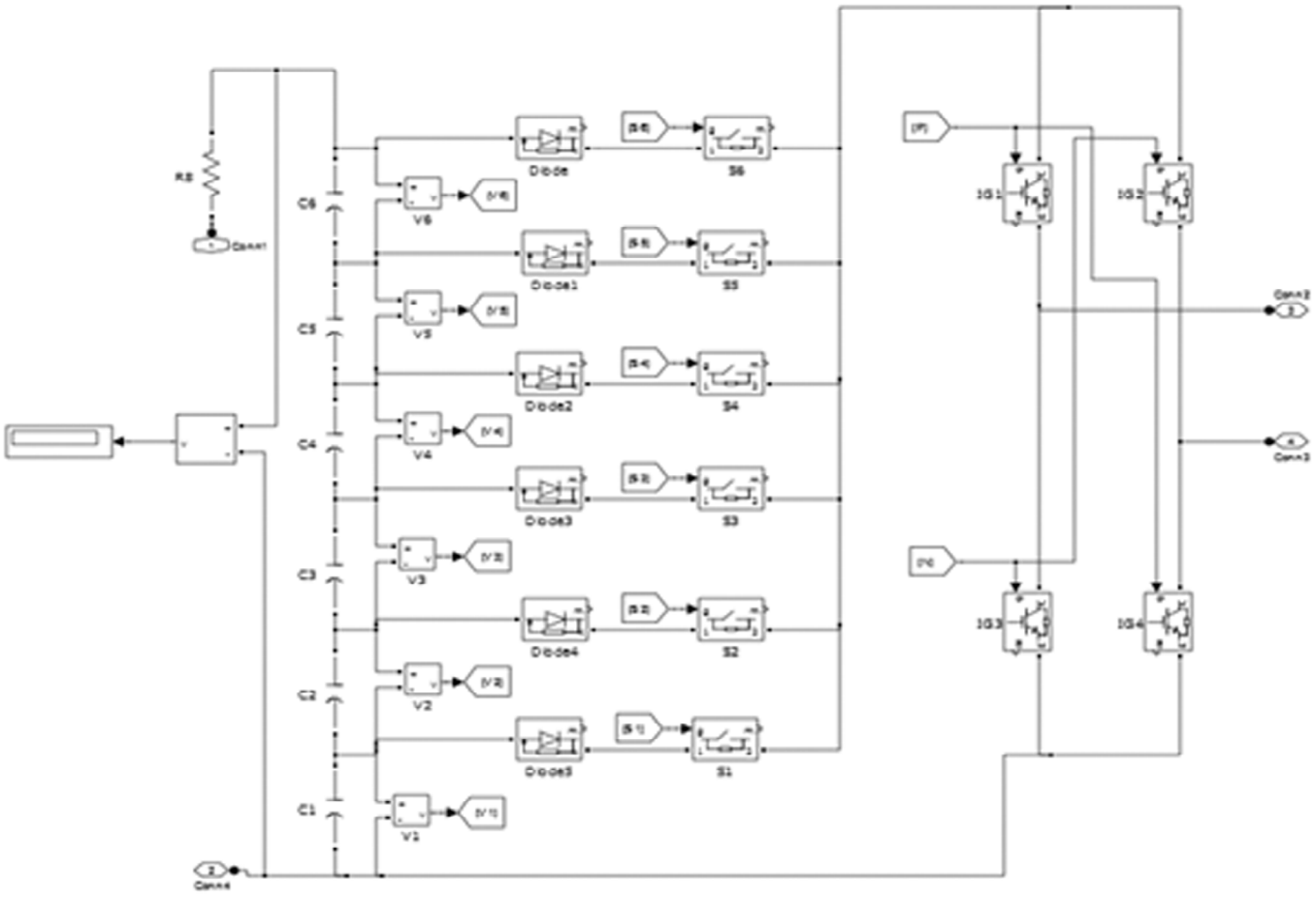


**Figure 3: Proposed system model**

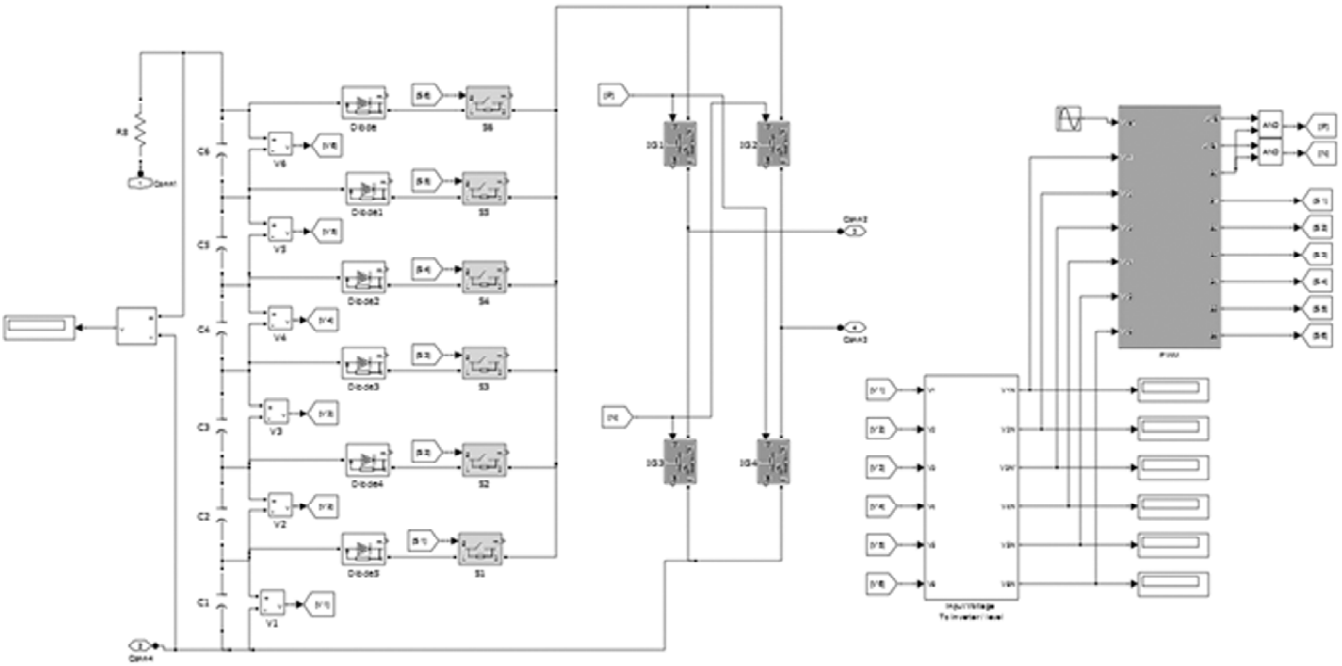

**Figure 4: Circuit diagram of a single phase grid connected reduced switch multilevel inverter based on time frame switching**

account for the required m yield levels:The topology is proposed to acquire thirteen level yield voltage waveform. It comprises of 6 capacitors (i.e., C1, C2, C3, C4, C5 and C6), six source switches (i.e., S1, S2, S3, S4, S5, S6) and four H Bridge switches (IG1, IG2, IG3, IG4).

The working principle of the proposed topology is understood in analogy with the working of a potentiometer. In a potentiometer output voltage is varied by changing resistance value. In a similar fashion the capacitor takes the role of resistor and the voltage across the load is subjected to vary based on the number of capacitors selected (i.e., active capacitors).

$$VC1 = VC2 = VC3 = VC4 = VC5 = VC6 = Vd \quad (2)$$

The polarity of the output voltage are interchanged in every half cycle of the reference sine wave by triggering one of the either pair of the H bridge switches. Initially, all the switches are left open and will result in zero output voltage across the load. Contrarily, during that instant the capacitors are made to charge in the opposite direction. During the positive half cycle of the output IG1 and IG4 are closed. When the source switch S1 is triggered alone, the voltage drop across the capacitor C1 is obtained. This is because the portion of input voltage Vdc (i.e., 5 Vdc/6) is dropped across the inactive capacitors C2–C6. The resultant voltage (i.e., Vdc/6) across the active capacitor C1 is only obtained across the load. When the source switch S2 is triggered alone, the resultant voltage (i.e., Vdc/3) across the active capacitor C1 and C2

**Table 1**
**Output voltage ($E_N$) across the load due to capacitor drop**

| *Source switch ($S_n$)* | *Active capacitor* | *$V_{out}$ ($E_n$)* | *$V_{out}$ at load* |
|---|---|---|---|
| $S_1$ | $C_1$ | $V_{dc}$ - $5V_{dc}/6$ | $V_{dc}/6$ |
| $S_2$ | $C_1 + C_2$ | $V_{dc}$ - $4V_{dc}/6$ | $2V_{dc}/6$ |
| $S_3$ | $C_1 + C_2 + C_3$ | $V_{dc}$ - $3V_{dc}/6$ | $3V_{dc}/6$ |
| $S_4$ | $C_1 + C_2 + C_3 + C_4$ | $V_{dc}$ - $2V_{dc}/6$ | $4V_{dc}/6$ |
| $S_5$ | $C_1 + C_2 + C_3 + C_4 + C_5$ | $V_{dc}$ - $V_{dc}/6$ | $5V_{dc}/6$ |
| $S_6$ | $C_1 + C_2 + C_3 + C_4 + C_5 + C_6$ | $V_{dc} - 0$ | $V_{dc}$ |

is obtained across the load. Similarly, the source switch S6 is triggered alone, the net input voltage Vdc is obtained across the load. During the negative half cycle of the output IG2 and IG3 are closed. The polarity of the load is interchanged. The same operation is carried out to obtain the output across the load discussed in table 1.

The proposed TFSS is planned to trigger fit as a fiddle in order to imitate a predefined unadulterated sine reference wave or the lattice voltage. It is accomplished by legitimate activating of one source switch SN and either combine of the H Bridge switches (IGN) at the same time. A reference sine wave is characterized in light of the prerequisite (i.e., sufficiency and recurrence) at the lattice/load side. At that point the reference sine wave is isolated in number of time periods in view of the required number of yield level. The quantity of Time Frames per cycle of sine wave for the required m levels is 2 (m + 1). Here since we require 13 levels, the entire sine reference wave is isolated into 28 rise to outlines. The different modes of operation are appeared in figure 5.

## 4. RESULTS AND DISCUSSION

The estimating of the PV exhibit is measured for 75 V and 1KWp rating. In figure 6 the proposed topology is controlled by novel TFSS to produce exchanging beat for the 10 switches for 13 levels to top yields. The information dc join voltage of 220 V is relegated as the contribution to the inverter. The voltage is further dropped over the idle capacitors symmetrically. Consequently a voltage drop of 40 V is seen over every

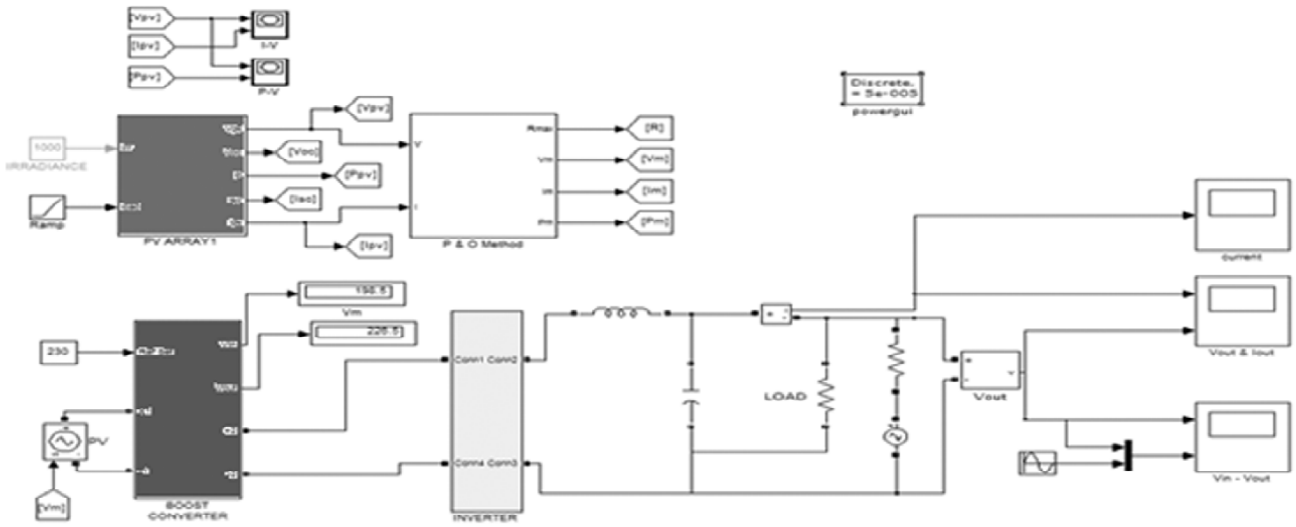


**Figure 5: Simulation for the proposed system**

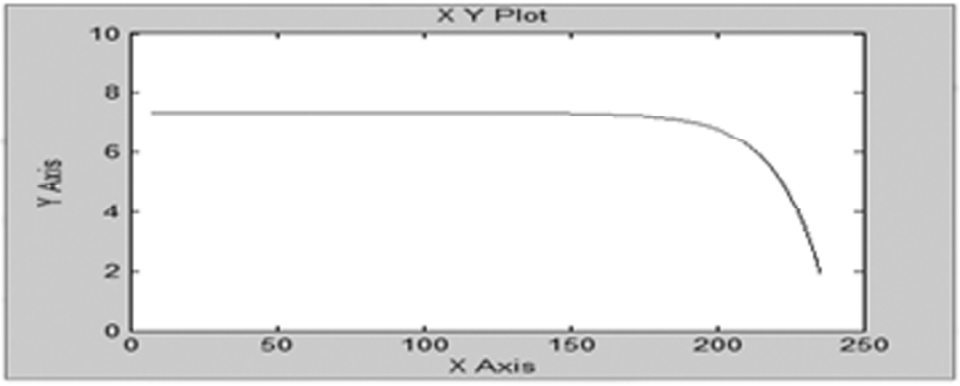


**Figure 6: Current Vs Voltage Curve**

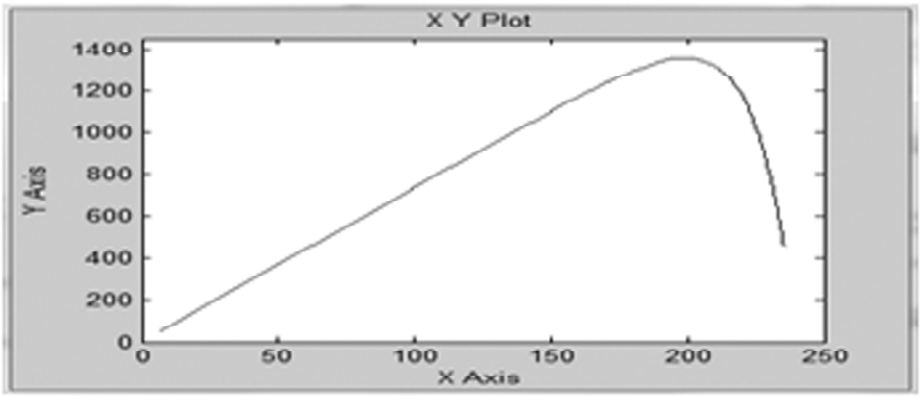


**Figure 7: Power Vs Voltage Curve**

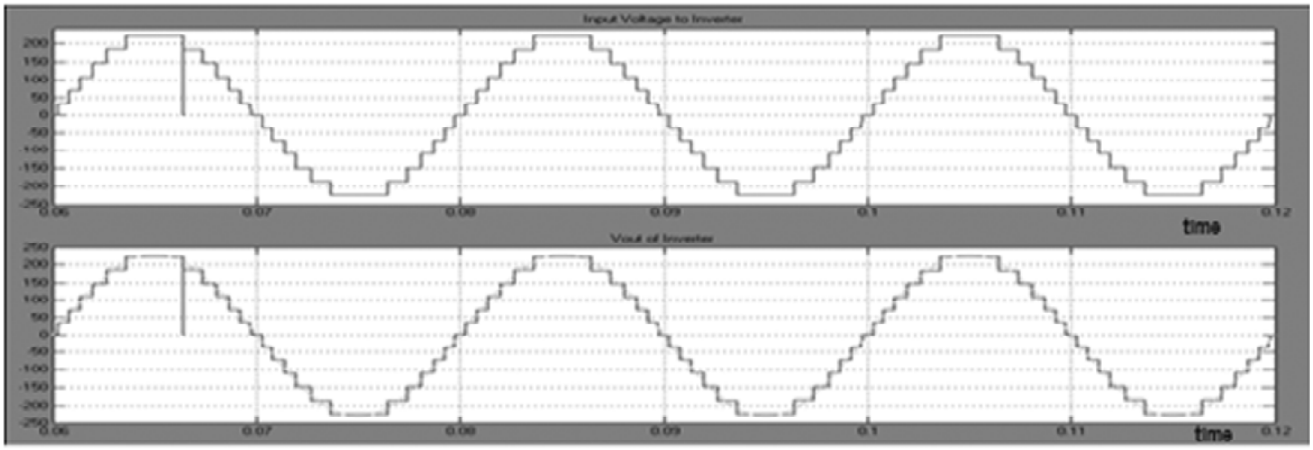


**Figure 8: Multilevel Inverter Stepped Waveform for 13 Level**

capacitor. To acquire 13 levels ventured yields the exchanging plan is isolated into 7 methods of operation for each quarter cycle. Tuning of the capacitor values and the modifying the terminating moment of the switches by receiving TFSS the symphonious substance can be lessened to a passable reach before sifting is further enhanced to 1.47% 13 level yield is 248 V, which is over the reasonable scope of 240V. The TFSS will now change the exchanging operation by diminishing the ventured yield from 13 to 11 levels. Thus the crest yield is presently 225 V which is underneath the passable scope of 240 V shown in figure 7.

During the mode 1 operation, since all the switches are left open, no voltage is created over the heap. The info voltage of 65 V is dropped over the inert capacitors C1–C6 by 65 V to acquire a resultant yield voltage of 0 V over the heap. In mode 2, the info voltage of 65 V is dropped over the dormant capacitors C2–C6 by 200 V to get a resultant yield voltage of 60 V. In mode 3, the information voltage of 65 V is dropped over the idle capacitors C3–C6 by 65 V to get a resultant yield voltage of 65 V. In mode 4, the info voltage of 240 V is dropped over the inert capacitors C4–C6 by 120 V to get a resultant yield voltage of 120 V. In mode 5, the info voltage of 240 V is dropped over the latent capacitors C5–C6 by 80 V to get a resultant yield voltage of 160 V. Thus in mode 6, the information voltage of 240 V is dropped over the idle capacitors C6 by 40 V to acquire a resultant yield voltage of 200 V. At long last in mode 7, the information voltage of 65 V is gotten as resultant yield voltage of 65 V over the heap. It was seen with legitimate tuning of the capacitor values and the altering the terminating moment of the switches by receiving TFSS the consonant substance can be lessened to a reasonable reach before sifting as appeared in figure 8. The sifted yield of current and voltage yield in the wake of separating, THD is further enhanced to 3.87% shown in figure 9.

The circumstance of voltage swell is confirmed by presenting a blunder voltage of +14 V and +28 V. The set voltage is 240 V which can endure up to +10% above which the circumstance of voltage swell

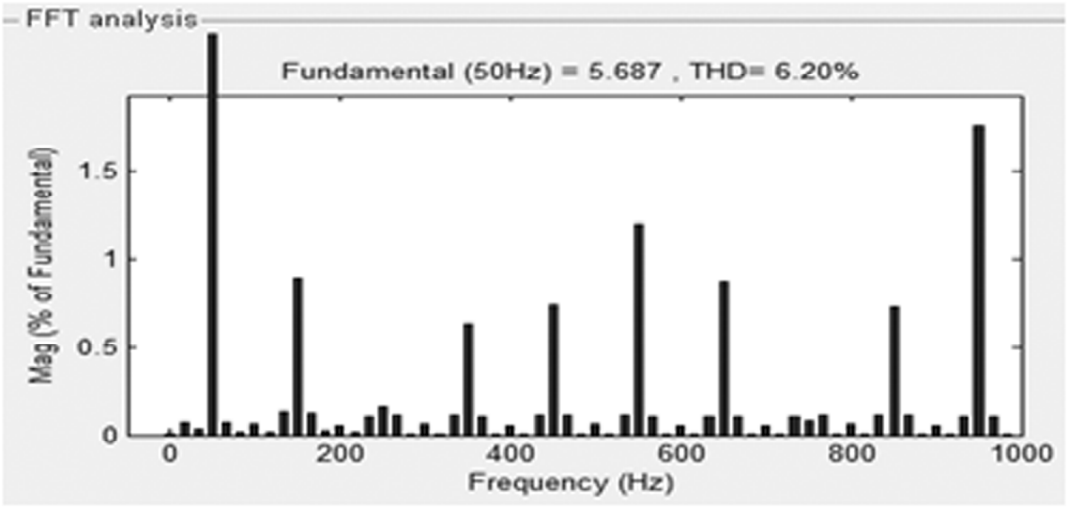


**Figure 9: FFT Analysis (Without Filter)**

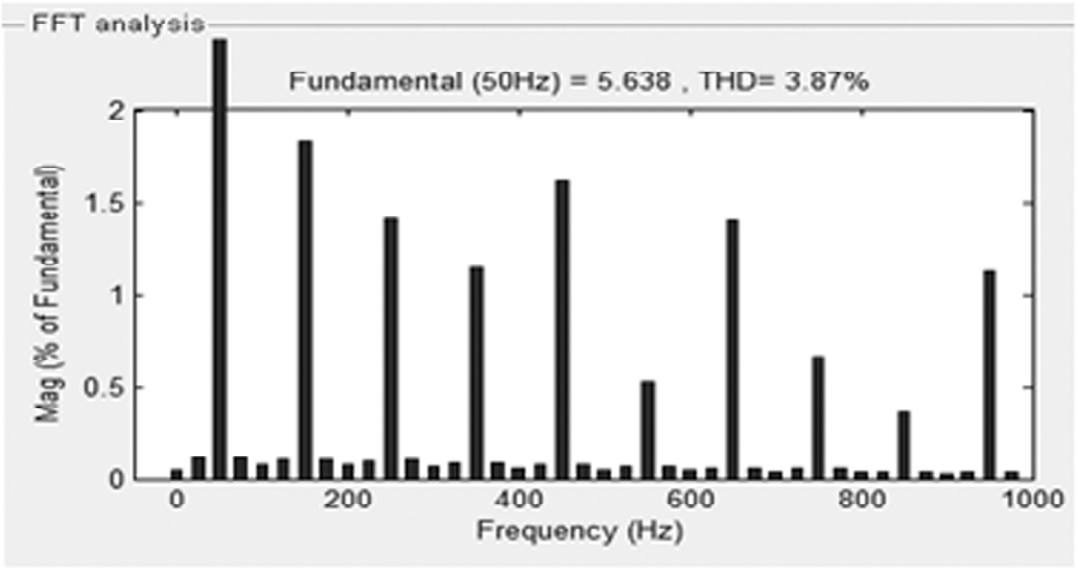


**Figure 10: FFT Analysis (With Filter)**

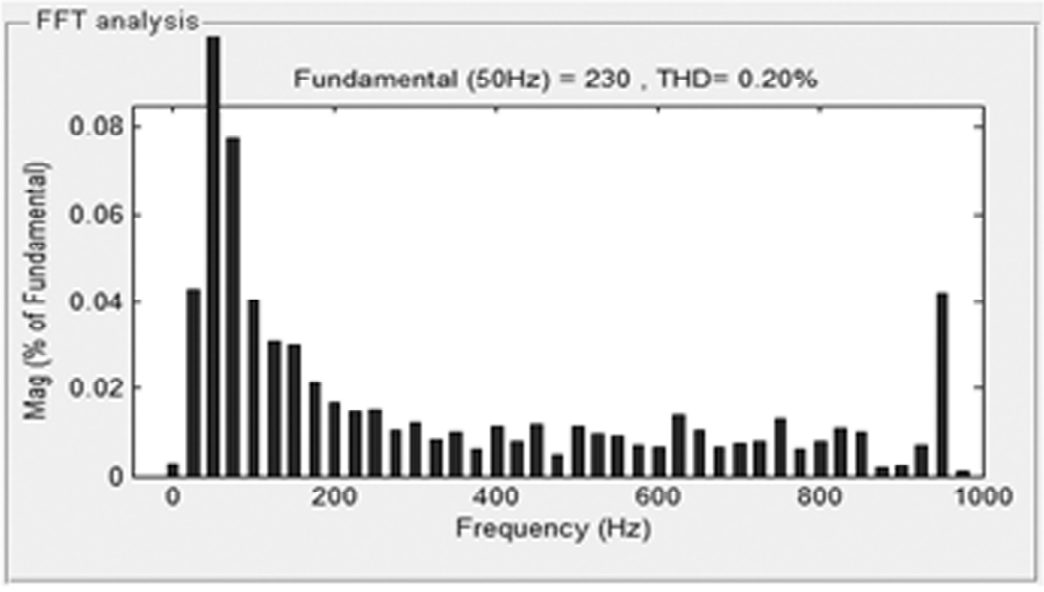


**Figure 11: FFT Analysis when connected to grid**

happens. At the point when the mistake voltage of +14 V, the top 13 level yield is 234 V, which is underneath the allowable scope of 240 V When the blunder voltage of +28 V is distinguished.

To confirm the outcomes by equipment model, the framework is worked at a voltage of 19 V. The 19 V information voltage is nourished from 75 WP photovoltaic board. The obligation cycle of the help converter is worked at 0–50%. The information 19 V is helped to 65 V. The help converter controlled through P&O MPPT calculation coded in dsPIC30F2010, and used to keep up the required 65 V voltage at the yield of the inverter s (470 µF, 25 V) MOSFETs are utilized as exchanging gadgets appeared in figure 10. The calculation for TFSS is ordered utilizing a microchip MP-LAB C30 programming and afterward kept in touch with the dsPIC30F2010 controller. The information dc join voltage is made to drop symmetrically over the 6 capacitors of each 10.83 V. The voltage drop over every capacitor and the matrix voltage is detected by voltage divider and changed over to advanced signs by simple to computerized converter (ADC). The inverter current and

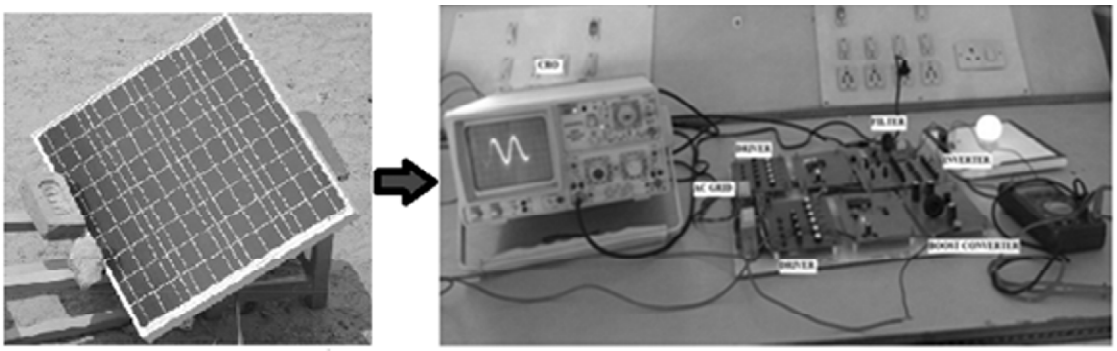

**Figure 12: Hardware implementation of the proposed grid connected inverter**

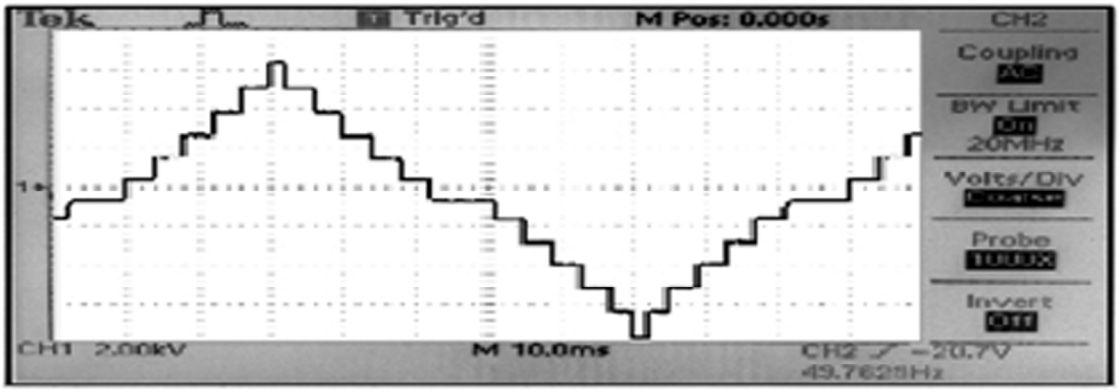


**Figure 13: The 13 level peak to peak inverter output voltage waveform without filter**

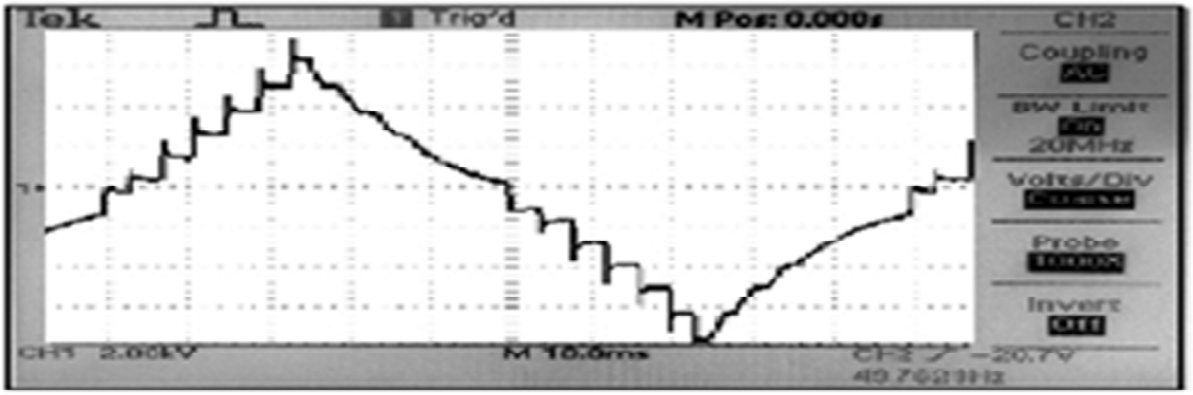


**Figure 14: The 13 level peak to peak inverter output voltage waveform with filter**

the matrix current are detected which is then sustained to the dsPIC30F2010 controller. The 240 V voltage from the network is downsized to 20 V utilizing a stage down transformer. The network reference voltage and the progression 13 level voltage yield from the inverter before sifting are thought about. The conditioner inverter yield and the framework working at 20 V are made to synchronize by going through a Zero Crossing Detector (ZCD). The inverter current and the lattice voltage are made in stage to guarantee solidarity power component. The THD measured for the proposed 13 level inverter yield computed preceding sifting is 6.20% shown in figure 11. The THD element for yield voltage waveform subsequent to sifting is 3.87% appeared in figure 12. The outcomes from the proposed GCI topology passes on that the execution of inverter is enhanced from ordinary topologies as far as exchanging misfortunes, consonant substance and low channel measuring.

## 5. CONCLUSION

The proposed topology acquires higher yield levels from a solitary dc source by considering required number of split capacitors. Higher the quantity of split capacitors less will be the bending of yield from an unadulterated sine wave. While assigning the time intervals by TFSS, significant duration for charging the split capacitors has to be assured prior to discharge of respective capacitors. The quantity of exchanging gadgets had decreased when contrasted and the traditional techniques. Extensive change in the consonant variable had decreased the extent of the detached channel. The consequence of the proposed Grid Connected Inverter (GCI) is confirmed by Matlab/Simulink reproduction and equipment usage.

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