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Center Boosted Sinusoidal Pulse Width Modulation for Three Phase Voltage Source Inverter

Sreeja P.* and L. Padma Suresh**

Abstract: This study deals with the performance analysis of Pulse Width Modulation (PWM) scheme for three phase voltage source inverter though amalgamating the boosted reference and random triangular carrier. The boosted reference is the addition of sine reference with injection of 1/3rd of reference amplitude ($3f_s$) in the middle portion of the reference wave. i.e (Π/3 to 2Π/3) and (4Π/3 to 5Π/3).. The proposed PWM scheme use two carriers, one is Triangle wave and another one is inverted Triangle wave. The arbitrary selection of these carriers is based on the linear feedback shift register value ('0' or '1'). This random carrier selection is serving to improve the spectral quality of the output of the inverter. Simulation results confirm the effectiveness of the proposed scheme in providing very less harmonic noises with minimum distortion and improved fundamental component. This study also shows the implementation compatibility of the work with Field Programmable Gate Array environment.

Key words: Harmonic spread factor, linear feedback shift register, pseudo random binary sequence, random pulse width modulation, voltage source inverter

1. INTRODUCTION

High power electronic devices are being used increasingly to control and facilitate the flow of electric power in modern industries. These devices are able to enhance the voltage profile, which impacts dynamic performance and stability of the system improved by the way of operating (ON and OFF) the devices[1]. One of such device is voltage source inverter that acts as a controlled voltage source, converting dc voltage to ac voltage with desired frequency, phase and magnitude. Figure 1 shows the schematic of two level VSI[2]. Pulse width modulation (PWM) is the inner control method of the inverter, which controls the output voltage efficiently. Sinusoidal PWM is a method, which decides the ON and OFF period of the switches by comparing sinusoidal reference and triangular carrier[3]-[10]. Basically, the PWM methods can be classified into two groups, (i) By changing the reference waveform and (ii) Changing the carrier waveform. Discontinuous PWM is a method, which under first group whose reference shape is not pure sinusoidal which aids improve the fundamental and at the same time this will decrease the harmonic spreading effect of the inverter output. The major accumulation of the harmonics are present at the multiples of the switching frequency (fs,2fs,3fs….), which decides the acoustic noise of the induction motor. By changing the shape of the carrier waveform randomly these harmonics can be spread in the voltage band. But this method slightly decreases the fundamental which will affect the performance in the modern drives[4]. In this paper it proposes the new methods which will increase the fundamental as well as harmonic spreading effect. The reference waveform of the method can be changed by adding the regular sine wave shape with the inverse third order harmonic in the centered 60°. i.e (Π/3 to 2Π/3) and (4Π/3 to 5Π/3). Random pulse width modulation has been investigated so far, for providing less acoustic noise of the motor[5]. The triangle and the inverse triangle have been used randomly as a carrier which is generally called random

* Research Scholar Noorul Islam University, *Email: sreejathambi0@gmail.com*

** Professor & Head Electrical and Electronics Engineering Noorul Islam University, *Email: suresh_lps@yahoo.co.in*

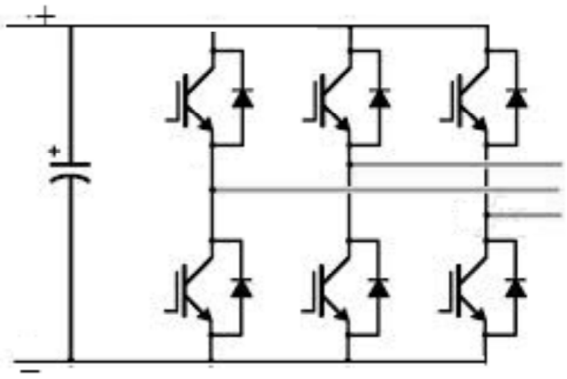

Figure 1: Two Level Voltage Source Inverter

pulse width modulation (RPWM). The selection of the triangle is based on the linear feedback shift register (LFSR) output.

Field programmable gate arrays (FPGAs) are a special class of ASICs which differ from mask-programmed gate arrays in that their programming is done by end users at their site with no IC masking steps[7][9]. The complete proposed pulse generation method has been designed by using very high speed hardware description language (VHDL) for FPGA and simulated by using Modelsim. And these pulses has been sent to MATLAB environment by using co-simulation methodology and verified by using three phase inverter. The simulation results are compared with the existing (i) SPWM (ii) sine reference-random carrier (iii) center boosted reference with single triangle.

2. PROPOSED METHOD

In the Proposed Method Both Reference and Carriers are Modified Compare Regular SPWM.

2.1 Reference Waveform Generation

The reference of any sinusoidal PWM is based on the equation0020

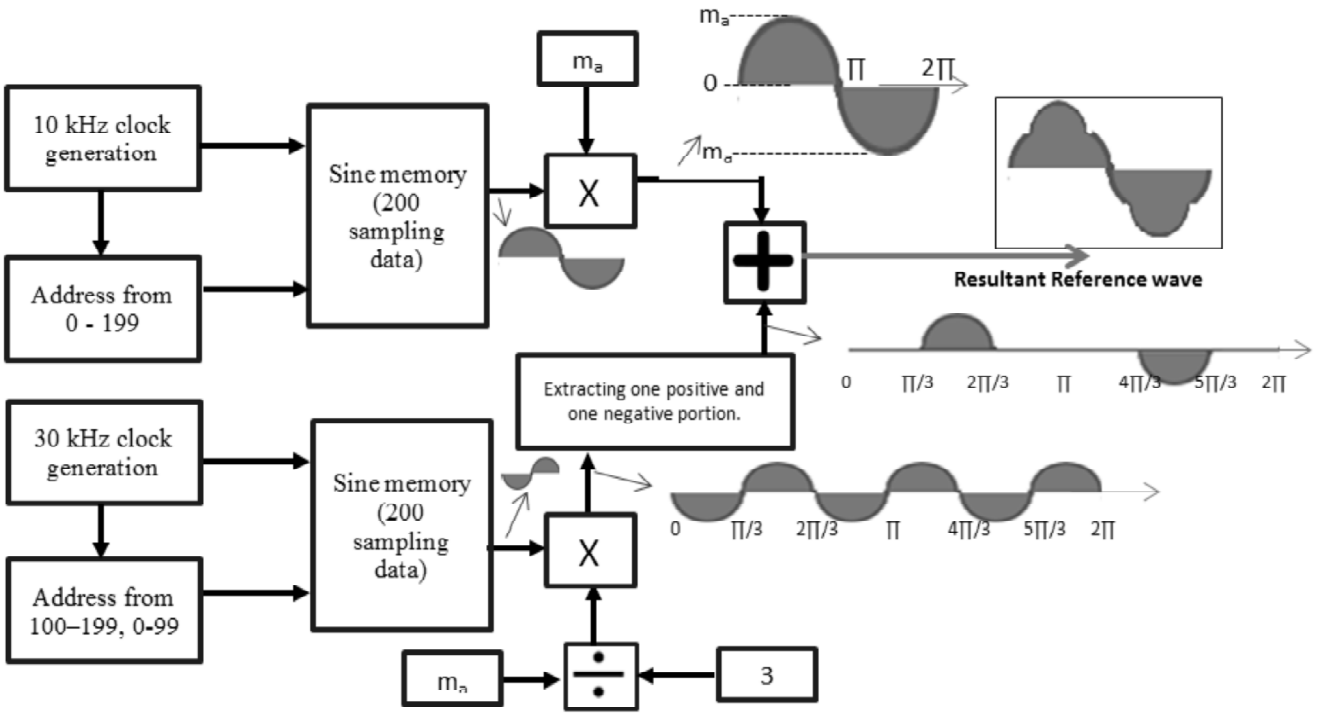

Figure 2: Proposed Method Reference Waveform Generation

$$V_{ref} = m_a \sin \alpha \quad (1)$$

m_a-> modulation index .It is the ratio of reference voltage to the triangle carrier voltage.α-> angle varies from 0° to 2Π. In the proposed method the reference waveform has been modified based on the equation (2)

$$V_{ref} = m_a \sin \alpha \text{ for } 0°<\alpha<\Pi/3,\ 2\Pi/3<\alpha<4\Pi/3,\ 5\Pi/3<\alpha<2\Pi$$
$$V_{ref} = m_a \sin \alpha + (ma/3 \text{ x } \sin 3\alpha) \text{ for } \Pi/3<\alpha<2\Pi/3,\ 4\Pi/3<\alpha<5\Pi/3- \quad (2)$$

In the FPGA based digital environment, reference waveform has been generated based on the above equation which is shown in figure 2. The reference design consists of 1. Address generation modules 2. Sine wave generation module 3. 10 kHz clock generation module and 4.summer and multiplier components. In the first address generation module have a up counter starting from 0 to 199.In the second address generation module have a same type of up counter but starting address from 100,101….199,0,1……The first one is used to generate the address for 50 Hz sine wave generation and second one is used to generate 150 Hz generation. These modules receive the clock signal 10 kHz and 30 kHz from the clock generators. Clock generator is a clock divider which is used to convert 50 MHz into 10kHz

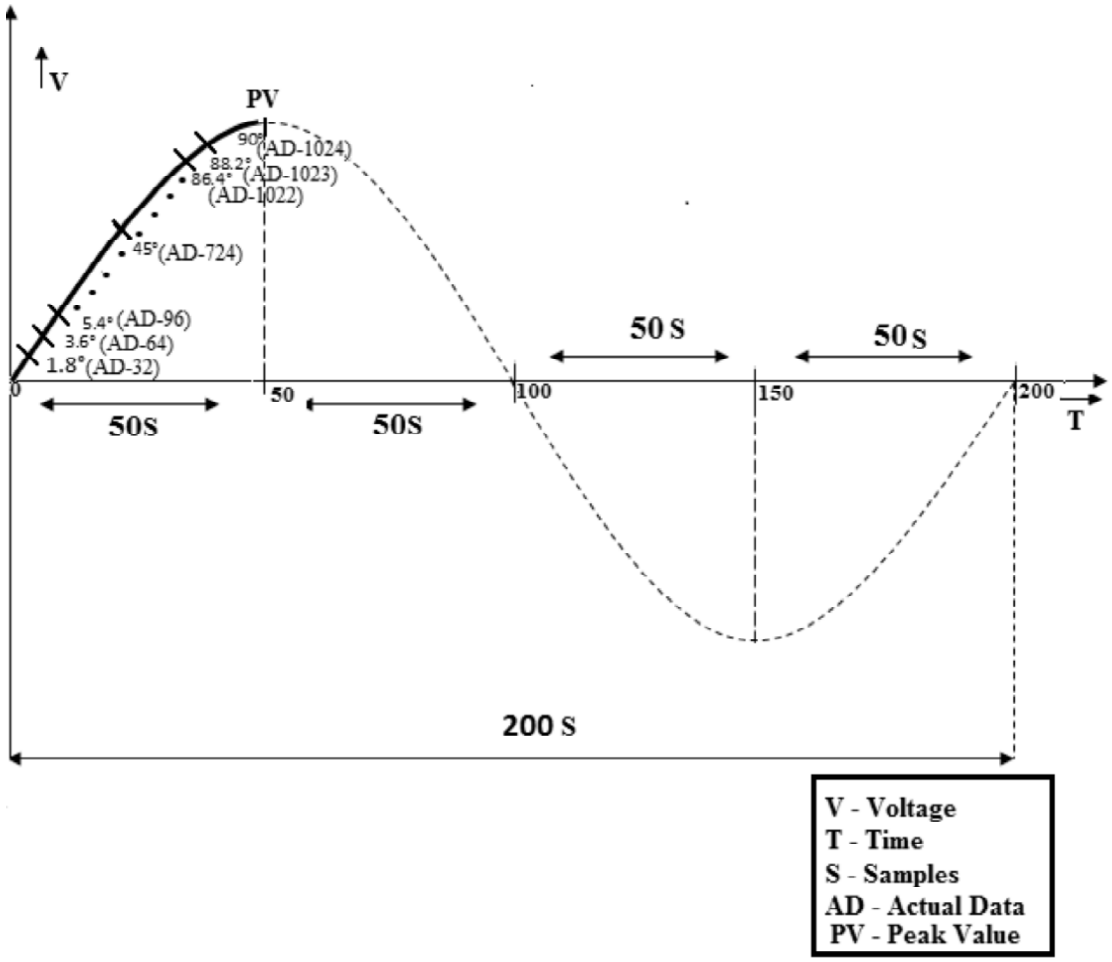

Figure 3: Sine Wave Sampling representation

and 30 kHz clock signals. The method to generate the sine samples is shown in figure 3. which illustrates clearly. The output of the sine generation modules depicts in figure 2. With the advantage of FPGA programming both sine waves (50 Hz, 150 Hz) **are** generated parallel. The 150 Hz sine wave is like 3rd order harmonics but shifted by 180°.Two multipliers has been used **to** involve with the modulation index which will decide the pulse width variation in the complete cycle, one summer has been used to add both sine waves. The resultant sine wave clearly depicts in figure 2.

The sine wave sampling has been taken as per figure 3. Total samples for a cycle is 200. So that sampling duration is 360°/200, which will give 1.8°. The 10 kHz and 30 kHz clock signal has been used to sample the 50 Hz sine data and 150 Hz sine data.

2.2. Carrier Waveform Generation

In this method two carriers have been used, one is triangle wave and another one is inverted triangle but both are having same fixed 5 kHz frequency. In the digital implementation, it is basically the up down counter whose maximum value is equal to the V_a. The selection of winning triangle is based on LFSR based pseudo random binary sequence (PRBS). The LFSR is an 8 bit register which is used to select the winning triangle. The LFSR output is based on the two XOR gate operations. The winning triangle is going to compare with the modified sine wave.

2×1 multiplexer is used for selecting resultant winning triangle. If the PRBS value '1' then resultant winning carrier will be regular triangle, otherwise inverted triangle will be the winning triangle, which is shown in figure 4.

In order to obtain the real time random number generators that offer good randomness, computer search has been conducted for the logical RPWM schemes. The probability density function is used to examine the quality of randomness. The 8 bit,10 bit and 12 bit LFSRs are investigated so for [11].

3. SIMULATION RESULTS AND DISCUSSION

The performance parameters are verified by the simulation software's. The performance parameters are fundamental component, total harmonic distortion (THD) and harmonic spread effect (HSF). The modulation

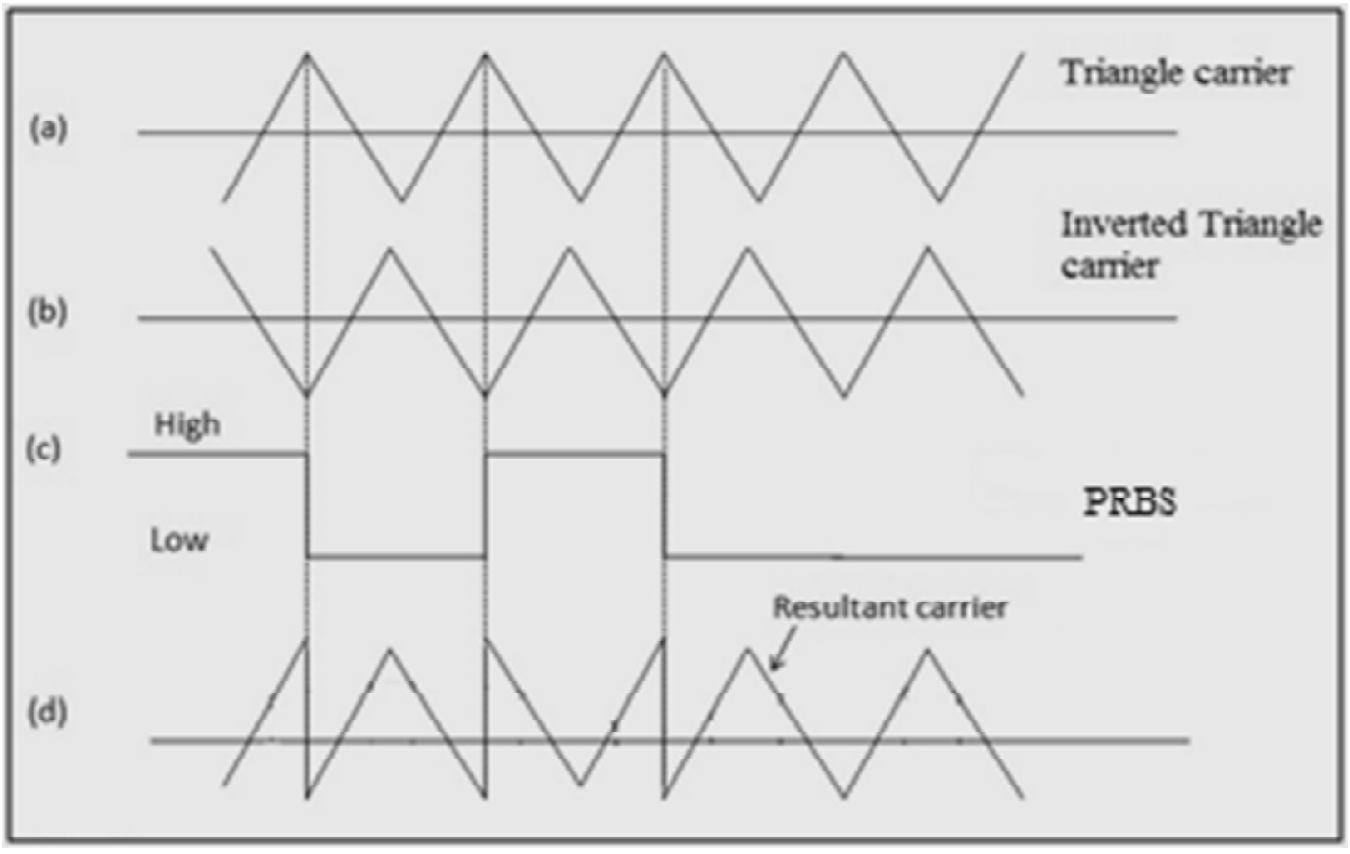

Figure 4: Carrier Generation

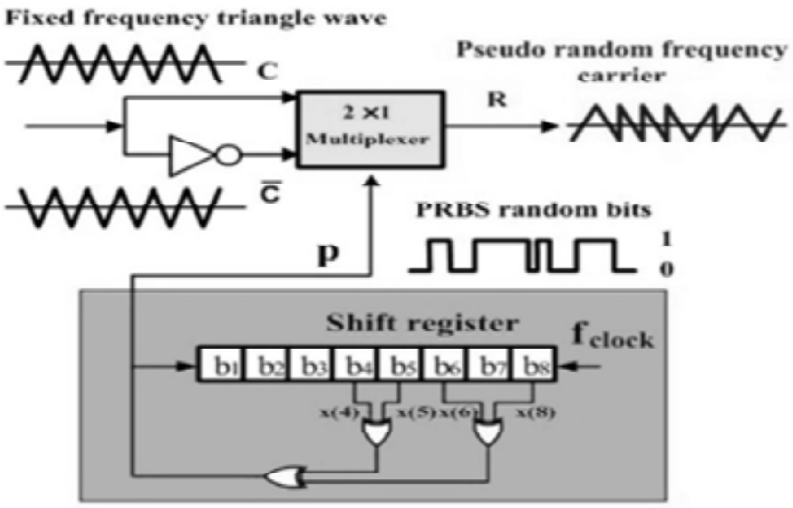

Figure 5: PRBS Generation

index, M_a is defined as a ratio between amplitude of the reference (sine) wave to the amplitude of the carrier (triangular) wave.

$$Ma = V_{sin}/V_{tri} \tag{3}$$

The distortion of voltage/current waveforms can be quantified using total harmonic distortion (THD) and give as

$$THD = \sqrt{\frac{V^2_{2(rms)} + V^2_{3(rms)} + ... + V^2_{n(rms)}}{V^2_{1(rms)}}} \tag{4}$$

Where, V_1 is the rms value of fundamental component of the output voltage of the V_1, V_2, V_3,... are the rms values of second, third,... harmonics.

Another performance parameter, harmonic spread factor is a simple quality indicator would be useful for evaluating the harmonic spread effect of the random PWM scheme. The factor is named as harmonic spread factor (HSF) and uses the concept of statistical deviation. The HSF [12-13] is defined as follows:

$$HSF = \sqrt{\frac{1}{N-1}\sum_{j>1}^{N}\left(H_j - H_0\right)^2} \tag{5}$$

$$H_0 = \sum_{j>1}^{N}(H_j)/(N-1) \tag{6}$$

Where,'H_j' is amplitude of jth harmonics, 'H_0' is average value of all 'N-1' harmonics. The HSF quantifies the harmonic spectra spread effect of any PWM scheme and it should be small. For ideally flat spectra of white noise, the HSF would be zero.

In this work, followed combined simulation between two software. 1.Modelsim, which is used to generate the PWM pulses for three phase inverter. 2. Matlab7.10, which is used to analyze the line to line voltage harmonics, THD and harmonic spread effects.

The simulation results of harmonic spectrum for existing methods with proposed method for 0.8 modulation index as shown in Figure 6, 7, 8, 9. Figure 10 specifies the line to line voltage of the proposed method.

The simulation results of proposed sine reference wave as shown in Figure 11, derived from digital simulation method by using Modelsim6.3f. The random triangle carrier is simulated and shown in Figure 12.The triangle frequency is 5 kHz. Figure 13 shows the proposed PWM pulses for three phase inverter.

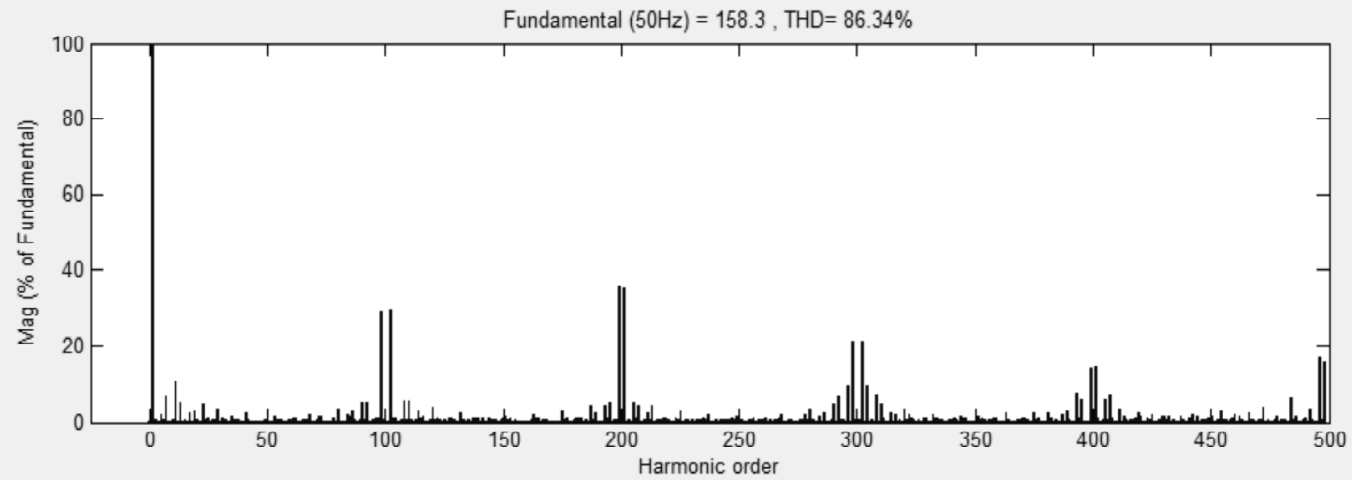

Figure 6: Harmonic Spectrum for SPWM

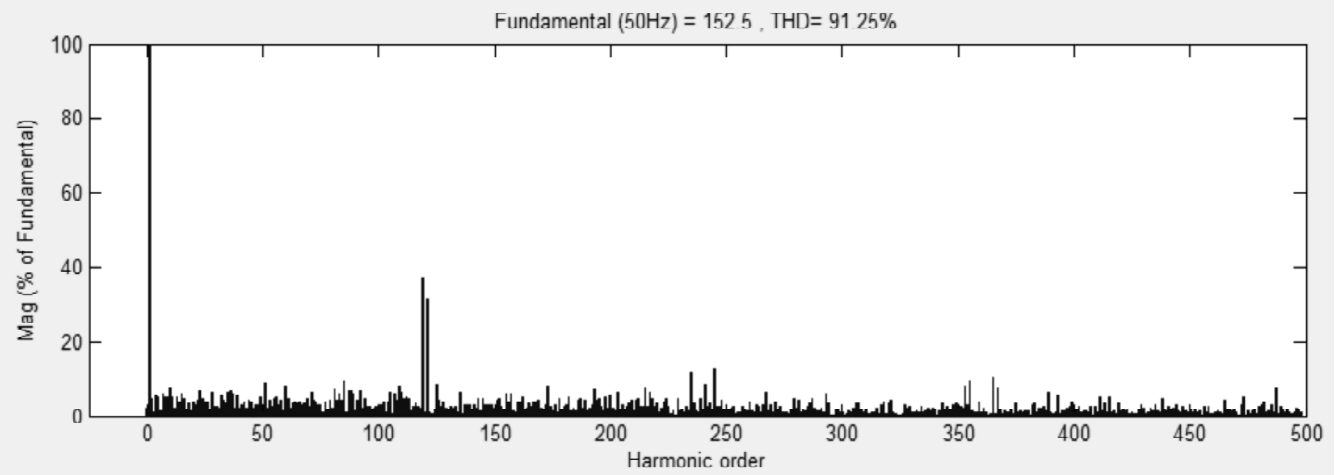

Figure 7: Harmonics Spectrum for Sine Reference with Random Triangle

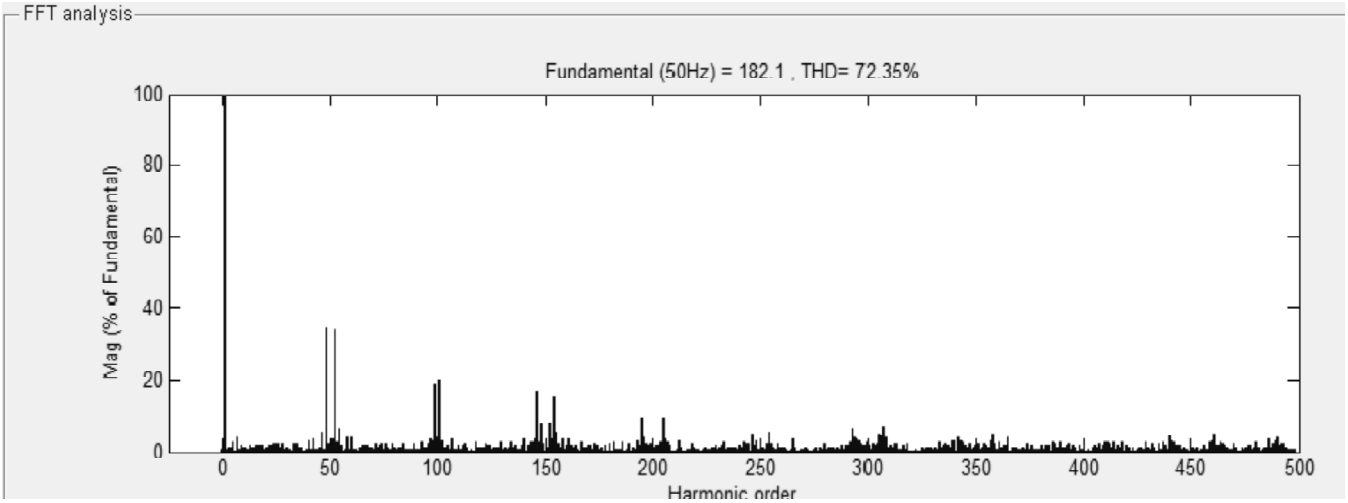

Figure 8: Harmonic Spectrum for Boosted Reference with Single Triangle

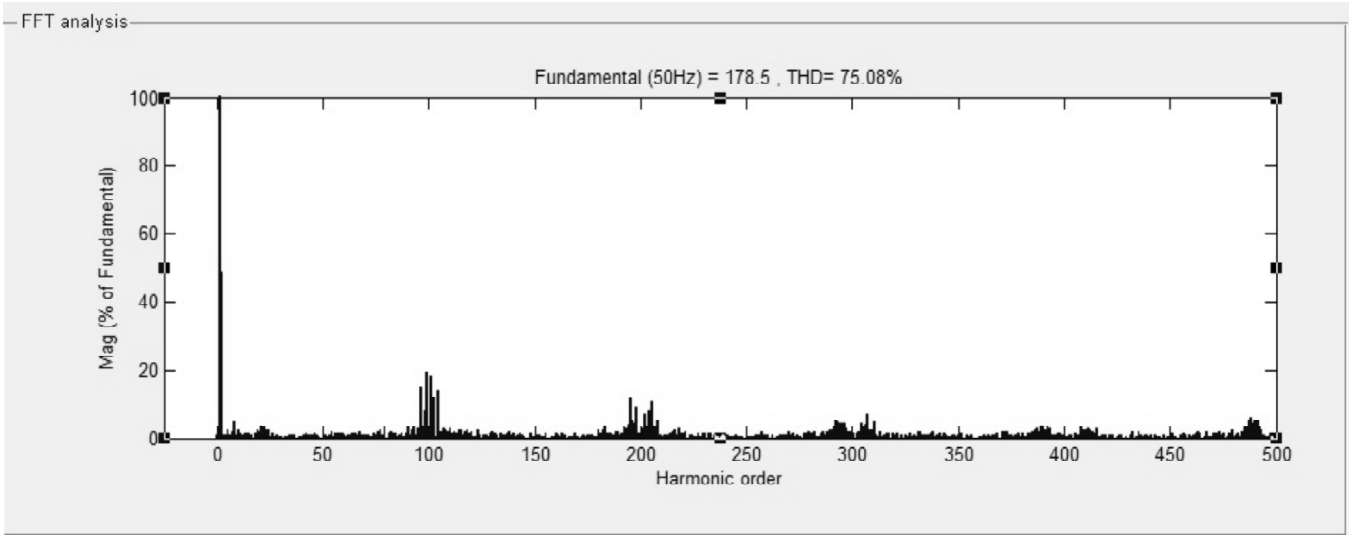

Figure 9: Harmonics Spectrum for Proposed Method

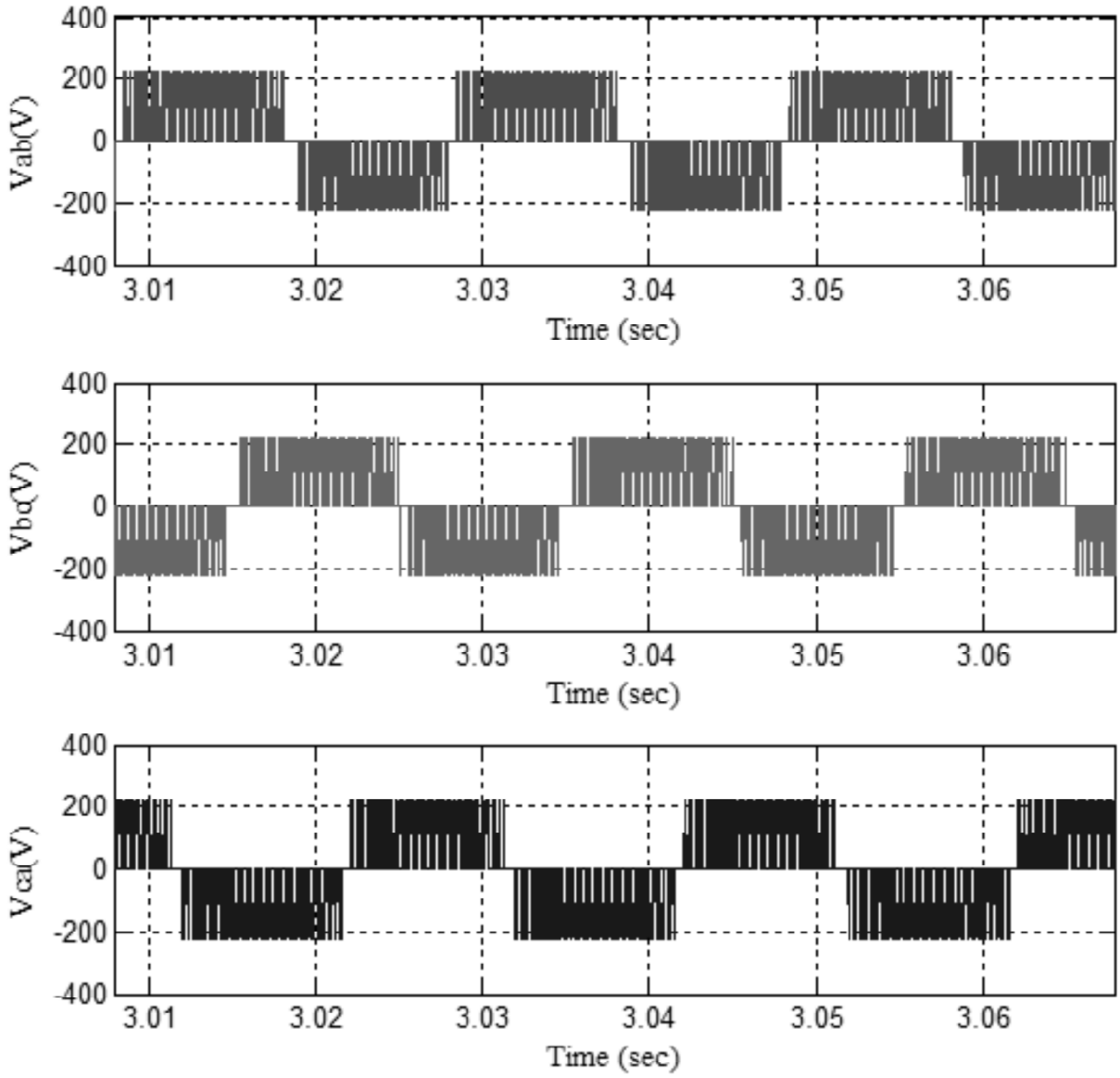

Figure 10: Line to Line Voltage of the Proposed Method for the Modulation Index 0.8

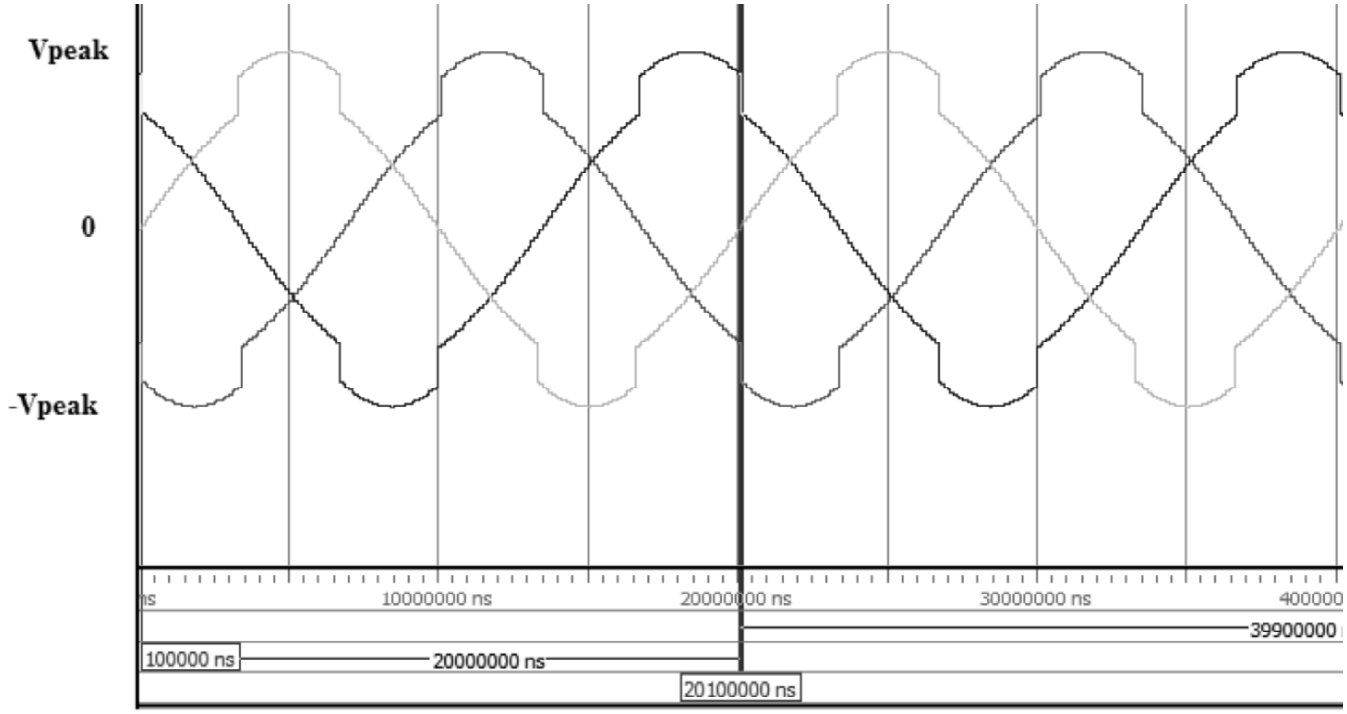

Figure 11: Reference Waveform Generation-Modelsim Environment

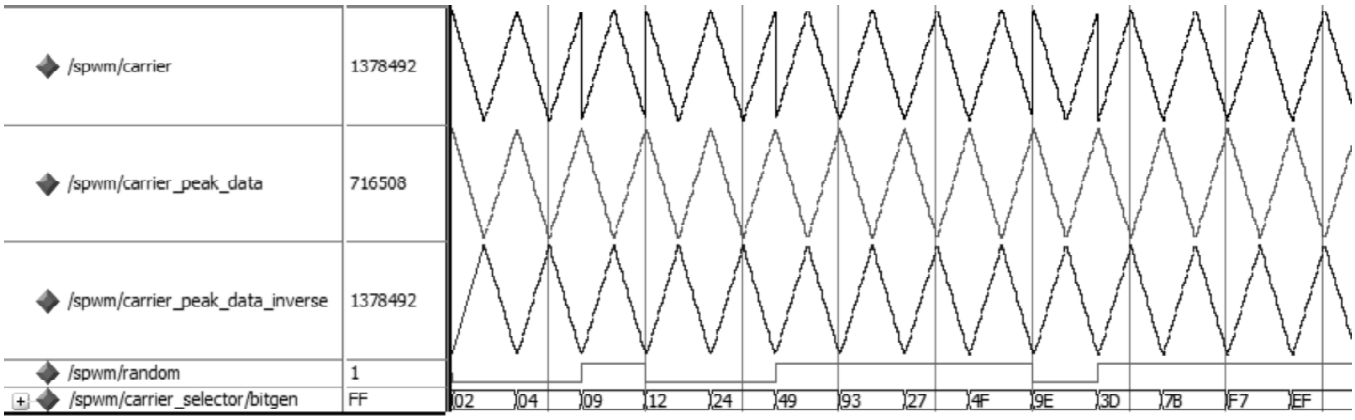

Figure 12: Random Triangle Carrier Output (5 kHz)

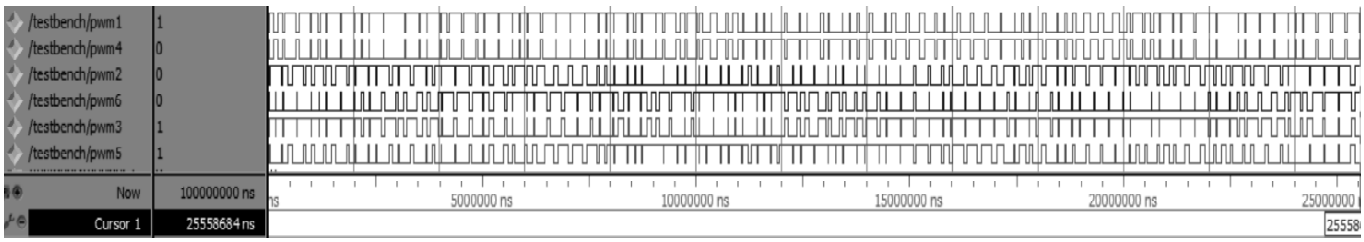

Figure 13: Pulse Generation for Three Phase Inverter

From the simulation results, while comparing the SPWM with Random triangle method fundamental voltages are more for all modulation index but spreading capability i.e HSF is also more in SPWM, it implies, acoustic noise of the induction motor will be more in SPWM but less in Random triangle. While comparing SPWM with boosted reference SPWM, the fundamentals are more in boosted, but boosted reference PWM will give more acoustic noise. From the first three existing methods results showing that acoustic noise is less in random triangle and fundamental is more in boosted reference. In the proposed

Table 1
Comparison of existing and proposed method

Modulation Index	*Performance Parameters*	*SPWM*	*sine reference + Random triangle*	*Boosted Reference+ single Triangle*	*Boosted reference+ Random triangle*
	Fundamental	38.18	38.86	49.27	48.58
0.2	THD	254.93	249.57	207.36	220.57
	HSF	9.897617	8.2	8.250875	8.457998388
	Fundamental	78.04	75.87	91.51	92.46
0.4	THD	160.92	163.22	144.06	141.48
	HSF	6.355232	5.4	5.823541	5.569945262
	Fundamental	114.1	111	134.7	138.4
0.6	THD	120.49	123.49	102.09	100.05
	HSF	4.787056	3.7025	3.998662	3.892589785
	Fundamental	158.3	152.5	182.1	178.5
0.8	THD	86.34	92.15	72.35	75.08
	HSF	3.491573	2.6058	2.896567	2.781722216
	Fundamental	192.4	190.2	193.8	198.1
1	THD	67.3	68.43	66.18	64.09
	HSF	2.520655	2.4058	2.583066	2.503836162
	Fundamental	211.2	209.8	207.6	213
1.2	THD	57.97	58.04	59.66	57.12
	HSF	2.249542	2.2583	2.300457	2.202508629

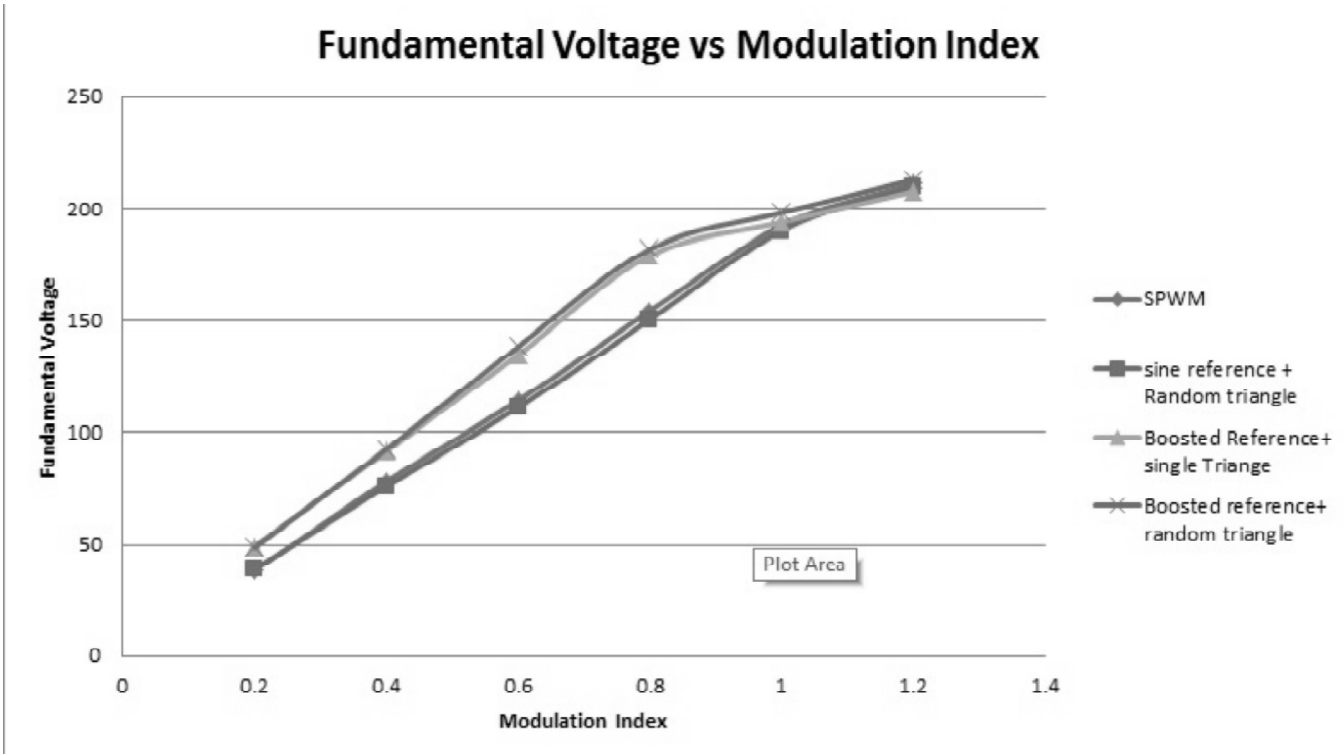

Figure 14: Pictorial Representation of Fundamental Voltage Comparison

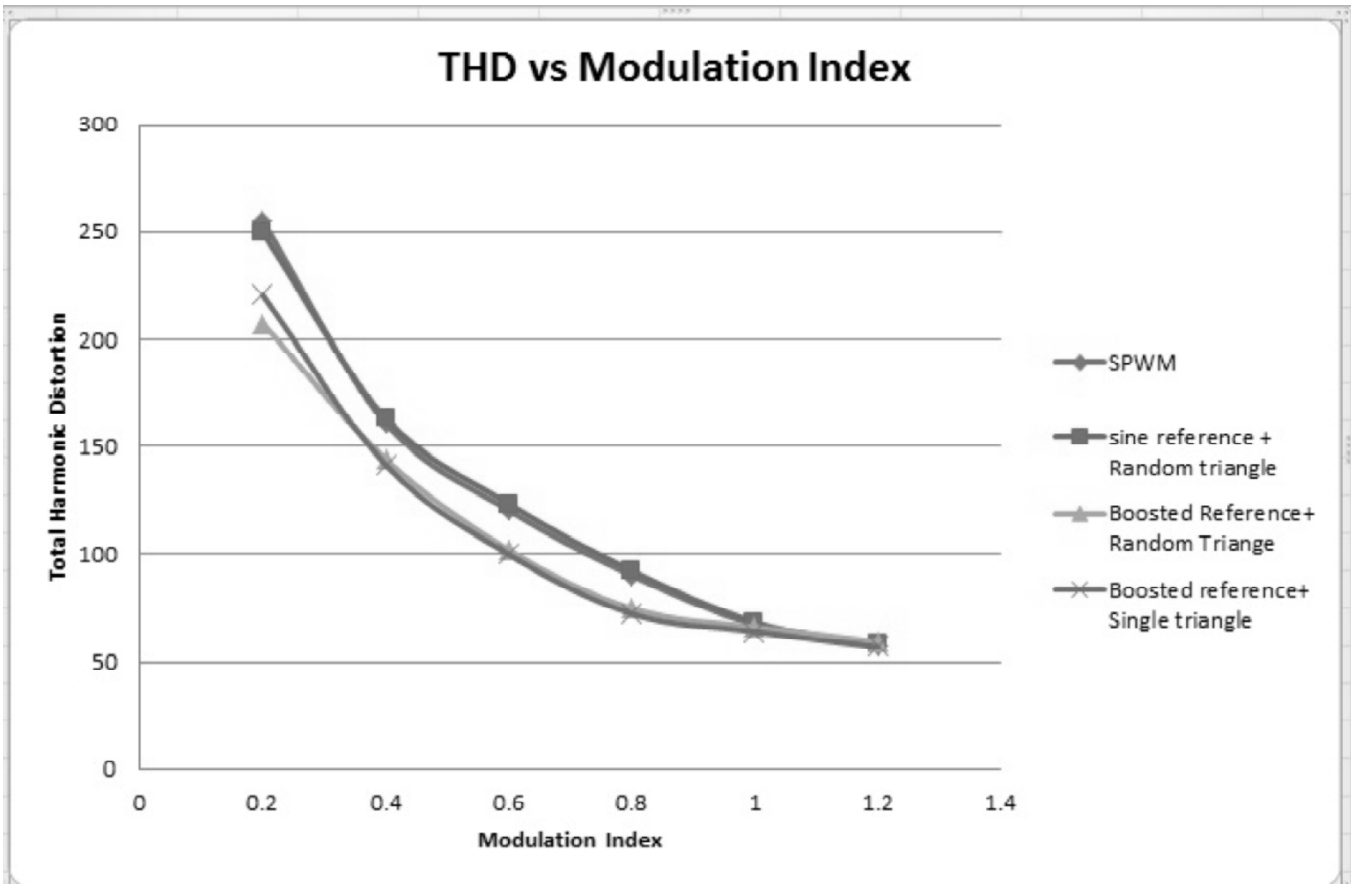

Figure 15: Pictorial Representation of THD Comparison

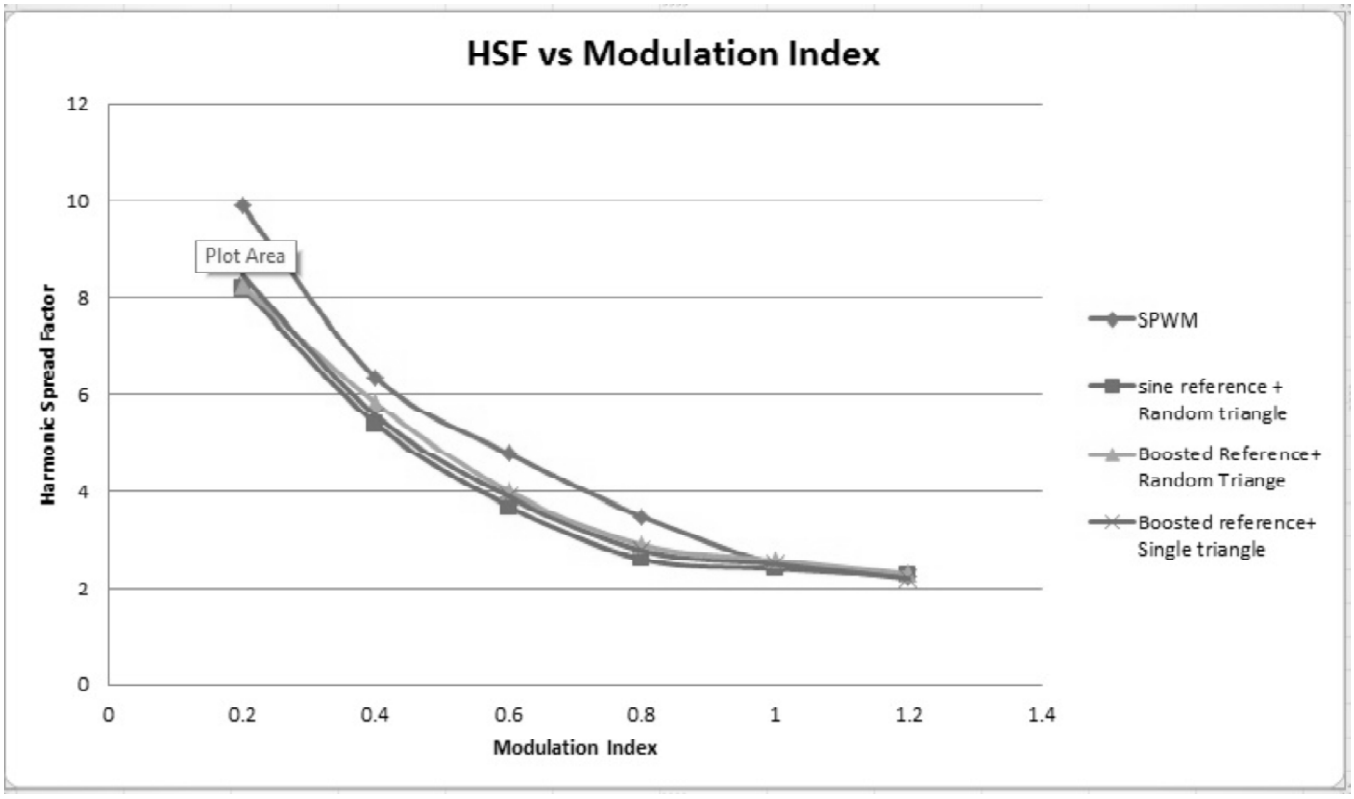

Figure 16: Pictorial Representation of HSF Comparison

method i.e intermingling of both advantages will give much better results which are shown in table 1. Figure 14 compares the fundamental voltage of all the methods. Figure 15 compares the THD of all the methods. In the over modulation region all the methods are giving the same fundamental voltage and same THD. Interestingly HSF also follows the same path as over modulation region gave the lowest value for all the methods.

4. HARDWARE IMPLEMENTATION

The scheme has been designed by using VHDL language for FPGA device environment. Modelsim based digital simulation results of carrier and reference wave generation are shown in Fig.11 and Fig.12 resultant RPWM pulses are shown in Fig.13 with Ma = 0.8 and fs = 5 kHz. This has been synthesized by using Xilinx13.1 project navigator tool.XC3S500E FG320-4, 90 nm technology FPGA device has been selected for synthesis.

Interestingly, this multiple carrier PWM digital work has occupied only 28 % of the slices of FPGA resources. 6 DSP based multipliers have been used to generate the Proposed PWM shown in table.2. 50 MHz clock oscillator has been used for sequential circuits. A Xilinx power estimator tool is used to estimate power analysis. Device static power or quiescent power is a function of process voltage and temperature. In this work, static power dissipation is 78 mW. Dynamic power dissipation is 40mW. Total power dissipated by FPGA device is 118 mW. In the hardware exploitation YOKOGAWA digital storage oscilloscope has been used. The complete setup consists of three phase voltage source inverter, FPGA, 3 Φ Induction motor and DSO. In Figure 17 and Figure 18, shows the line to line voltage of the inverter output voltage and phase voltage/current respectively for 0.8 Modulation index has been used, V_{dc}=415 V

Table 2
Utilization of Proposed Method in FPGA

	Device Utilization Summary (estimated values)		
Logic Utilization	Used	Available	Utilization
Number of Slices	1211	4656	26%
Number of Slice Flip Flops	783	9312	8%
Number of 4 input LUTs	2315	9312	24%
Number of bonded IOBs	8	232	4%
Number of MULT18X18SIOs	6	20	30%
Number of GCLKs	4	24	16%
Timing Summary:Speed Grade:-4 Minimum period: 15.980ns (Maximum Frequency: 62.578MHz) Minimum input arrival time before clock: 7.059ns Maximum output required time after clock: 4.283ns = Process “Synthesize-XST” completed successfully			

5. CONCLUSION

The Center Boosted Sinusoidal Pulse Width Modulation with randomization capability method is presented. This digital control pulse generation scheme is simple to design and implemented by FPGA device for three phase VSI. Figure 14, 15 and 16, shows that the critical performance comparison with conventional schemes. Table.1, clearly depicts that the significant reduction of the harmonic spread factor which decides the acoustic noise of the motor for the Modulation index with the satisfactory performance reduction of fundamental and total harmonic distortion. This scheme is applicable in industries to provide the noiseless

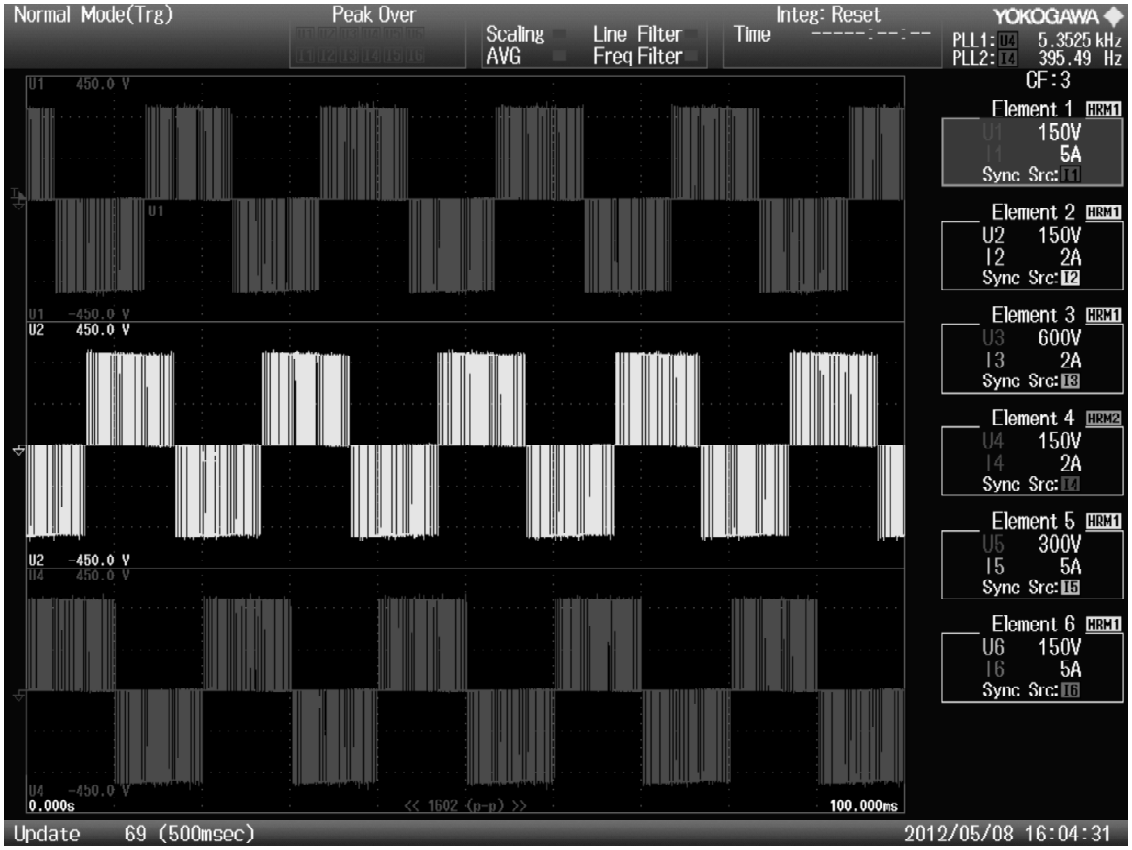

Figure 17: Line to Line Voltage of 0.8 Modulation Index, V_{dc}=415

V.

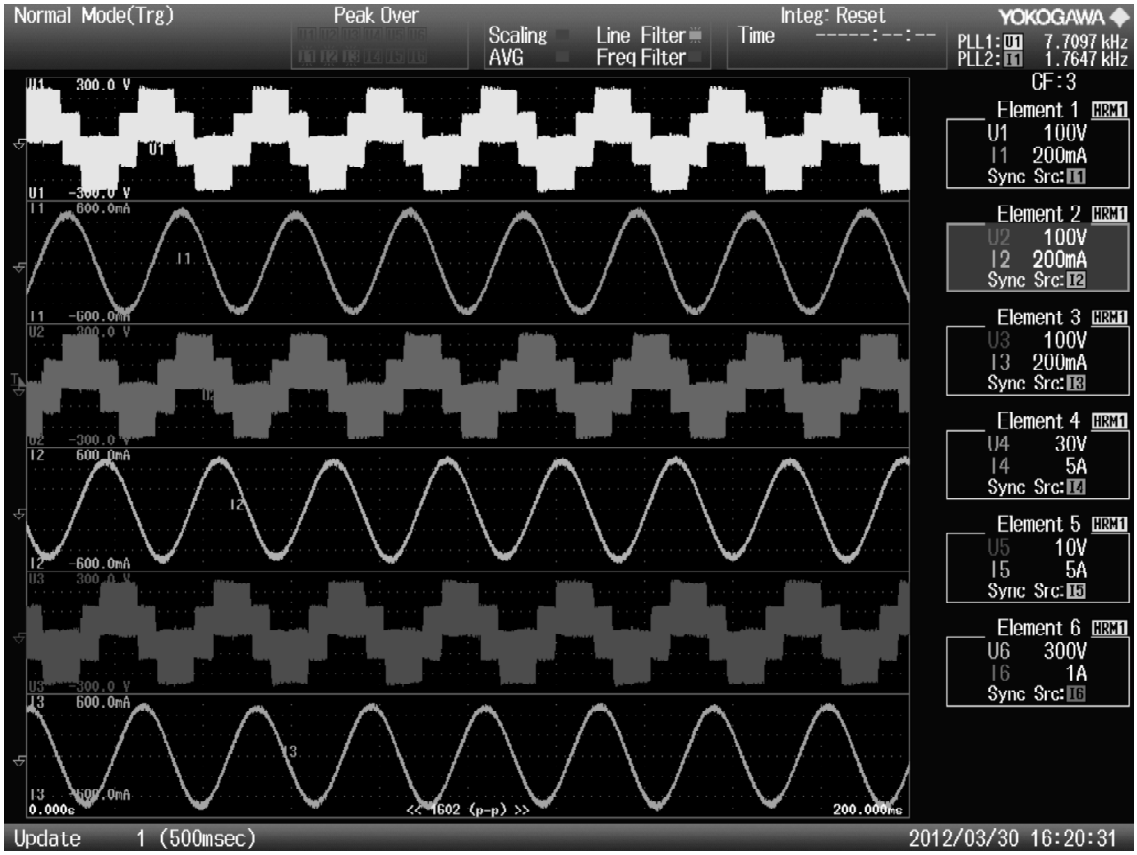

Figure 18: Phase to Neutral Voltage and Current Waveform of 0.8 Modulation Index, V_{dc}=415 V

environment. This scheme is also well adopted with FPGA based digital environment which utilize less area, better speed and reduced power dissipation. The hardware results of line to line voltage and phase voltages are evidenced as shown in Figure 17 and 18.

Appendix

MATLAB Simulation-INDUCTION MOTOR SPECFICATION

Power	3 HP
Line-Line Voltage	220 V
Frequency	220 V
Rs	.435 Ω
Ls	.002 H
Rr'	0.816 Ω
Lr'	0.002 H
Inertia J	.089 Kgm^2
Friction factor	0.005 Nms
Pole Pairs	2

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