I J C T A, 9(34) 2016, pp. 779-785

An Novel Design & Analysis of Low Power DTC in TDC for PII Based Applications Using Finfet & GNRFET in 16nm Technology

[1]S. Ranjith, [2]T. R. Chenthil and [3]G. C. Jagan

ABSTRACT

Nowadays most of the electronic components have been increased. This tends to power dissipation and the power supply provided to the electrical and electronic circuits are not fully utilized. In larger circuits, Propagation delay is the major reason for power dissipation. The work focuses on ultra-low-power and highly integrated implementations of ADCs, in complementary metal-oxide-semiconductor (CMOS) very large scale integrated(VLSI) circuit fabrication technologies. In particular, for data conversion time-based techniques, can potentially achieve significant reductions in power consumption of ADC architectures. Today, digital signal processors (DSP) and digital integrated circuits(DIC) are taking advantage of technology scaling to significant improvements in power, speed, and cost. simultaneously technology scaling reduces supply voltage and intrinsic transistor gain leads to two new broad trends in ADC research. Initial approach is the emergence of digitally assisted analog design, which emphasizes the relaxation of analog domain precision and the recovering accuracy in the digital domain. Latter trend is the representation of signals, and the processing of signals, in the time domain. Low power, small analog-to-digital converters (ADCs) have numerous applications in areas ranging from power-aware wireless sensing nodes for environmental monitoring to biomedical monitoring devices in point-of-care (PoC) instruments. Various performance metrics have been tested and estimated by implementing in FINFET and GNRFET in 16nm technology using Tanner EDA tool.

Keywords: analog-to-digital converters, power dissipation, gnrfet, phase locked loop

1. INTRODUCTION

In many electronic components Analog to digital converters (ADC) are key components which has been used. Today's integrated circuits (ICs) are likely to use mixed-signal (i.e., a combination of analog and digital) circuits, consisting of a digital signal processor (DSP) core which has input interfaces to the external analog signals through ADCs. The inflation in hand-held and battery-operated electronic systems is making designers to look for ADC architectures which ensuras lower power consumption and are more cost-efficient. The starting point of the research presented in this thesis is to identify the limiting features of today's conventional technologies, and explore alternative architectures which address and potentially overcome these shortcomings. Increasingly, many experiments and measurements require signal digitization of a large number of parallel channels for storage and analysis. Examples can be found in applications such as high energy physics, spectroscopy, medical imaging, radiation sensors, and environmental sensors [3]. Due to the large number of channels in these applications, power consumption and the die area of the ADC per channel should be as small as possible. The motivation of the research is the implementation of a multichannel ADC for a wireless sensor,here ADC operates in a sensor node which sends data to a central node where data is processed. Since the sensor is battery-operated, the ADC needs to be extremely power efficient.

[1,2,3] AssistantProfessor,Department of Electronics and Communication, JEPPIAAR Engineering College, Chennai, Tamilnadu, India

2. EXISTING DTCOMPARATOR

The need for low-power, area efficient, and high speed analog-to-digital converters is moving towards the use of dynamic regenerative comparators to maximize speed and power efficiency. Due to the better performance of double-tail architecture in low-voltage applications, the existing comparator design is based on the double-tail structure.

The main idea of the existing comparator is to increase ΔVfn/fp in order to improve the speed of latch regeneration . For this purpose, two control transistors (Mc1 and Mc2) have been added to the first stage in parallel to M3/M4 transistors but in a cross-coupled manner[4][8].

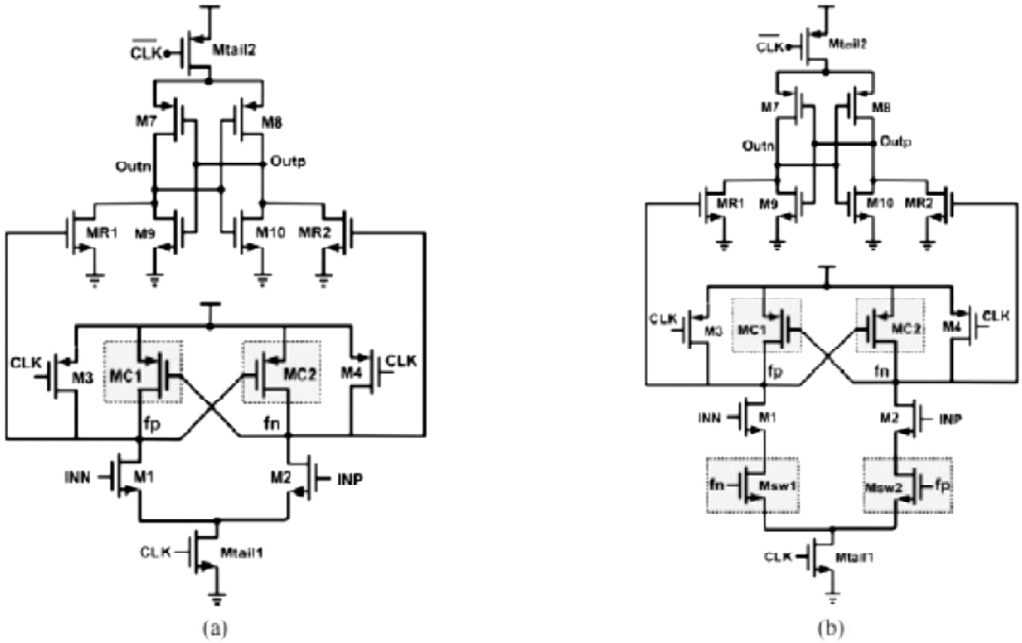

Figure 1: Schematic diagram of existing DT dynamic comparator. (a) Main idea. (b) Final structure

2.1. Operation of existing Comparator: The operation of the existing comparator is shown in Fig.1. During reset phase (CLK = 0, Mtail1 and Mtail2 are off, avoiding static power), M3 and M4 pulls both fn and fp nodes to VDD, hence transistor Mc1 and Mc2 are cut off. Intermediate stage transistors, MR1 and MR2, reset both latch outputs to ground[8][5].

During decision-making phase (CLK = VDD, Mtail1 and Mtail2 are on), transistors M3 and M4 turn off.At the beginning of this phase, the control transistors are still off (since fn and fp are about VDD). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose VINP>VINN, fn drops faster than fp, (since M2 provides more current than M1). As long as fn continues falling, the corresponding PMOS control transistor (Mc1 in this case) starts to turn on, by pulling fp node back to the VDD, so another control transistor (Mc2) remains off, allowing fn to be discharge completely. In other words, conventional double-tail dynamic comparator, in which Vfn/fp is just a function of input transistor transconductance and input voltage difference, in the existing structure as soon as the comparator detects that for instance node fn discharges faster, a PMOS transistor (Mc1) turns on, pulling the other node fp back to the VDD[4],[8],[9]. Therefore by the time passing, the difference between fn and fp (Vfn/fp) improves in an exponential manner, leading to the decrease of latch regeneration time. Inspite of the effectiveness of the existing idea, the main thing that should be considered in this circuit, when one of the control transistors (e.g., Mc1) turns on, a current from VDD is drawn to the ground via input and tail transistor (e.g., Mc1, M1, and Mtail1), resulting in static power consumption. In order to overcome this issue, two NMOS switches are used below the input transistors [Msw1 and Msw2, as shown in Fig. 1(b)]. At the earlier stage of the decision making phase, due

to the fact that both fn and fp nodes have been pre-charged to VDD (during the reset phase), at different discharging rates both switches are closed and fn and fp start to drop. As soon as the comparator detects that one of the fn/fp nodes is discharging faster, control transistors will act in a way to improve their voltage difference. When fp is pulling up to the VDD and fn should be discharged completely, the switch in the charging path of fp will be opened (in order to prevent any current drawn from VDD) but the other switch connected to fn will be closed to allow the complete discharge of fn node. In other words, the operation of the control transistors with the switches emulates the operation of the latch[7].

3. PROPOSED TDC DESIGNS

The Proposed Time to Digital converter (TDC) designed for decreasing the average power consumed, the transient noise and the output noise. Conventional design has high power consumption and noise. Hybrid based architecture is used in the Time to Digital Converter design. A charge pump is implemented by placing the capacitor in the circuit. This gives out the charge even the supply is in off state. Level shifter is used to boost up the low level voltage to the high level voltage. Eventually counter is used to display the ouput in the digitized format. In digital circuits the propagation delay or gate delay, is given as the length of time which starts when the input to a logic gate becomes stable and valid to change, to the time that the output of that logic gate is stable and valid to change. Often on manufacturers' datasheets this refers to the time required for the output to reach 50% of its final output level when the input changes to 50% of its final input level. Decreasing gate delays in digital circuits allows them to process data at a faster rate and increase overall performance. Propagation delay increases with operating temperature, marginal supply voltage as well as an increased output load capacitance[1][2][3].

The proposed designs are designed using the Tanner EDA tool and moreover the proposed DTC is carried out in nanodevice like MOSFET, FinFET AND GNRFET using HSPICE Synopsis.The proposed DT dynamic comparator is based on combining the transconductance of both p type and n type transistors. It has two phases.

1. RESET Phase — Clock '0'
2. COMPARISON Phase — Clock '1'

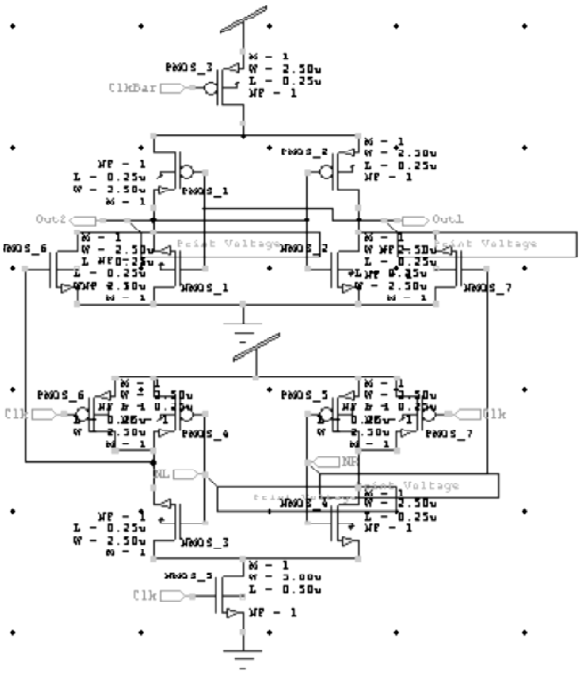

Figure 2: Proposed Comparator design

3.1. Reset Phase: During reset phase (CLK = 0), transistors P3 and N5 are off, avoiding static power, P6 and P7 are turns on then pulls both fl and fr nodes to VDD. Intermediate stage transistors, N6 and N7, reset both latch outputs to ground.

3.2. Comparison phase: At the decision-making phase (CLK = VDD), transistors P3 and N5 turns on, transistors P6, P7 turn off. Furthermore, at the earlier stage of this phase, the fl and fr nodes are about VDD. Thus, fl and fr starts to drop with different rates according to the input voltages. Suppose NL > NR, thus out1 drops at a faster rate than out2. The inputs are applied during decision making phase, the 0.2V and 0.8V are given at the input nodes NR and NL respectively. In accordance with the inputs given here, the input NL corresponding N3 transistor conducts and P4 transistor turns off and pull the fl node with digitally low value (0). The fl node value is given as input gate value to N6. The NR input value is given here is 0.2V, transistor N4 turns off and P5 pulls up the fr node with digitally high value (1). The fr node value is given as input gate value to N7 transistor. After the n-channel transistor turns on (N2 transistor) output (out 2) will be discharged to the ground, charging front p-channel transistor to turn on and charge another output (out 1) to VDD. The regeneration time is achieved in accordance with the latching delay of two cross-coupled inverters. The difference between fr and fl (V fr/fl) increases in an exponential manner. This leads to the decrease of latch regeneration time. Instead of control transistors and switching transistor used in existing circuit, the average delay and power is obtained by providing input voltage at the inverter based architecture[1][2].

3.3. Sub-threshold Operation with Current Tails: When this inverter-based architecture is designed at a low supply voltage (<2vt), the inverter transistors will operate in the sub-threshold region. Because of this region of operation, bias currents and power consumption can be significantly decreased, with the sacrifice of bandwidth and amplifier driving strength. A tail current source can be used to better control the current flow through the inverters, pushing the transistors further into the sub-threshold region, and further decreasing power consumption. The use of tail isolates the need for low power consumption and low input offset voltage. When this architecture is implemented with a standard supply voltage (>2vt), the overall transconductance can be increased significantly depending on how transistors in the inverters are sized and the resulting current through the inverter[3]. High current through the inverter allows significantly to achieve high bandwidths. Another advantage of this topology is an improvement in output swing and linearity when compared to a traditional common source or cascode amplifier if the respective transconductance of the p and n type transistors are equal in magnitudeapproximately. For noise, the inverter-based topology produces lower equivalent noise resistance compared to the equivalent common source topology[4][8].

3.4. Proposed Time to Digital Converter: The proposed Time to Digital Converter (TDC) design is built based on the hybrid architecture. A charge pump is implemented by placing the capacitor in the circuit. This gives out the charge even if the supply is in off condition. Level shifter is used to built up the low level voltage to the high level voltage.Eventually counter is used to display the ouput in the digitized format[1].

The supply voltage is connected with one of the comparator's input and the capacitor. The capacitor of value 1pf is charged during the 'on' condition of the supply voltage and discharged when it is in 'off' condition. The comparator block is followed by the inverter circuit. Level shifter is placed between the feedback path

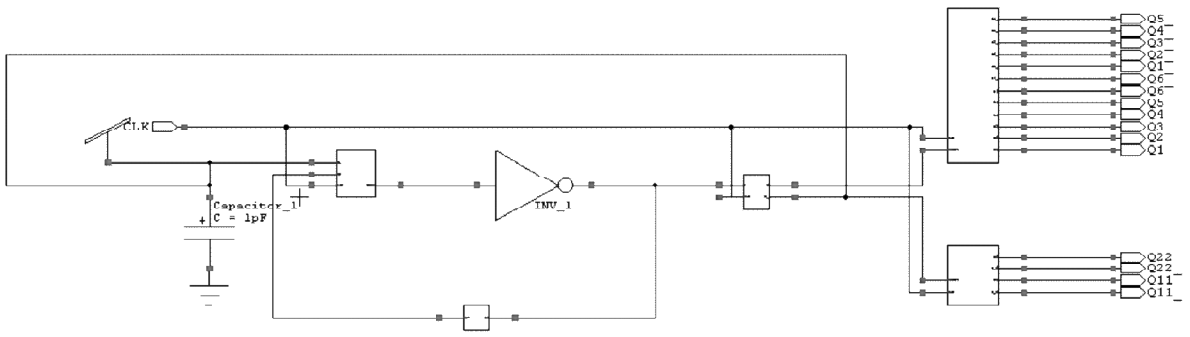

Figure 3: Proposed Time to Digital converter design

of inverter to another input voltage of the comparator to maximize the voltage level i.e., low vdd level to the high vdd level. At the binary counter, the output is obtained as digitized through the flip flop from the previous blocks.

4. NANO DEVICES

FINFET: Generally Conventional CMOS technology's performance deteriorates due to improve the short channel effects. Double-gate (DG) FinFETs has better short channel effects performance compared to the conventional CMOS and also it is used tostimulates technology scaling**.** The main disadvantage of using CMOS transistors are high power consumption and high leakage current. Fin-type field-effect transistors (FinFETs) are most suitable substitutes for bulk CMOS in nano- scale circuits. FinFET, which is a double-gate field effect transistor (DGFET), is more versatile than traditional single-gate field effect transistors because when compared tocontrolled independently it has two gates. Usually, the second gate of FinFET transistors is used to dynamically control the threshold voltage of the first gate in order to increase the performance and decrease the leakage power. In the context of digital logic design, the ability to control the two gates of a DG-FET independently has been utilized chiefly in two ways: by adding pairs of parallel transistors to decrease circuit area and capacitance, and the next way through the use of a back-gate voltage bias to modulate transistor threshold voltage. A parallel transistor pair which consists of two transistors with their source and drain terminals tied together. In Double-gate (DG) FinFETs, the second gate is merged opposite the traditional (first) gate, which have been identified for their potential to better control short-channel effects (SCEs) and as well as to control leakage current. The four modes ofFinFET operation are recognized, such as the shorted-gate (SG) mode with transistor gates tied together, the independent gate (IG) mode where independent digital signals are used to drive the two device gates, the low-power (LP) mode where the back-gate is tied to a reverse-bias voltage to reduce leakage power and the hybrid (IG/LP) mode, which employs a combination of LP and IG modes .The structure of the FinFET is shown in the Fig 4b.Over the past decade, much efforts have been directed to the introductionof new materials such as compound semiconductors,carbon nanotubes, and graphene. Among them, graphenedue to its excellent electronic properties has attracted considerable attention from the scientific community, such as high electronand hole mobilities even at room temperature and at high dopingconcentrations , high thermal conductivity , and its interestingoptical properties. Graphene is a gapless material,which makes it unsuitable for transistor application. However,an energy gap can be induced by tailoring a graphene sheet intonanoribbons [graphenenanoribbons (GNRs)] . GNRs can have edgeswith zigzag shape, armchair, or a combination of these two. GNR structuredependingon the orientation of the ribbon edges, has been shown in fig. 4c[11].

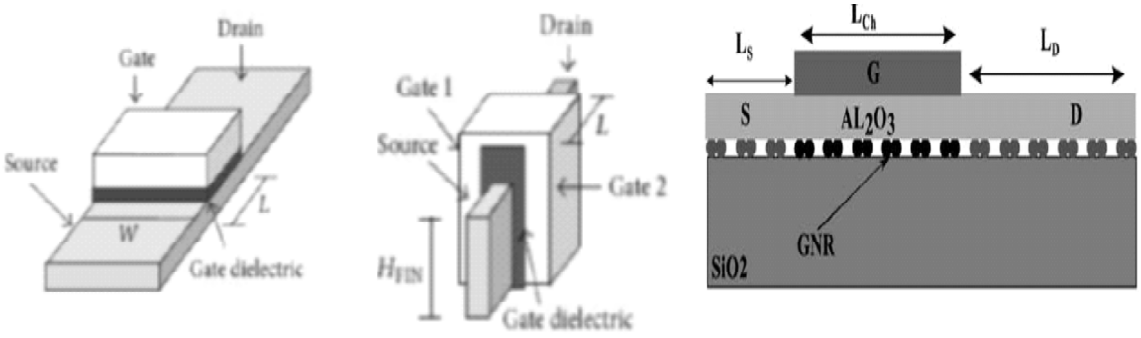

Figure 4: Structure of a) MOSFET b) FINFFET C) CNTFET

5. RESULTS AND DISCUSSIONS

These proposed design is further implemented in FinFET, GNRFET technology. FinFETand GNRFET based SRAM cell designs are simulated using HSPICE synopsis. Thus, the following results are obtained from HSPICE coding under FINFET and GNRFET 16nm technology.

POWER COMPARISON

The power comparison of comparator designs are compared below in Table1. The power comparison for TDC designs are shown in Table 2.

Table 1
Power comparison between comparator designs

COMPARATOR DESIGNS	*POWER (in watts) FINFET*	*POWER (in watts) GNRFET*
Conventional Single tail	3.158480×10^-8	4.487231×10^-10
Conventional Double tail	8.011349×10^-8	6.674239×10^-10
Existing Design 1	7.194841×10^-8	7.857202×10^-10
Existing Design 2	1.077523×10^-7	2.985703×10^-9
Proposed Comparator	7.446347×10^-8	5.988799×10^-10

Table 2
Power comparison between TDC designs

TDC Designs	*Static 0v (mW)*	*Static 5v(mW)*	*Dynamic(mW)*
Conventional TDC	0.2439927	0.3742227	0.2439927
Proposed TDC Using design1	0.1219976	0.1409117	0.1607451
Proposed TDC Using design2	0.1219976	0.1774055	0.1607472

5.2. Noise Analysis

Noise analysis can be performed in 0.18um technology at a temperature of 25 deg C. The devices work normally at this temperature i.e., Tnor. The output noise and their transfer function of existing and the proposed methods are then compared for various frequencies. This analysis mainly deals with the input noise, output noise and resulting transfer function. Thus the transfer function is obtained as, *Transfer Function = output noise equivalent input noise* i.e., *TF = VoutVin*

Table 3
Noise obtained on comparator designs

Frequency	*Tdc Design*	*Transfer Function (Vout/Vin)*	*Output Noise (V/Hz)*	*Input Noise*
2 MHz	Conventional	1.2339e-004	3.3076e-009	2.6807e-005
Existing	1.0000e-004	6.6446e-009	6.6446e-009	
proposed	1.2339e-004	3.3076e-009	2.6807e-005	
10 MHz	Conventional	6.1840e-004	3.3076e-009	5.3487e-006
Existing	9.9999e-004	6.6445e-009	6.6445e-009	
proposed	6.1840e-004	3.3076e-009	5.3487e-006	
500 MHz	Conventional	3.0118e-002	3.2939e-009	1.0937e-007
Existing	9.7635e-001	6.2403e-009	6.3914e-009	
proposed	3.0320e-002	3.2940e-009	1.0864e-007	
2 GHz	Conventional	9.9482e-002	3.1249e-009	3.1411e-008
Existing	7.9127e-001	3.9507e-009	4.9928e-008	
Proposed	9.9724e-002	3.1236e-009	3.1323e-008	
3 GHz	Conventional	1.3756e-001	2.9433e-009	2.1396e-008
Existing	7.0061e-001	2.9671e-009	4.2351e-009	
proposed	1.3436e-001	2.9418e-009	2.1896e-008	

CONCLUSION

This aims at designing a low power double tail comparator and implementing that in the high speed Time to Digital Converter. The proposed designs reduces dynamic power consumption as well as static power consumption on compared to conventional design. These designs also has reduced noise compared to conventional one. The proposed comparator design is based on latch based comparator. The power minimization is obtained by using the double tails (single pmos and nmos connected directly with supply voltage and ground respectively). By the proposed design, subthreshold leakage and the voltage swings are reduced which leads to the increase in efficiency of the comparator architecture. The implementation of comparator circuit in the charge pump based Time to Digital Converter (TDC) design results in the effective TDC for the PLL based applications. From the simulation and comparison results of conventional, existing and proposed designs of comparator and Time to Digital Converter. Here the simulations are done using Synopsis Hspice tool under 16nm FINFET and GNRFET technology. The analysis of the proposed design also takes various parameters like Noise, Power under consideration. Noise analysis is done for existing design and proposed design for various frequencies at nominal temperature. This analysis includes the input noise, output noise and resulting transfer function. Power is compared for existing and proposed designs. Finally 16nm FINFET and GNRFET based comparator design is simulated and average power is obtained using HSPICE Synopsis.

REFERENCES

[1] Chin-Hsin Lin, MarekSyrzycki (2011), 'Single-Stage Vernier Time-to-Digital Converter with Sub-Gate Delay Time Circuits and Systems', Vol. 2, Issue 8, Pp. 365-371.

[2] Fiorenza J K (2006) et al., 'Comparator-Based Switched-Capacitor Circuits for Scaled CMOS Technologies', IEEE Journal of Solid State Circuits, Vol. 41, Issue 12, Pp. 2658-2668.

[3] Guansheng Li, Yahya M, Tousi (2009), 'Delay-Line-Based Analog-to-Digital Converters', IEEE Transactions on Circuits And Systems, Vol. 56, Issue 6, Pp. 56-63.

[4] Ping Lu, Ying Wu, PietroAndreani (2012), 'A 90nm CMOS digital PLL based on Vernier-Gated-Ring-Oscillator Time-to-Digital Converter', IEEE International Symposium on Circuits and Systems, Pp. 2593-2596.

[5] SamanehBabayan-Mashhadi, Reza Lotfi (2013), 'Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator', IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 22, Issue 2, Pp. 156-163.

[6] ShrutiHathwalia et.al (2014), 'Analysis & Design of Low Power CMOS Comparator at 90nm Technology', International Journal of Engineering Research and Applications, Vol. 4, Issue 4, Pp. 289-292.

[7] ShaikMastanVali, Pyla Rajesh (2013), 'A 3GHz Low-offset Fully Dynamic Latched Comparator for High-Speed and Low-Power ADCs', International Journal of Emerging Technology and Advanced Engineering, Vol. 3, Issue 6, Pp. 96-102.

[8] Umamaheswari V S, Rajaramya V G (2014), 'Low Power High Performance Double tail Comparator', International Journal of Scientific Engineering and Technology, Vol. 3, Issue 5, Pp. 647-650.

[9] Wei Deng, Dongsheng Yang, Tomohiro Ueno, Tomohiro Ueno, TeerachotSiriburanon, Satoshi Kondo, Kenichi Okada, Akira Matsuzawa (2015), 'A Fully Synthesizable All-Digital PLL With Interpolative Phase Coupled Oscillator, Current-Output DAC, and Fine-Resolution Digital Varactor Using Gated Edge Injection Technique', IEEE Journal of Solid-State Circuits, Vol. 50, Issue 1, Pp. 899-903.

[10] HueiChaeng Chin, etal, "Enhanced device and circuit level performance benchmarking of GrapheneNanoribben FET against a Nano-MOSFET with Interconnect", Journal of Nanomaterials, vol. 2014, pp14, 2014.