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Comparative Analysis and design of CMOS Folded Cascode OTA using different technology nodes by Using Gm/ID Technique

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ABSTRACT

In this paper we proposed a folded cascode operational trans conductance amplifier OTA that designed by using 0.35 µm CMOS technology node. We analyze this proposed OTA in different regions of operations: Moderate, weak and Strong inversion region and also separately calculate the Unity Gain Bandwidth and Noise margin, Phase margin and power consumption for each region . In strong region and weak region, moderate region simulation shows the DC Gain of 80.4 dB, 77.56db , 76.45db and Power consumption of 413.34 µW, 110.67 nW, 27.67nW and Phase margin of 76.56°, 78.23° 89° respectively. The total noise in the circuit is 106.14mV in strong inversion region, 54.44mV in moderate inversion region and 9.85mV in weak inversion region .Also in this paper we compared the proposed design on different technology modes i.e. 350nm, 180nm, 130nm and 90nm.

Keywords: Operational Transconductance Amplifier, analog integrated circuits, Complementary Metal Oxide Semiconductor, Operational Amplifier, Bandwidth, Phase margin

1. INTRODUCTION

The Operational Amplifier is the backbone of analog circuit design. Op-amps are basically designed to provide very high output impedance and hence provide very good isolation. The output voltage, current, output impedance and the gain of the op-amp can be set in order to suit the application. These op-amps are utilized in circuits like integrators, differentiators, buffers, analog to digital converters and digital-to-analog converters. The amplifier's performance is usually limited due to various factors such as gain, bandwidth, slew rate, voltage swing, etc. Gain and speed are the two important parameters of the operational amplifier[1]. The transconductance of the amplifier is dependent upon the bias current and is calculated by the formula.

$$I_{o} = G_{m} \{V(+) - V(-)\} \quad (1)$$

The main objective is to achieve high gain, lower noise and high gain bandwidth. Another important parameters are slew rate and input common mode range. Telescopic and folded cascade structures are the two main structures for operational amplifiers.In this work higher gain and higher bandwidth can be achieved by using gain boosting technique. The OTA is an amplifier without buffer at output stage drives only load .Which is called as VCCS because its differential input voltage produces a current at output stage. The design procedure is based on following main parameters: noise, phase margin, gain, load capacitance, slew rate (SR), input common mode range, common mode rejection ratio (CMRR) and power mode rejection ratio (PSRR) with less power consumption common mode rejection ratio (CMRR) and power mode rejection ratio (PSRR) with less power consumption.

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2. OTA CONCEPT

OTA is called as voltage controlled current source, its takes the difference of the two voltages as the input and converted into current. The ideal model of OTA can be represented as

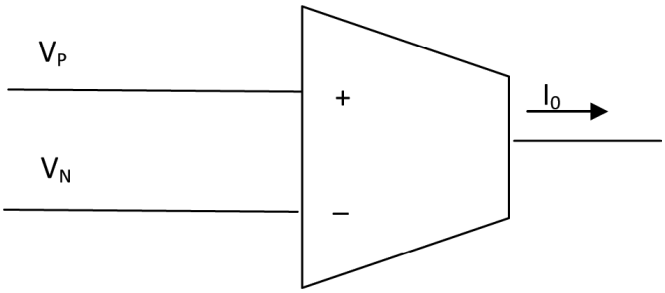

Figure 1: OTA ideal model

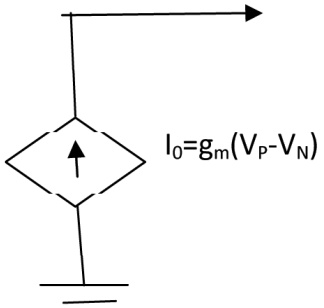

Figure 2: Equivalent circuit of OTA

The output current can be expressed as

$$I_0 = g_m (V_P - V_N) \tag{2}$$

where gm is the transconductance and can be expressed as

$$g_m = \frac{KT}{2qI_{Bias}} \tag{3}$$

Where K is Boltzmann constantand T is temperature in Kelvin

As the output of an OTA is derived as the current, the input and the output impedance of the OTA is very high (ideally infinity). It can be characterized as 9

$$I_0 = g_m V_i \tag{4}$$

$Z_i = \infty$, $Z_0 = \infty$ where I_0 is the output current and V_i is the input voltage respectively. Z_i and Z_0 are the input and output impedance respectively.

2.1. Block Diagram of Folded Cascode OTA

The circuit presented here is a folded cascode operational transconductance amplifier. The first stage consists of NMOS differential pair M1 and M2 because NMOS is having greater mobility. There are many configurations of OTA like single stage OTA, two stage OTA, class AB OTA but folded cascode is considered due to is high gain and high bandwidth.

Transistors M3 and M4 form a current mirror circuit which provides DC bias voltage to transistors M5, M6 M7 and M8.

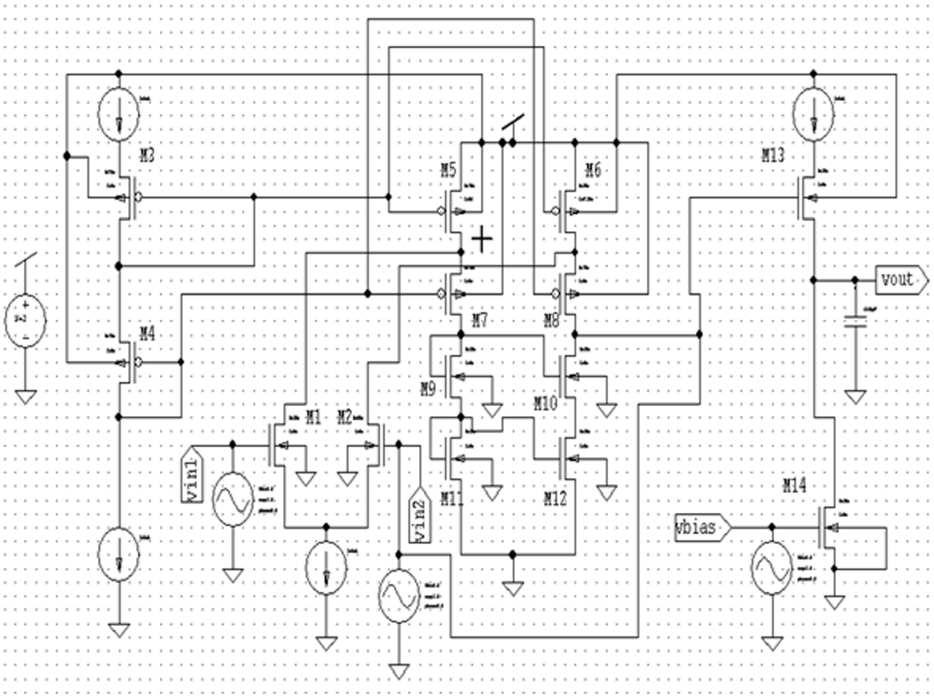

Figure 3: Folded Cascode OTA Architecture

2.1. Gain Boosting Technique

The cascaded structures are used to boost the gain. The transfer function of cascade stage is

$$\frac{\Delta I_0}{\Delta V_i} = \frac{g_{m1}\left(g_{m2}r_{01} + \frac{r_{01}}{r_{02}}\right)}{\left(g_{m2}r_{01} + \frac{r_{01}}{r_{02}} + 1\right)} = gm_{eff} \tag{5}$$

The output voltage is given by

$$\Delta V_0 = \Delta I_0 R_{out} \tag{6}$$

Where R_{out} is the output impedance and is given by

$$R_{out} = \left(g_{m2}r_{02} + 1\right)r_{01} + r_{02}$$

Now the DC gain can be calculated as

$$A_0 = g_{m1}r_{01}\left(g_{m2}r_{01} + 1\right) \tag{7}$$

A cascode is a two transistor stack used to obtain high gain and high outputimpedances. A cascode consists of a common source configuration followed by acommon gate stage [2]. Consider in figure 2.4 the action of the circuit in response to the testcurrent I_x applied at node B. This will flow through R_2 and raise the voltage atintermediate node A. If there is no input given to M_1 then $V_x = I_x R_1$.

However as V_a is driving M2 it will produce a transconductance current $I_{ds} = G_{M2} V_a$. This will flow through R_2 in addition to the externally applied I_x. Thus

$$V_x = V_b = V_a + (I_x + G_{M2}) R_2 \tag{8}$$

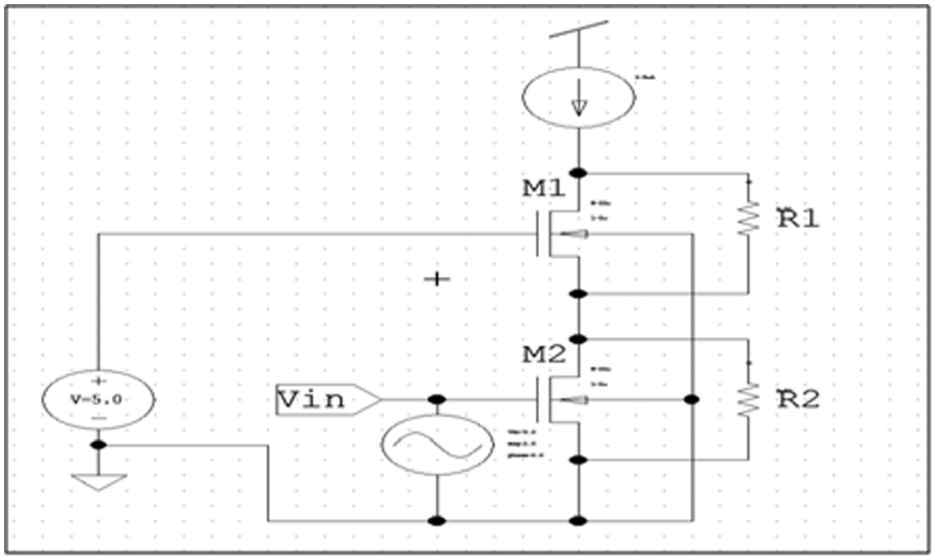

Figure 4: Cascode Gain Stage

Hence the output impedance is

$$R_1 + (1 + G_{M2}\, R_1)\, R_2 \tag{9}$$

$R_1 + (1 + G_{M2}\, R_1)\, R_2$ which is usually taken as $G_{M2}\, R_1\, R_2$

Hence $R_{out} = G_{M2}\, R_1\, R_2$

The other important thing is that the input impedance at the intermediate node Ais very small, usually taken to be $\frac{1}{G_{M2}}$. Thus the Miller effect on the capacitance $C_{gd}(M_1)$ is greatly reduced. The cascode configuration gives more gain as compared to a simple commonsource configuration. The gain is taken to be the product of the transconductanceand the output impedance. The gain depends on the loading of the amplifier. The load impedance should be suitably high or the effect of high output resistance ofthe cascode configuration is lost.

3. DESIGN METHODOLOGY

Through this methodology the high DC gain and high bandwidth can be achieved.The flow diagram of this methodology can be shown as

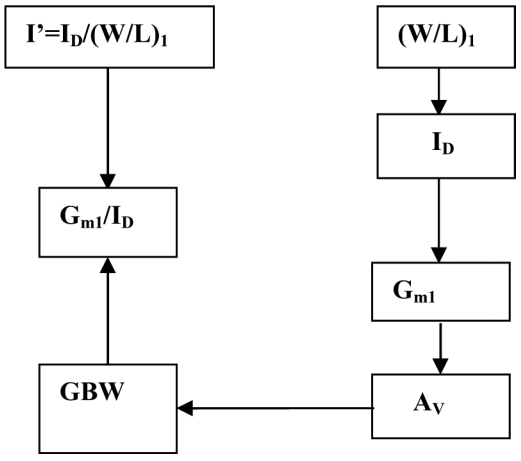

Figure 5: Design methodology of folded cascode OTA

3.1. G_m/I_D Methodology for Folded Cascode OTA

The various performance parameters of folded cascade OTA are DC gain, unity gain bandwidth, noise and power and these can be analyzed using bias current, supply voltage etc.

3.2. Design in Weak Inversion Region

Weak inversion presents higher gm/ID values with smaller current, so an increased gain is favorable for this operating mode. The capacitance value used in this region is 10fF i.e (C_L(fF) = 10) with the supply voltage of 1V. The specifications in weak inversion region can be presented in Table 1.

Table 1
Design parameters in weak inversion region

Parameters	*Values*
I_D(µA)	40nA-0.4µA
$W_{1,2}$(µm)	5.25
$W_{9,10,11,12}$(µm)	4.5
$W_{3,4}$(µm)	13.625
$W_{5,6,7,8}$(µm)	14.563
W_{13}(µm)	26.87
W_{14}(µm)	6.4

3.3. Design in Strong Inversion Region

In strong region of operation G_m/I_D ratio decreases as a function of current. The capacitance value used in this region is 0.1pF i.e(C_L(pF) = 10) with the supply voltage of 2V. The design parameters in strong inversion region can be shown in Table 2.

Table 2
Design parameters in strong inversion region

Parameters	*Values*
I_D(µA)	54
$W_{1,2}$(µm)	3.7
$W_{9,10,11,12}$(µm)	3.7
$W_{3,4}$(µm)	7.75
$W_{5,6,7,8}$(µm)	7.75
W_{13}(µm)	28.78
W_{14}(µm)	18.56

3.4. Design in Moderate Inversion Region

In weak inversion, we succeed in reaching good performances with very low consumption; hence, the gain bandwidth product isn't raised and necessary enough to satisfy wide band applications.

In order to improve gain bandwidth parameter, relatively with the same lower consumption, we will study the design of the OTA in moderate inversion region. The capacitance value used in this region is 0.1pF i.e(C_L(pF) = 10) with the supply voltage of 2V. The specifications can be shown in Table 3.

Table 3
Design parameters in moderate inversion region

Parameters	*Values*
$I_D(\mu A)$	5μA
$W_{1,2}(\mu m)$	4.5
$W_{9,10,11,12}(\mu m)$	4.5
$W_{3,4}(\mu m)$	9.5
$W_{5,6,7,8}(\mu m)$	9.5
$W_{13}(\mu m)$	29.99
$W_{14}(\mu m)$	4.5

4. RESULTS & DISCUSSION

4.1. Weak Inversion region

After applying the above parameters as discussed in table I, the following parameters has been achieved with a output current of 52nA ($I_D(nA) = 52$), gain of 77.56 dB with unity gain bandwidth of 18.56MHz with a supply voltage of 1V as shown in fig 6.

The curve described the dynamic power consumed by the circuit in Weak inversion region is shown in Fig.7.

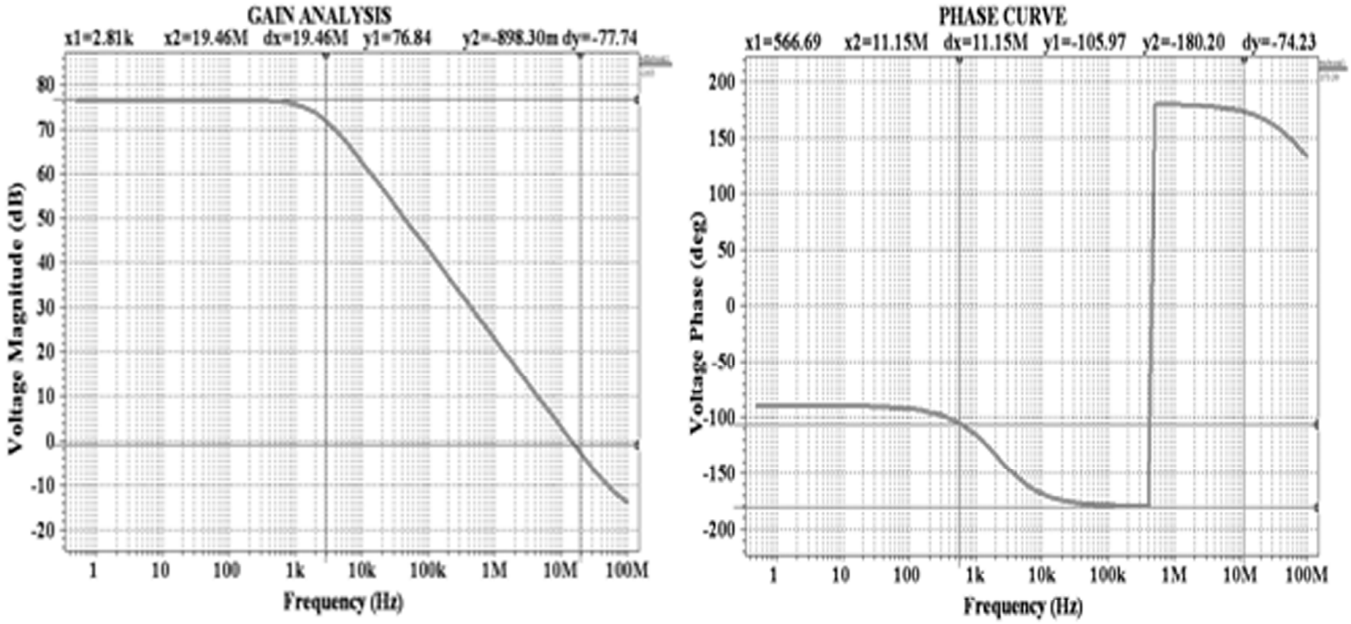

Figure 6: Folded cascode OTA's gain &phase curve in weak inversion region

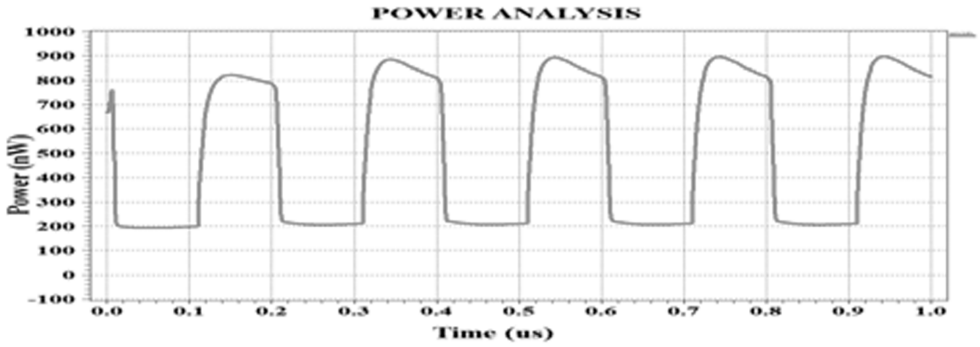

Figure 7: Power consumption in weak inversion region

The folded cascodeOTA consumes average power of 0.1167 µW.as shown fig 7.

The curve described the total noise in the circuit in weak inversion region is shown in fig. 8.

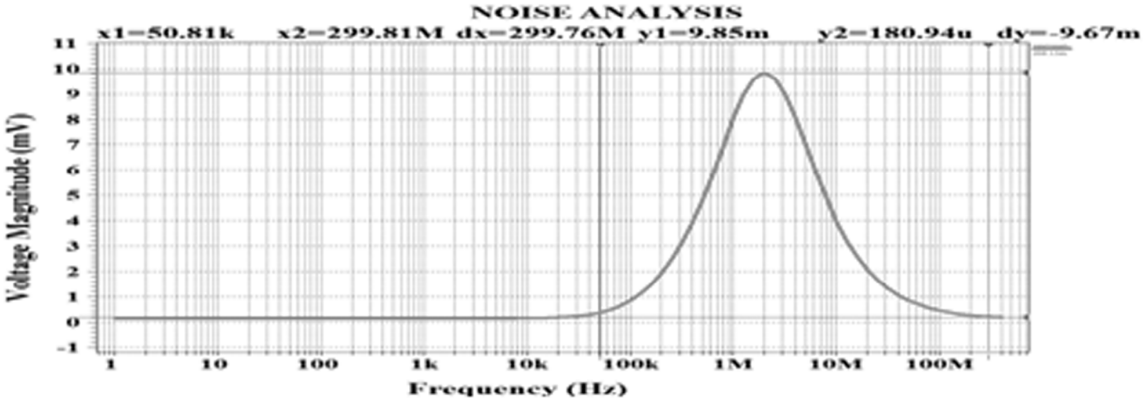

Figure 8: Noise in weak inversion region

Noise rises up to 8.75mV at a cut off of 287.76MHz and then decreases at a point of 170.94µV.

4.1.1. Comparison on basis of different Technology Nodes

After evaluating different parameters in weak inversion region, the comparison between different technology nodes has been made as shown in Table 4.

Table 4
Weak inversion region of folded Cascode OTA

Parameters	*Technology Node*			
	350nm	*180nm*	*130nm*	*90nm*
Power Consumption(nW)	110.67	103.56	78.67	67.45
DC Gain(dB)	77.56	76.58	74.32	67.89
Phase Margin(degrees)	78.23	89.35	81.34	76.67
GBW(MHz)	18.56	17.54	4.35	11.78

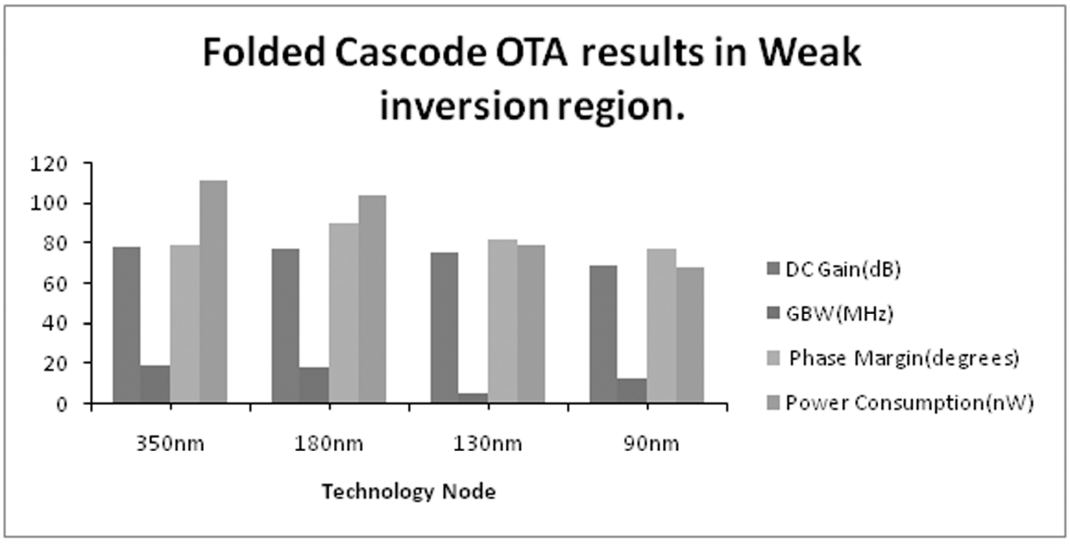

Figure 9: Comparison in weak inversion region

4.2. Strong inversion Region

After applying the above parameters as discussed in table II, the following parameters has been achieved with a output current of 27.5μA (I_D(μA) = 27.5), gain of 80 dB with a unity gain bandwidth of 440.05 MHzandphase margin of 76.56degas shown in fig.10with power consumption of 413.34μW as shown in fig 11.

The curve described the dynamic power consumed by the circuit is shown in fig. 11.

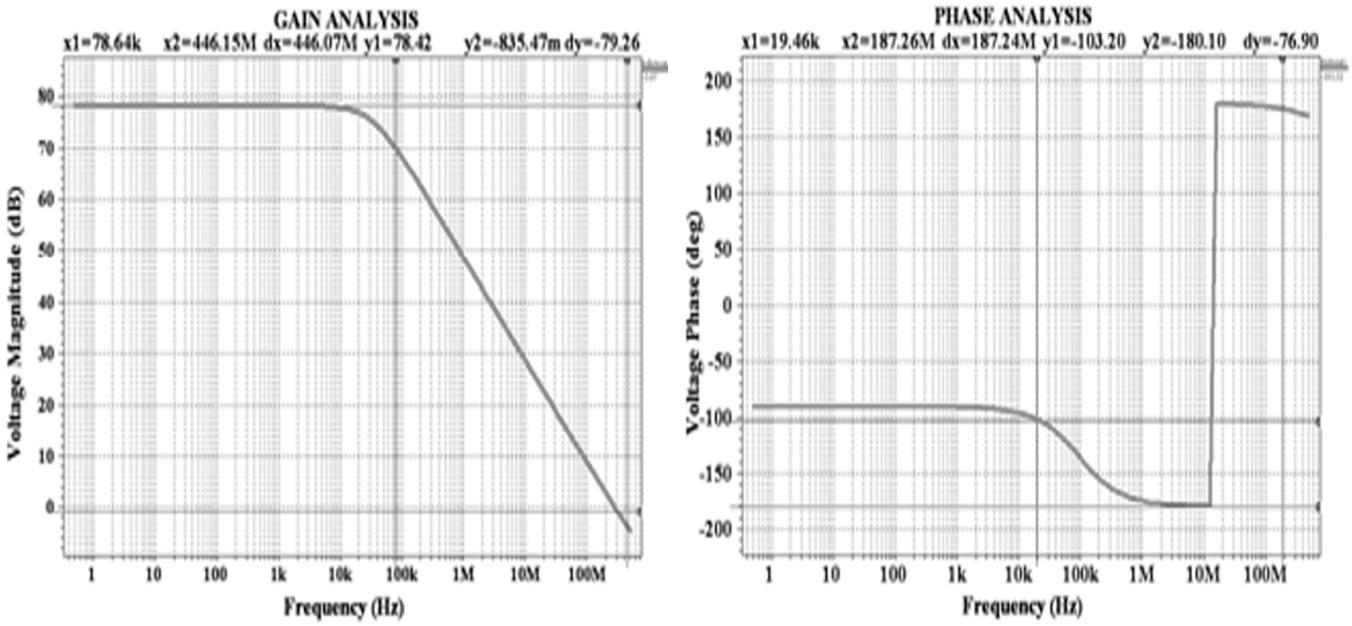

Figure 10: Phase & Gain curve of folded cascode OTA in strong inversion region

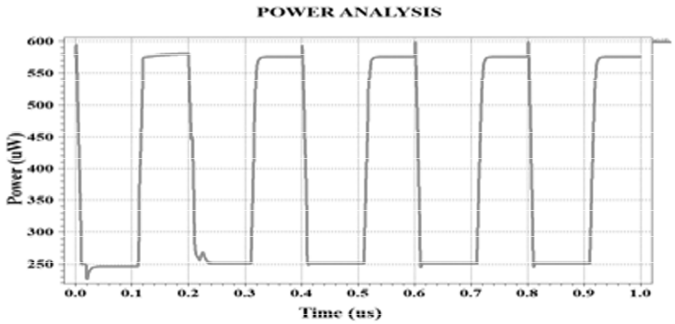

Figure 11: Power Consumption of folded cascode OTA in strong inversion region

The folded cascode OTA consumes average power of 413.34 μW as shown in fig 10 and

The curve described the total noise in the circuit in strong inversion region is shown in fig.12.

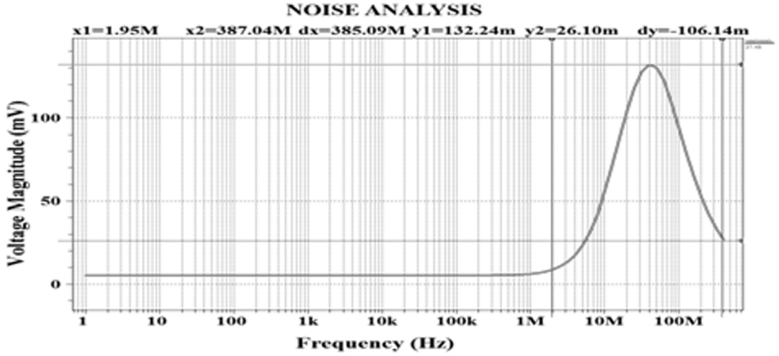

Figure 12: Noise in Strong inversion region

Noise rises up to 122.26mV at a cut off frequency of 376.87MHz and then decreases at a point of 30.12mV

4.2.1. Comparison on basis of different Technology Nodes

After evaluating different parameters in strong inversion region, the comparison between different technology nodes has been made as shown in Table 5.

Table 5
Strong inversion region of folded Cascode OTA

Parameters	*Technology Node*			
	350nm	180nm	130nm	90nm
Power Consumption(μW)	413.34	409.35	397.37	386.35
DC Gain(dB)	80.4	78.28	73.18	64.64
GBW(MHz)	440.05	286.97	110.06	89.05
Phase Margin(deg)	76.56	80.34	83.13	79.45

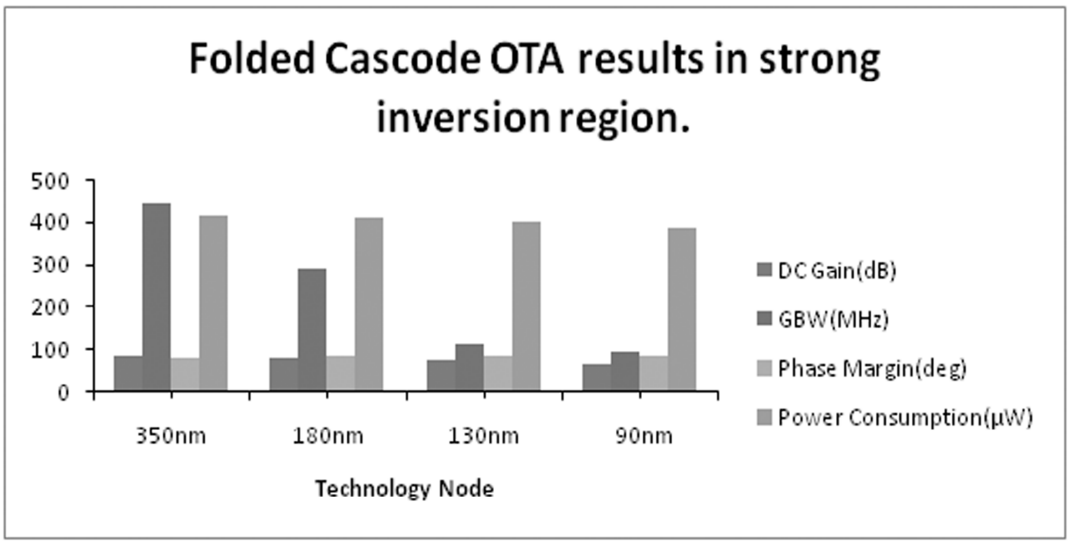

Figure 13: Comparison in strong inversion region

4.3. Moderate inversion Region

After applying the above parameters as discussed in table 3, the following parameters has been achieved with a output current of 2 μA (I_D(μA)=2), a gain of 94dB with unity gain bandwidth of 76.45MHz with a supply voltag of 2V as shown in fig 14.

The curve described the dynamic power consumed by the circuit in Moderate inversion region is shown in Fig. 15.

The folded cascode OTA consumes average power of 27.67 μW. The maximum and minimum power consumed by the folded cascode OTA is 30.857 μWand 8.624 μW respectively.

The curve described the total noise in the circuit in moderate inversion region is shown in fig.16

Noise rises up to 93.46mV at a cut off frequency of 1.67MHz and then decreases at a point of 40.52mV.

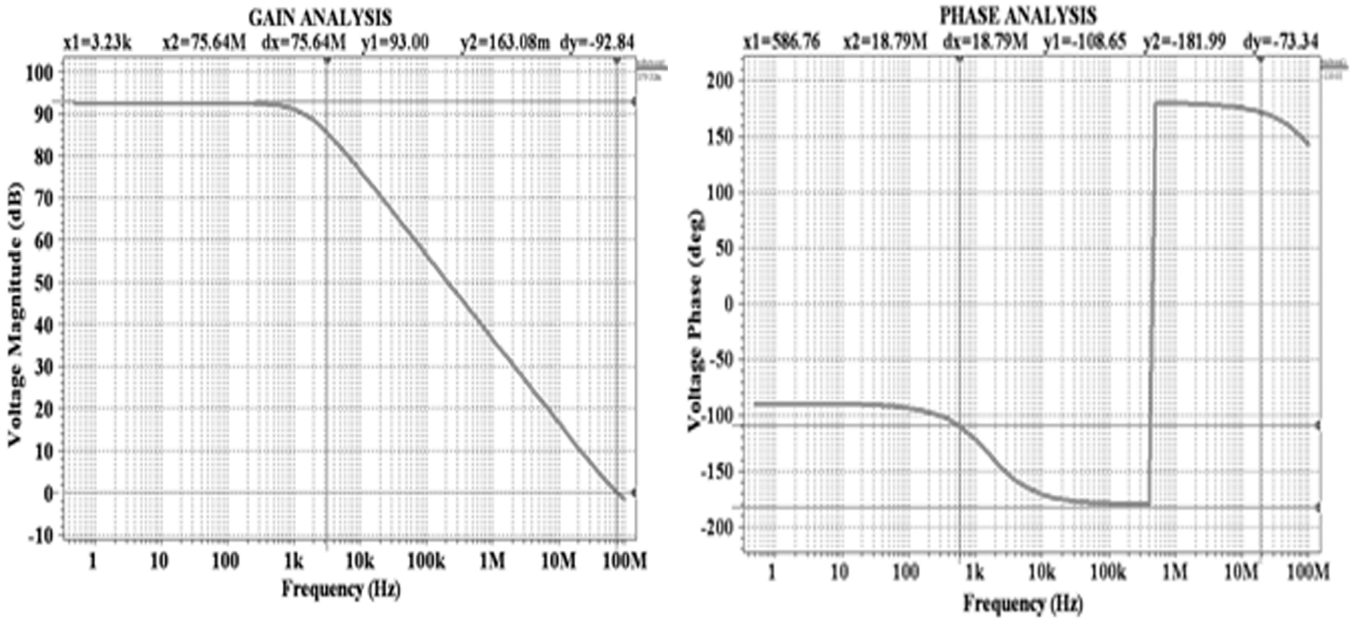

Figure 14: Folded cascode OTA's gain &phase curve in moderate inversion region

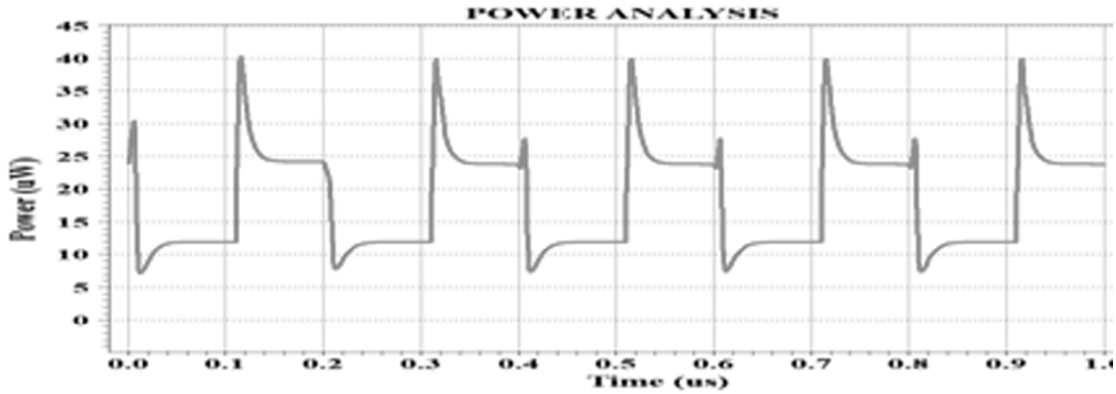

Figure 15: Power consumption in moderate inversion region

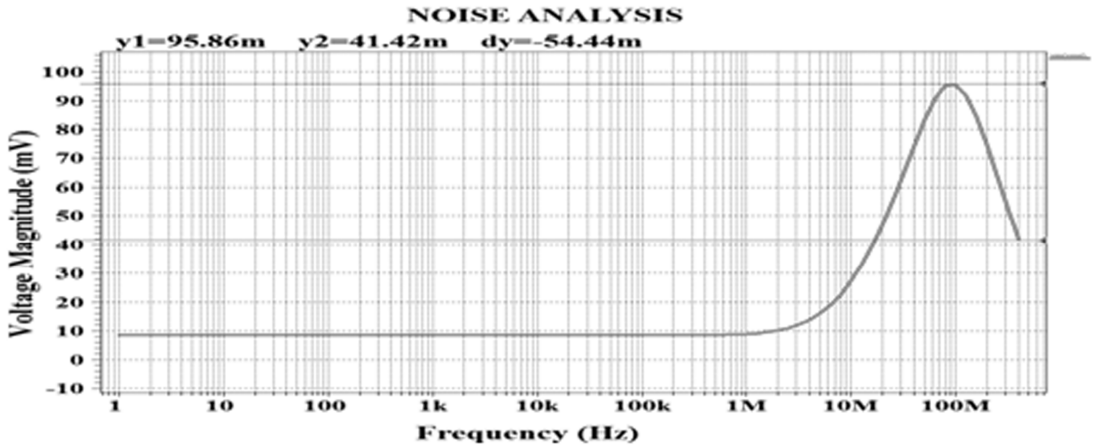

Figure 16: Noise in moderate inversion region

4.3.1. Comparison on basis of different Technology Nodes

After evaluating different parameters in moderate inversion region, the comparison between different technology nodes has been made as shown in Table 6.

Table 6
Moderate inversion region of folded Cascode OTA

Parameters	*Technology Node*			
	350nm	180nm	130nm	90nm
DC Gain(dB)	94	89.34	87.45	68.34
GBW(MHz)	76.45	78	65.78	56.78
Phase Margin(degrees)	89	78.56	73.48	71.45
Power Consumption(μW)	27.67	24.35	20.78	16.78

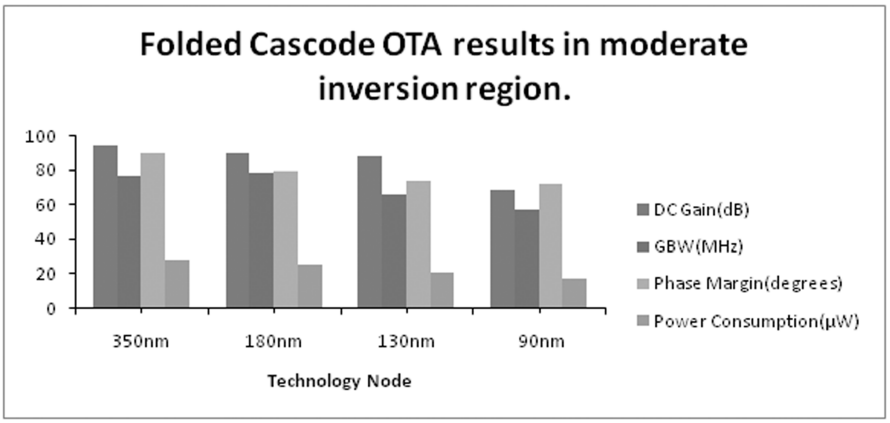

Figure 17: Comparison in moderate inversion region

4.4. Comparison of Class AB OTA with Folded OTA

After evaluating all the performance parameters of folded cascade OTA , it results has been compared with Class AB OTA as shown in Table 7.

Table 7
Comparison of Class AB OTA with Folded OTA

Parameter	*Class AB OTA*	*Folded Cascode OTA*
DC gain(dB)	68.67	78.56
GBW(MHz)	14.67	23.45
Phase Margin(Deg)	95.67	76.87
Power Consumption(nW)	378.78	119.89

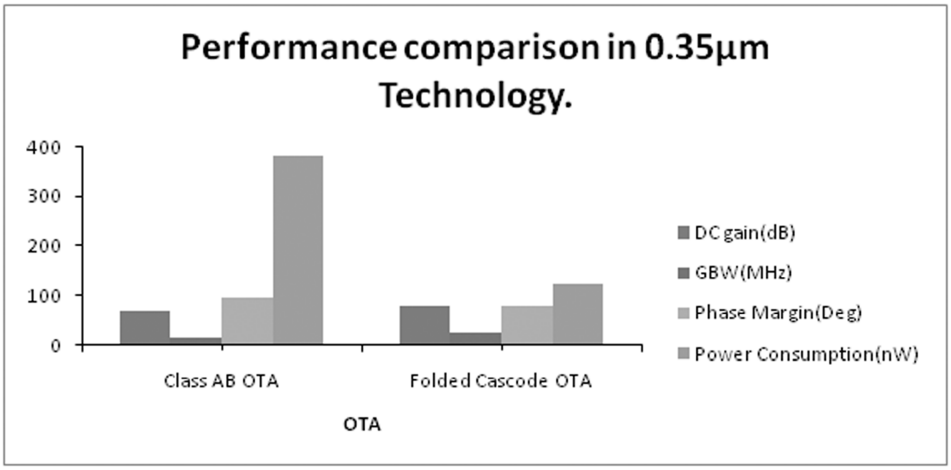

Figure 18:

5. CONCLUSION

Design of OTA is the important part in the design of analog circuits. It is designed and optimized in 0.35 μm CMOS technology.The main objective is to achievehigh gain and high bandwidth.In weak inversion region the gain of 77.56 dB with unity gain bandwidth of 18.56MHz with a supply voltage of 1Vhas been achieved, gain of 80 dB with a unity gain bandwidth of 440.05 MHzwith supply voltage of 2V in strong inversion region and gain of 94dB with unity gain bandwidth of 76.45MHz with a supply voltage of 2V in moderate inversion region by Gain Enhancement Technique. Noise rises up to 8.75mV at a cut off of 287.76MHz and then decreases at a point of 170.94μV in weak inversion region.Noise rises up to 122.26mV at a cut off frequency of 376.87MHz and then decreases at a point of 30.12mV in strong inversion region.Noise rises up to 93.46mV at a cut off frequency of 1.67MHz and then decreases at a point of 40.52mV in moderate inversion region. The comparison has been made based on different technology nodes i.e. 180nm, 130nm and 90nmas shown in Tables IV, V and VI.Table VII describes the performance comparison in 0.35μm technology of folded cascade OTA with Class AB operational transconductance amplifier.

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