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Three-Level Quasi-Z-Source Inverter using Multi-Carrier PWM Technique for PV Applications

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Abstract: This paper presents the 3Level-Neutral Point Clamped Quasi Z source inverters (NPC-QZSI) have been proposed as an alternative to power conversion concepts as they can both buck or boost the input voltage and also perform inverter operation. ZSI is single stage of conversion compare to conventional DC-DC boost converter with Voltage Source Inverter. In this paper, multi-carrier based modulation technique are used for 3L-NPC quasi Z-source inverter. In recent years, several modified control techniques have been proposed to control the quasi Z-Source inverter in an efficient way. Simulation is carried out in MATLAB and same circuit is implemented in hardware. The results of simulation and hardware are compared.

Keywords: Quasi Z-source Inverter, shoot through state, Non-shoot through state, Multi carrier PWM.

1. INTRODUCTION

Many industrial applications require high power converters which are now almost exclusively implemented using one of the multilevel types. For high power applications, multilevel converters offer many benefits which include an ability to synthesize voltage waveforms with lower harmonic content than two-level converters. The operation of multilevel converters at higher DC voltages using series connection of a basic switching cell of one type or another. Even though many different multilevel topologies have been proposed, the three most common topologies are the cascaded inverter, the diode clamped inverter, and the capacitor clamped inverter [1]. Among the three, the three-level diode clamped also known as the neutral point clamped (NPC) inverter has become an established topology in medium voltage drives and is arguably the most popular certainly for three-level circuits.

The quasi *z*-source concept can be applied to all DC-TO-AC, AC-TO-DC, AC-TO-AC and DC-TO-DC power conversion whether two-level or multilevel. In this paper, instead of several phase opposition and disposition

modulation techniques for a three-level neutral-point-clamped quasi impedance source inverter are discussed. The theoretical development is discussed in detail, and simulations as well as experimental results are used to verify the operation of the circuit with proposed sinusoidal-based modulation techniques [2]-[7].

The QZSI can buck and boost DC-link voltage in a single stage without additional switches. The QZSI can boost the input voltage by introducing a special shoot-through switching state, which is the simultaneous conduction (cross conduction) of both switches of the same phase leg of the inverter. This switching state is forbidden for traditional voltage source inverters because it causes a short circuit of the DC-link capacitors. Thus, the QZSI has excellent immunity against the cross conduction of the top and bottom-side inverter switches. The possibility of using shoot-through eliminates the need for dead-times without having the risk of damaging the inverter circuit. The input voltage is regulated only by adjusting the shoot-through duty cycle. In addition, the QZSI has a continuous mode input current which makes it especially suitable for renewable energy sources.

In the case of small loads and relatively low switching frequency the performance of QZSI is degraded. In these conditions the QZSI starts to work in discontinuous conduction mode, which causes an over-boost effect and leads to instabilities.

This paper is organized as the introduction is explained in section I. Then the proposed system is explained in section II. Then the results and discussion is presented in section IV and the conclusion in section V.

2. PROPOSED SYSTEM

This paper presents a three-level neutral-point-clamped quasi-Z-source inverter in the single-stage buckboost multilevel inverter family. The three-level neutral-point-clamped quasi-Z-source inverter was derived by combining the properties of the quasi-Z-source network with those of a three-level neutral point clamped inverter. This paper presents a steady state analysis of the topology along with a special modulation technique to distribute shoot-through states during the whole fundamental period. A new converter combines the advantages of the two topologies of continuous and discontinuous conduction mode. But at the same time shoot-through switching state demands new approaches to modulation techniques in order to combine the boost factor, lower input current ripple and more capacitor voltage balance with the best possible output voltage quality. This paper is devoted to the simulation of different shoot through sinusoidal PWM techniques for the 3L-NPC QZSI that allows 50 Hz to be obtained as an output voltage frequency.



Figure 1: Proposed Circuit Diagram of Three level NPC quasi ZSI

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The operation of each inverter phase leg of a traditional NPC inverter can be represented by three switching states P, O and N. Switching state "P" denotes that the upper two switches in a phase leg are gated ON, "N" indicates that the lower two switches conduct, and "O" signifies that the inner two switches are gated ON. However, each phase leg of the Z-source NPC inverter has three extra switching states which resemble the "O" state of the traditional NPC inverter. These extra switching states occur when all the four switches in any phase leg are gated ON [full shoot- through (FST)], or the three upper switches in any phase leg are gated ON [upper-shoot-through (UST)] or the three bottom switches in any phase leg are gated ON [lower shoot-through (LST)]. These shoot-through states are forbidden in the traditional NPC inverter because they would cause a short circuit of the dc-side capacitors. Again, the Z-source network makes these shoot-through states permissible and provides the boost operation [8]-[12].



Figure 2: Sketch of the Proposed multi-carrier modulation technique for three level NPC quasi ZSI

3. SIMULATION RESULTS

The simulation is carried out in MATLAB/Simulink. The simulation circuit is shown in Figure 3 and PWM generation circuit is presented in Figure 4. The output phase voltage without filter and with filter are shown in Figure 5 and 6 respectively.

4. EXPERIMENTAL SETUP

The proposed modulation technique is implemented in PIC 16F877A controller. This controller is widely used in experimental and modern applications because of its low price, high quality, wide range of applications and easily available in the market. PIC16F877 has 5 basic input/output ports. They are usually denoted by PORT A (R A), PORT B (RB), PORT C (RC), PORT D (RD), and PORT E (RE). These ports are used for input/output interfacing. In this controller, PORT Ais only 6 bits wide (RA-0 to RA-7), PORT B, PORT C and PORT D are only 8 bits wide (RB-0 to RB-7, RC-0 to RC-7, RD-0 to RD-7), PORT E has only 3 bit wide (RE-0 to RE-7).

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Figure 5: Output voltage of the inverter without filter

The following steps should be taken when configuring the CCP module for PWM operation:

- Set the PWM period by writing to the PR2 register.
- Set the PWM duty cycle by writing to the CCPR1L register and CCP1CON<5:4> bits.
- Make the CCP1 pin an output by clearing the TRISC<2> bit.
- Set the TMR2 prescale value and enable Timer2 by writing to T2CON.
- Configure the CCP1 module for PWM operation.

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Figure 6: Output voltage of the inverter with filter

The PWM outputs from PIC controller is not enough to drive the MOSFET switch, hence it is given to the driver circuit. The output from the driver circuit is 12V pulses, these pulses are applied to MOSFET (IRFP250N) switches of the Z-Source inverter[13]-[14].

Figure 7 represents the driver circuit for the inverter switches and figure 8 and 9 shows the hardware setup and output voltage of the quasi Z-Source inverter without filter respectively.





5. CONCLUSION

In this paper, multi-carrier based PWM technique for the quasi Z-source three level inverters has been developed and simulation results are presented. This modulation technique gives better performance and behavior because the shoot-through states are uniformly distributed and with constant width during the whole output voltage period and the average output voltage is compensated through the displacement of the carriers. The designed value of

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inductor and capacitor in shoot through mode input DC of 30 V is inverted and boosted to 120 V in single stage. The same circuit is implemented in hardware.



Figure 8: Hardware setup of proposed system



Figure 9: Three level output from Inverter

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