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An Improved Topology Based Multilevel Inverter Implementation Using Solar Power

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ABSTRACT

In this paper, an existing topology of Multilevel Inverter with a reversing-voltage component has been extended to enhance the multilevel performance. This topology requires lesser number of components compared to existing inverters ,particularly at higher levels using fewer carrier signals and driving devices. Thus, giving the advantage of reduction in cost and complexity particularlyfor higher output voltage levels. This paper concentrates on electricity from renewable energy systems like solar energy. This paper also focus on Photo Voltaic (PV) power system for multilevel inverter.Seven level proposed MLI is simulated using Matlab/Simulink environment and the corresponding results are presented in this paper.

Index Terms: MLI, SPWM,PV system

I. INTRODUCTION

The peculiar nature of multilevel inverters [MLI] lies in generating waveforms with better harmonic spectrum and with less THD[1]. When compared with the conventional power conversion aspect, this approach is more improved and advantageous. The higher power quality waveforms are produced by smaller voltage steps thus reducing voltage (*dv/dt*) stress on the load and also electromagnetic compatibility concerns[2].

The important factor allowing semiconductors to be operated at higher voltages is their series type connection. Even so, the series connection is done typically with clamping diodes, which removes over voltage problems.

The more number of semiconductor switches required is a flaw regarding multilevel power conversion.The lower voltage rated switches can be used in the multilevel converter and, therefore, the active semiconductor cost is not appreciably increased when compared with the two level cases. Another disadvantage of multilevel power converters is that the small voltage steps are typically produced by isolated voltage sources or a bank of series capacitors. Isolated voltage sources may not always be readilyavailable, and series capacitors require voltage balancing[3].

Cascaded H-bridge MLIs are mostly preferred for high power applications as the regulation of the DC bus is simple[4]. But it requires separate dc sources and also the complexity of the structure is increases as the level predominantly increase.

In the context of power consumption, the use of the conventional energy sources are limited and can be exhausted. Many renewableenergy sources are existing such as solar, wind, biomass,hydro, geothermal and ocean power.Among them, PV has the advantage of clean and no pollution, and thus provides remedy to the problems of conventional energy sources.The basic element of a PV system is the solar cell. A solar cell directly converts the energy of sunlight directly into electricity in the form of dc.A typical PV cell consists of a p-n junction formed in a semiconductor material similar to a diode. The PVsystems whichhas multiple applications [5] also provide solution for voltage balancing in the multilevel conversion.

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Some earlier approaches required less dc supplies by inserting transformer instead of them[6]. The main disadvantage of the approach is adding so many transformer windings which will add up to the overall volume and cost of the inverter. The proposed topology is asymmetrical topology since all the values of all voltage sources need not be equal. The topology we are proposing here does not require steady state amplitude to achieve the required voltage levels. In conventional inverters, voltage levels are acquired through algebraic sum of source voltages. PV system performs voltage level acquisition with the help of Voltage regulatorsIt is also more efficient since the inverter has a component which operates the switching power devices at line frequency. Therefore, there is no need for all switches to work in high frequency which leads to simpler and more reliable control of the inverter.

This paper describes the general multilevel inverterschematic in single phase. A general method of multilevel modulation phase disposition (PD) SPWM is utilized to drive the inverter and can be extended to any number of voltage levels.

II. PROPOSED TOPOLOGY

(A) General Description

The proposed topology is a hybrid approach which separatesthe output voltage into two major parts. One part is named *Level Generation* which is responsible for level generating in positive polarity. This part requires high-frequency switching capability togenerate the required voltage levels. The second part called *Polarity Generation*, is responsible for generating the polarity of the output voltage. This is the low-frequency part operating at line frequency.

The topology combines the twoparts to generate the multilevel voltage output. In order to generate a complete multilevel output, the positivelevels are generated by the high-frequency part (level generation),andthe result is fed to a full-bridge inverter (polarity generation), which will generate the required polarity for theoutput. This will avoid use of many semiconductor switcheswhich were needed to generate the output voltage levels in positive and negative polarities.

It consists of a one H-bridge inverter and ‘N’ number of cascaded cells, which are having a dc rating of Vdc. The number of levels can be given by the formula:

$$\text{Number of Levels } L = [2n + 1]$$

Where n= Number of cells excluding the H-bridge. For generating +Vdc we need turned on switches S7 and S10, for -Vdc, switches S8 and S9 has to be turned ON, and for zerovoltage either switches S7 and S10 or switches S7and S9 has to be turned ON.

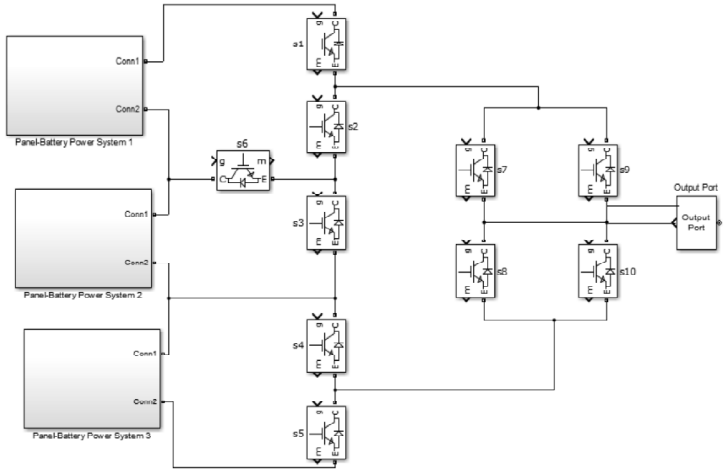

Figure 1: Schematic of a seven-level inverter in single phase

This topology in seven levels requires ten switches and three isolated sources. The principal idea of this topology as a multilevel inverter is that the left stage in Fig. 1 generates the required output levels without any polarity and the right circuit (full-bridge converter) decides about the polarity of the output voltage. It transfers the required output level to the output with the same direction or opposite direction according to the required output polarity. It reverses the output voltage direction only when the voltage polarity requires to be changed for negative polarity.

This topology can be easily extended to higher voltage levels by duplicating the middle stage of Fig. 1..It can also be applied for three-phase applications with the same principle. This topology uses isolated supplies from the PV array. Therefore, it does not face voltage-balancing problems due to fixed dc voltage values. In comparison with a cascade topology, it requires justone-third of isolated power supplies used in a cascade-type inverter.

This topology requires half of the conventional carriers for SPWM controller. SPWM for seven-level conventional converters consists of six carriers, but in this topology, three carriers are sufficient.The topology we describe does not need fast switches for the polarity generation part. In the following sections, the superiority of this topology with respect to PWM switching and number of components is discussed.

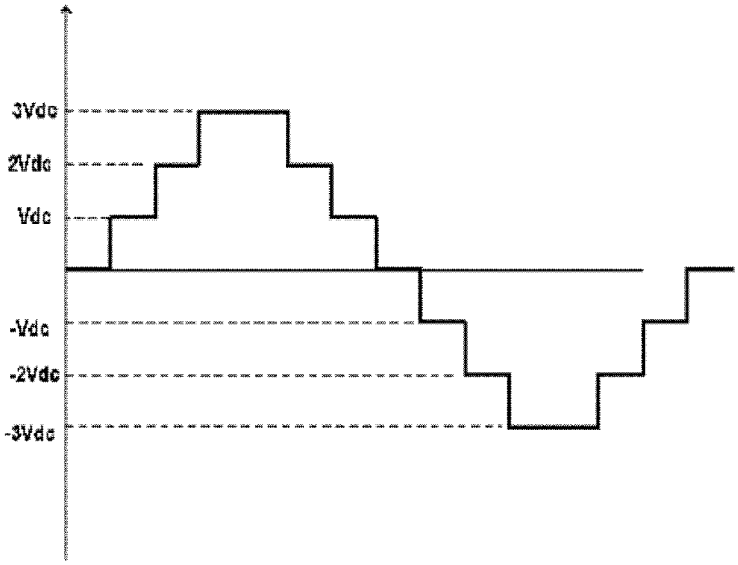

Figure 2: Ideal seven-level output waveform

(B) Switching Sequences

According to the proposed approach, it does not need to generate negative pulses for negative cycle control. Thus, there is no need for extra conditions for controlling the negative voltage. Instead, the reversing full-bridge converter performs this task, and the required level is produced by the high-switching-frequency component of the inverter. The voltage level is transformed to negative or positive according to output voltage requirements.

Table I
Switching Sequences for Each Level

Level	*0*	*1*	*2*	*3*
Mode 1	2,3,4	2,3,5	1,4	1,5
Mode2		2,4,6	2,6,5	

Different switching modes in generating the required levels for a seven-level inverter are shown in Table I. In Table I, the numbers show the switch according to Fig. 1 which should be turned on to generate

the required voltage level. According to the table, there are six possible switching patterns to control the inverter. It shows the great flexibility of the topology. However, as the PV system is externally adjustable through voltage regulators, there is no need for voltage balancing for this work.

In order to avoid unwanted voltage levels during switching cycles, the switching modes should be selected so that the switching transitions become minimal during each mode transfer. This will also help to decrease switching power dissipation.In this topology, the sequences of switches (2–3-4), (2-3-5), (2-6-5), and (1, 5) have been chosen for levels 0 up to 3, respectively. These sequences are shown inFig. 3. As can be observed from Fig. 3,the output voltage levels are generated in this part byappropriate switching sequences. The final output-voltage level is the sum of voltage sources, which are included in the current path that have marked in bold sequence.

In order to produce seven levels by SPWM, three saw-tooth waveforms for carrier and a sinusoidalreference signal for modulator are required as shown in Fig. 4.In this paper, PD SPWM is adopted for convenience.

Carriers in this method have unique values and they have definite offset from each other. They are in phase with each other.

According to Fig. 4, three states are considered. The first state occurs when the modulator signal lies between zero and the lowest carrier. The second state occurs when it is within the middle carrier. Finally, the third one is when the signal is within the highest carrier.

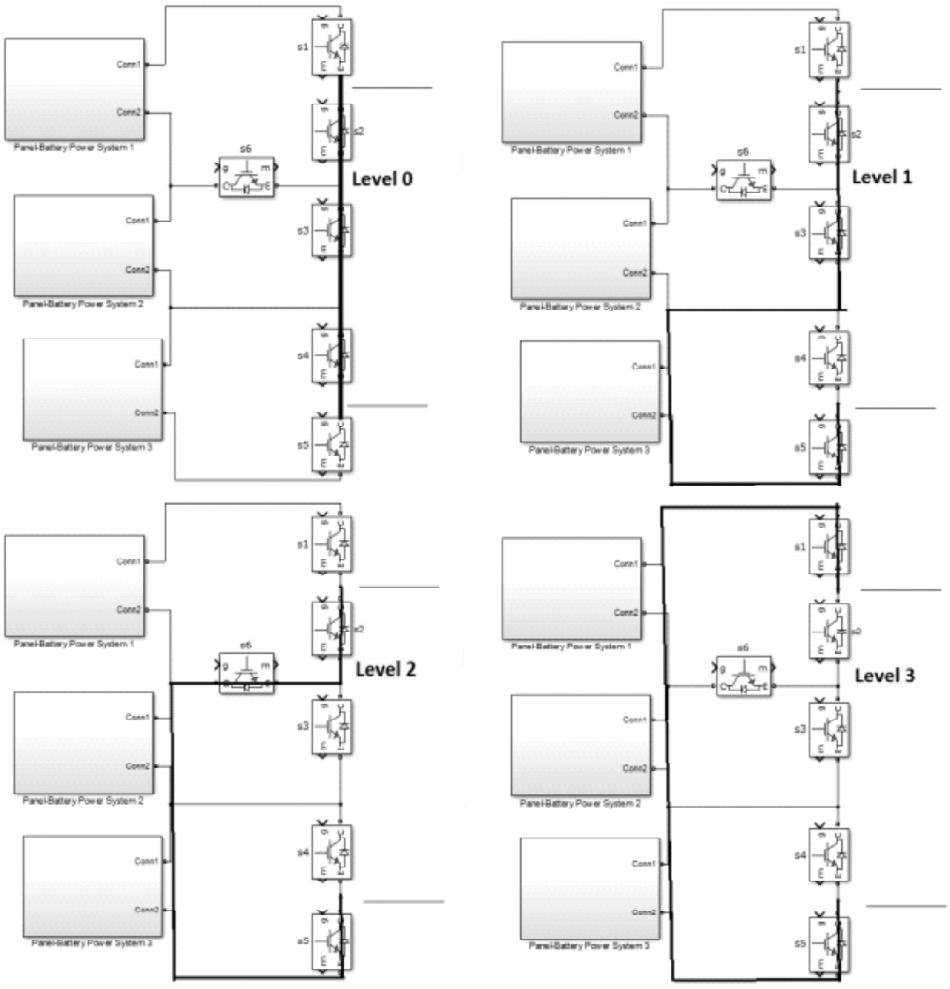

Figure 3: Switching sequences for level generation

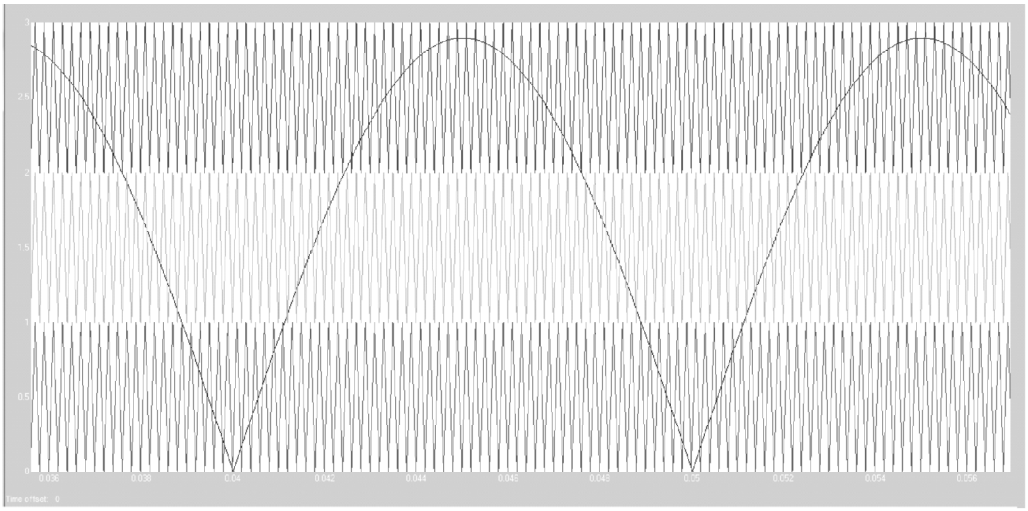

Figure 4: SPWM Carrier and modulator

In each state, some switching patterns are adopted to cover the voltage requirements. According to this definition, the switching states and switching modes are described in Table II.Table II shows the relation between the right comparator output according to the current state and required states forswitching to meet the voltage requirements.

Table II
Switching Cases for Each Comparator Output

States	*One*		*Two*		*Three*	
Compare	+	-	+	-	+	-
Mode	2-3-5	2-3-4	2-5-6	2-3-5	1-5	2-5-6

As illustrated in Table II, the transition between modes in each state requires minimum replacement of switches to improve the efficiency of the inverter during switching states.The number of switches in the path of conducting current also plays an important role in the efficiency of overall converter. However ,the numberof switches which conduct current in the proposedtopology ranges from four switches (for generatinglevel 3) to five switches conducting for other levels, while two of the switches are from the low-frequency (polarity generation) component of the inverter.Therefore, the number of switches in the proposed topology that conduct the circuit current is lower than that of the cascadeinverter[7], and hence, it has a better efficiency.

The same calculation is true in a topology mentioned in [8]. The least number of switches in the current path for a seven-level inverter according to is five (for generating level 3), which requires one switch more in the current path compared to thistopology which requires only four conducting switches. These switching sequences can be implemented by logicgates or DSP. The signal stage should be isolated from thepower stage by optocouplersfor control circuit protection.The drive circuit is also responsible to generate the dead timebetween each successive switching cycle across the dc-source.

The gating signal for the output stage, which changes the polarity of the voltage, is simple. Low-frequency output stage is an H-bridge inverter and works in two modes: forward and reverse modes. In the forward mode, switches 8 and 9 as inFig. 1 conduct, and the output voltage polarity is positive.However, switches 7 and 10 conduct in reverse mode, which will lead to negative voltage polarity in the output. Thus, thelow-frequency polarity generation stage only determines the output polarity and is synchronous with the line frequency.

Using PWM, highfrequency switches can be adopted in this stage based on the required frequency and voltage level. However, low-frequency polarity generation part drive signals are generated with the line frequency (50 Hz), and they only change at zero-voltage crossings.

III. SIMULATION RESULTS

The following Fig. 5 and 6 shows the Matlab/Simulink diagram of proposed seven level MLI and its output voltage wave form.

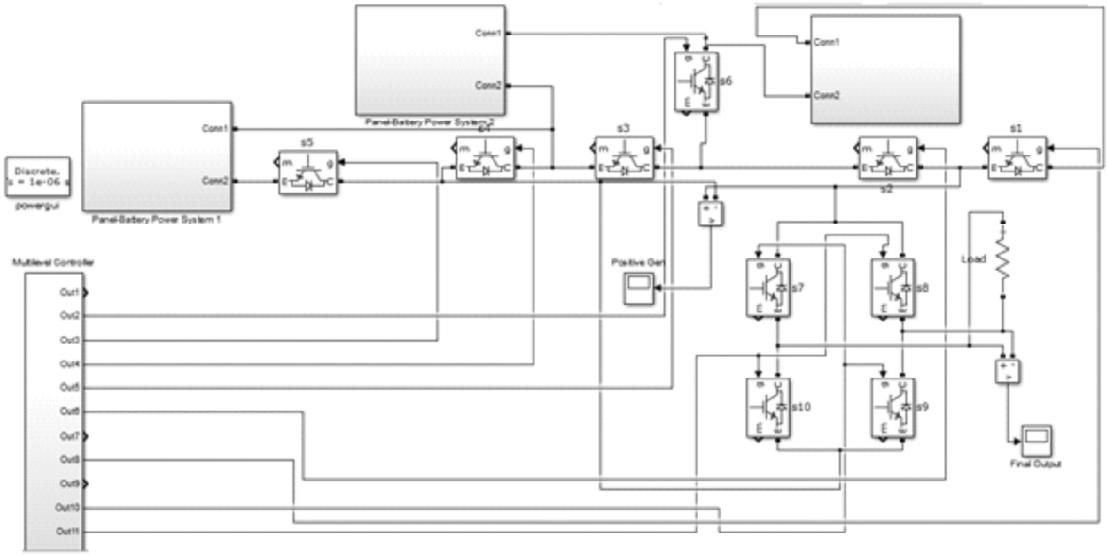

Figure 5: Matlab/Simulink diagram of proposed seven level MLI

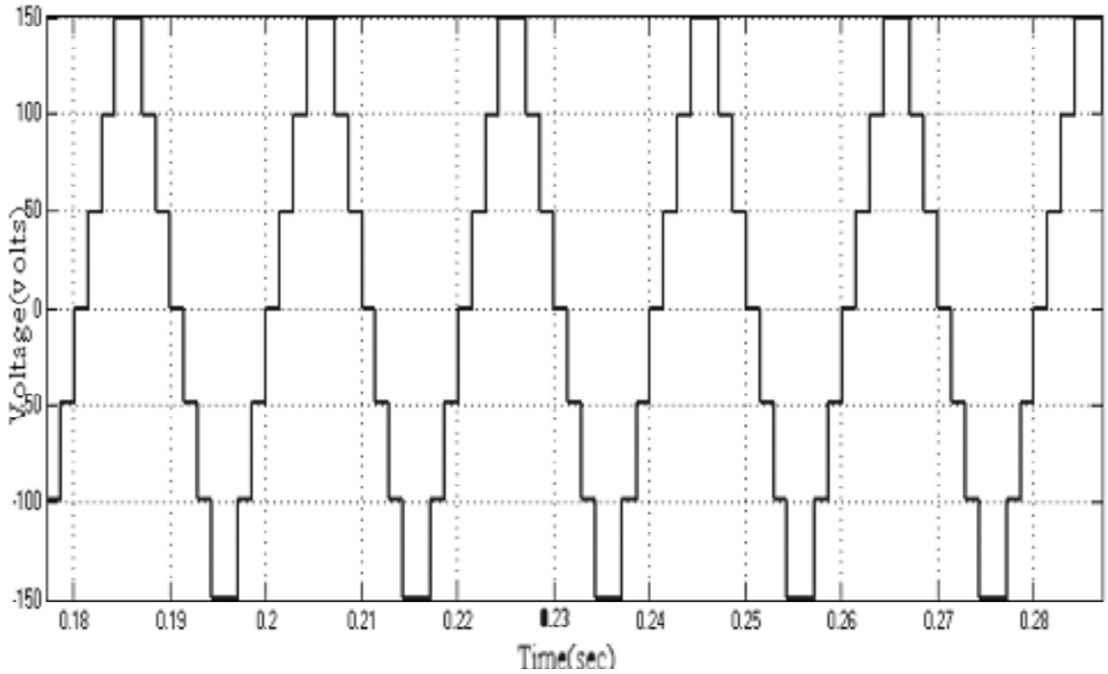

Figure 6: Proposed seven level inverter output voltage

From Fig. 6, it is observed that the output voltage of proposed MLI has seven levels with seven switches.The following Fig.7 shows the spectrum analysis of seven level output voltage.

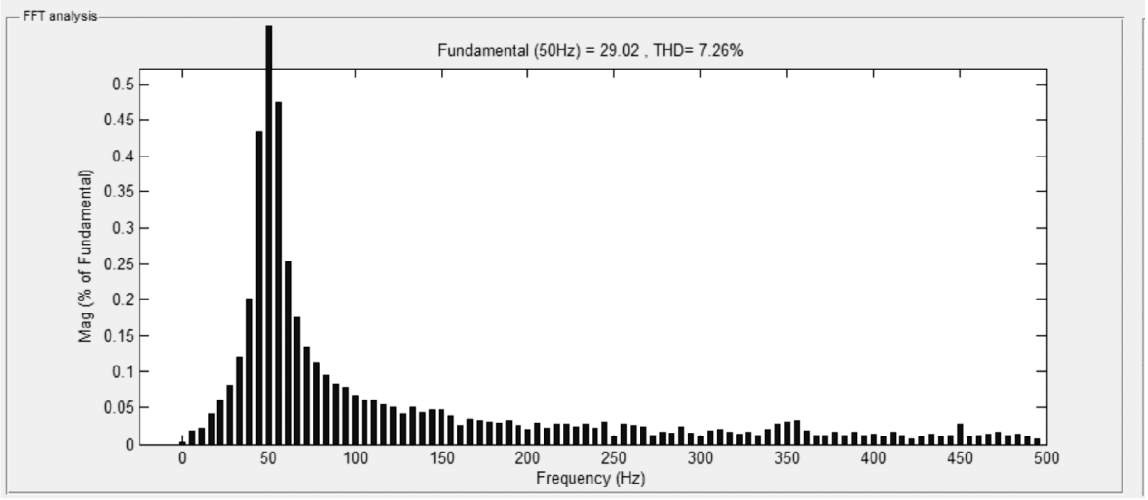

Figure 7: FFT analysis

From Fig. 7, the THD of the proposed seven level inverter is 7.22%.

IV. DISCUSSION

Conventionally, High-frequency switches and diodes are expensive and are more prone to be damaged than low-frequency-switches.

Based on the studies on this context, the reliability of a system is indirectly proportional to the number of its components. Therefore, as the number of high-frequency-switches is increased, the reliability of the converter is decreased. In this converter, as can be seen, half of the switches in the full-bridge converter will not require to be switched on rapidly since they are only switched at zero crossings operating at line frequency (50 Hz). Thus, in this case, the reliability of the converter and also related expenses are highly improved.

The number of required single phase components according to output voltage levels is illustrated in Table III [9].

It can clearly be inferred that the number of components of the proposed topology is lower than that of other existing topologies even more so as the voltage levels increase and it will decrease tremendously with higher voltage levels.

Table III
Comparison Between Different Topologies

Topology	*Number of switches for 7-level*	*Number of switches for 13-level*
Diode clamped MLI	12	24
Flying Capacitor MLI	12	24
Cascaded H-Bridge MLI	12	24
Proposed MLI	7	10

Checking the solar power concerns, PWM allows sources to be charged at constant level. Automatic reconnection of circuitry is prevented through Islanding protection between the sources.Considering the long term usage, solar power resources are cheap, with less maintenance occurrences. The net energy consumption is also reduced substantially.

V. CONCLUSION AND FUTURE WORK

In this paper, an existing inverter topology has been modified with enhanced features in terms of the required power switches and isolated dc supplies, control requirements, cost, and reliability. It is shown that this topology can be a good contribution for converters used in power applications such as FACTS, HVDC, PV systems, UPS, etc.[10]It can be implemented for systems that require uninterrupted high voltage power supply, as in Biomedical processes (Eg: MRI Scan).

In the mentioned topology, the switching operation is separated into high- and low-frequency parts. This will add up to the efficiency of the converter as well as reducing the size and cost of the final prototype. The PD-SPWM control method is used to drive the inverter.[11] The PWM for this topology has fewer complexities since it only generates positive carriers for PWM control. The simulation results of the seven-level inverter of the proposed topology are demonstrated in this paper. The results clearly show that the proposed topology can effectively work as a multilevel inverter with areduced number of carriers for PWM.

The proposed Inverter can be used to integrate the Photovoltaic system into Grid,[12] with satisfying the grid requirements such as phase angle, frequency and amplitude of the Grid voltage [13].

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