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Realization of Energy-Efficient and High-Speed 64-bit Carry Skip Adder under a Wide Range of Supply Voltages

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ABSTRACT

The main objective of the project is to design a 64-bit carry skip adder which is having high speed and lower power consumption when compared to CSKA. To improve speed which will be achieved by applying concatenation and incremenation structure to increase the efficiency of the existing cska structure. In the existing cska, instead of using multiplexer logic, the concatenation and incrementation structure makes use of AND-OR-Invert (AOI) and OR-AND-Invert (OAI) compound gates for the skip logic. *The carry skip adder structure is realized with both fixed and variable stage sizes where the delay is decreased, and speed is improved.* Hence, a hybrid variable latency extension of the concatenation and incrementation structure, which decreases the power consumption without considerably changing the speed. The results are obtained using CADENCE TOOL and the power, area and delay was lowest among all the structures.

Indexing Terms: Carry skip adder (CSKA), fixed stage size, variable stage size, High performance, hybrid variable latency adders.

1. INTRODUCTION

In designing digital IC's additional operations are the high essential and frequent. Adders are the main blocks in arithmetical, logical and DSP processing units and hence increasing their speed is very helpful in reducing their power/energy. Consumption strongly affect the speed and power of processor. The performance of a design will be often limited by the efficiency of its adders. One of the effective technique is to decrease the power consumption of digital circuits is to reduce the voltage supplydue to the switching energy on the voltage.

In existing method, it will use multiplexer logic in which the number of gates, power consumed by the carry skip adder are more and critical path delay is high. The ripple carry adder is constructed by using cascading of full adders (FA) blocks in series. One full adder is responsible for the addition of two binary digits of all stages of the ripple carry. The carry-out of one stage is fed directly to the carry-in of the next stage. The carry is generated in a serial computation and delay is high as the number of bits are increased in RCA.

The main contribution of the project is summarized as follows.

1) Proposing a modified CSKA structure by adding the concatenation and incrementation Schemes to the existing cska structure for improving the speed and energy efficiency of the adder. The modification provides the AOI/OAI logical gates instead of the multiplexer logic.

2) Constructing an improved CSKA structure based on analytical expressions presented to find the critical path delay.

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3) The hybrid variable latency Carry Skip Adder is based on the extension of the proposed CSKA which was replaced in the middle stages by using parallel prefix network structure.

2. DESIGN CONSIDERATIONS

The Carry Skip Adder can be designed by using Fixed and Variable Stage Sizes where the higher speed is achieved in Variable Stage Size structures.

Fixed Stage size Carry Skip Adder

The critical path delay of a Fixed Stage Size CSKA is calculated by

$$T_D = [M \times T_{CARRY}] + \left[\left(\frac{N}{M} - 1\right) \times T_{MUX}\right] + [(M-1) \times T_{CARRY} + T_{SUM}]$$

The maximum value of M (M_{opt}) that leads to minimum propagation delay can be calculated as $(0.5N\alpha)^{1/2}$

Where α is equal to T_{MUX}/T_{CARRY}.

$$T_{D,opt} = \sqrt[2]{2NT_{CARRY}\,T_{MUX}} + (T_{SUM} - T_{CARRY} - T_{MUX})$$

$$= T_{SUM} + \left(\sqrt[2]{2N\alpha} - 1 - \alpha\right) \times T_{CARRY}$$

Thus the maximum propagation delay ($T_{D,opt}$) is obtained and the maximum delay of the FSS CSKA is almost proportional to square root of the product of N and α.

Variable Stage size Carry Skip Adder

By applying variable stage sizes, the speed of the CSKA is improved. These delays are reduced by lowering its size of the first and last RCA blocks. For instance, the primary RCA block size is set to one, whereas sizes of the following blocks may vary.

The critical path delay of a Variable Stage Size CSKA is formulated by

$$T_{PD,opt} = T_{CARRY} + \left(\sqrt[2]{\frac{N}{\alpha}} - 1\right) T_{SKIP} + T_{SUM}$$

3. CONCATENATION AND INCREMENTATION CSKA STRUCTURE

The structure is based on adding the concatenation and the incrementation structures which includes the ripple carry adder structure with the AOI and OAI logical gates for skip operation. The operation replaces 2:1 multiplexers by AOI/OAI logical gates. The skip logic reduces the number of gate count in the structure. The speed of the structure is achieved by using skip logic and the delay is reduced. In addition, except the primary RCA block the carry input for remaining blocks is always zero, and hence, for these blocks the first adder acts as a half-adder. $(Q - 1)$ FAs in the basic structure are replaced with the same number of half adders in the concatenation and incrementation structure decreasing the area.

Figure 1. Shows the adder contains two 64 bits inputs, A and B, and 4 stages. Each RCA block which is having the size of Mj (j = 1,2,3,4). In this structure, the carry input for Ci, is one and remaining RCA blocks are zero are calculated in parallel which is known as concatenation.

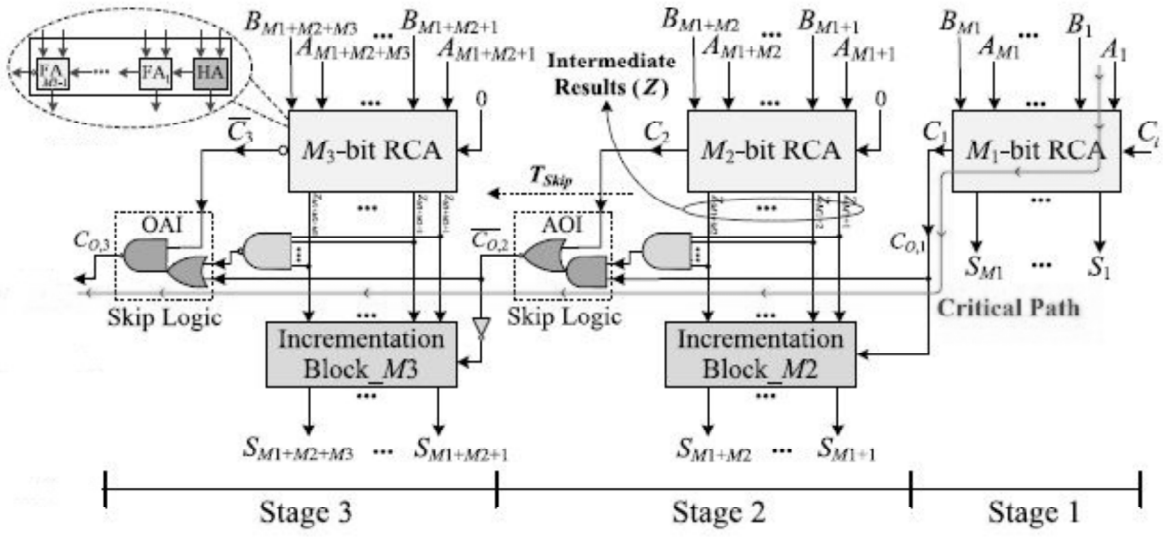

Figure 1: Concatenation and incrementation CI-CSKA Structure

The stages 2 to 4 which containing two blocks of RCA and incrementation. The incrementation block uses intermediate results which are obtained by using RCA block and the carry output of the previous stage is calculated through the final addition of the stages. The internal structure of the incrementation block containing a chain of half-adders (HAs), is as shown in figure 2.

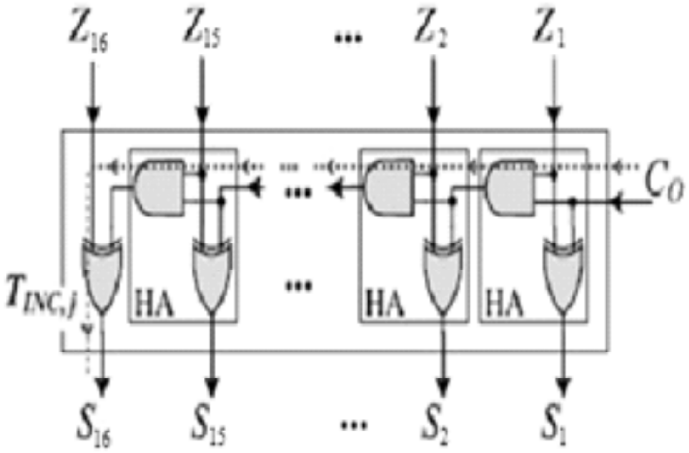

Figure 2: Internal Structure of Incrementation Block

In addition to reduce the delay, the carry output of the incrementation block should not be used. The incrementation contains chain of half adders. The carry input is directly into the structure and it performs the operations are unique to the half adder.

4. CONCATENATION AND INCREMENTATION HYBRID VARIABLE LATENCY CSKA

The concatenation and incrementation design of hybrid variable latency adder uses the voltage scaling depending on adaptive clock stretching. This structure based on the CI-CSKA structure. To provide the variable latency option for the Variable Stage Size CSKA structure, we replace the middle stages with a Parallel Prefix Adder which is modified. The basic idea in variable latency adders is that the critical paths of the adders are switched rarely. Hence, the voltage supply may be scaled down without lowering the clock frequency. Hence, in this structure, the time between the critical paths and the longest critical paths determines the optimum amount of the voltage supply scaling.

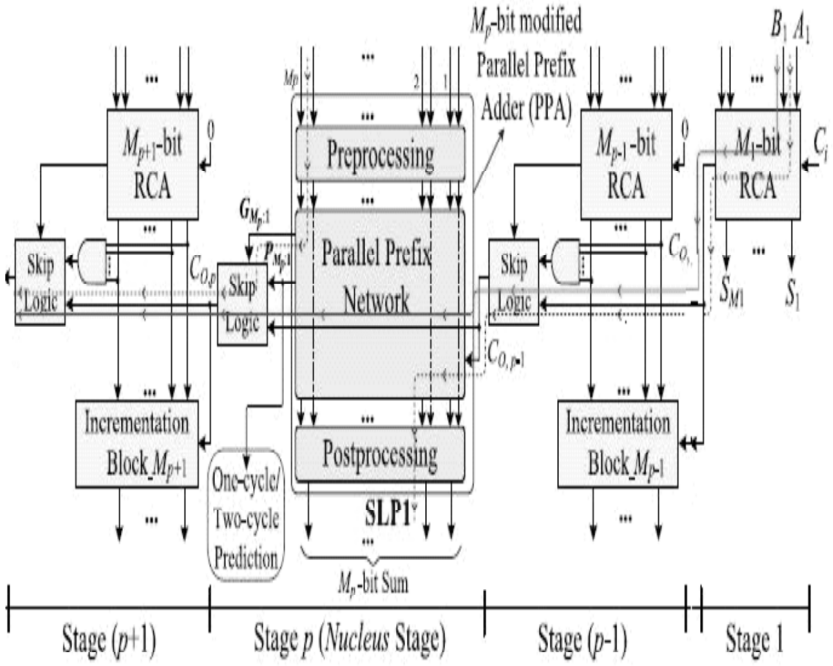

Figure 3: Concatenation and incrementation hybrid variable latency CSKA Structure

The sub-threshold current is the main discharge component in off devices which exponentially dependence on the voltage supply level in the drain-induced barrier lowering effect. Depending on the amount of the voltage supply reduction, the working of ON devices may depend on the super-threshold,

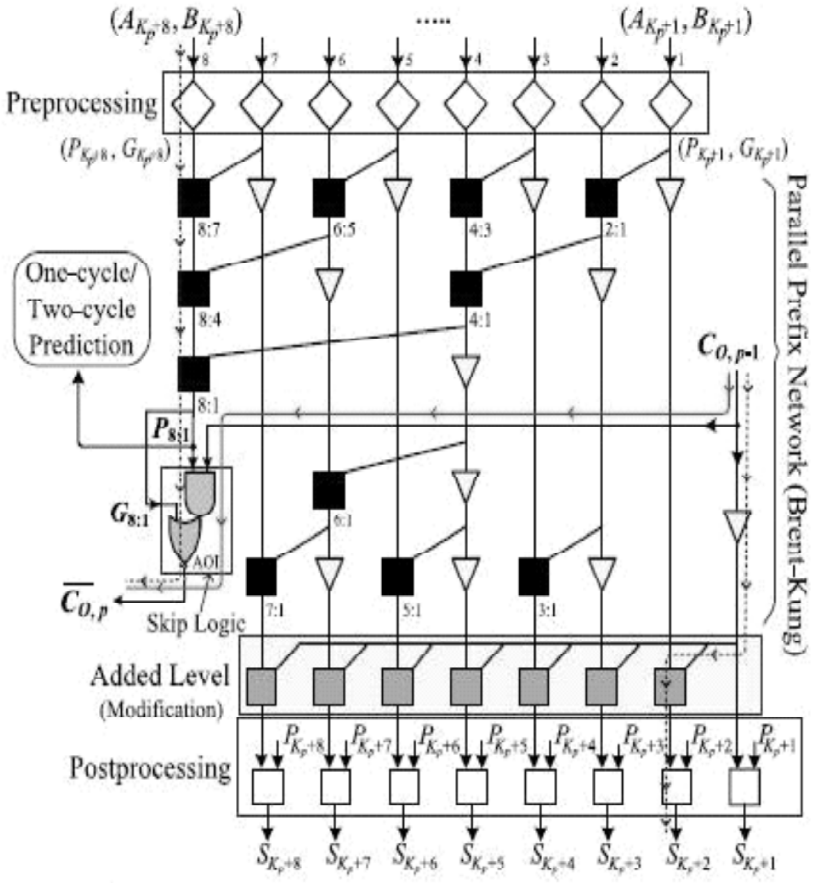

Figure 4: Internal Structure of Concatenation and incrementation hybrid variable latency CSKA Structure

near-threshold, or sub-threshold regions. The super threshold region generates the lower delay, higher switching and leakage powers when compared to near/sub threshold regions. In this region, the delay and leakage power totally dependent on the supply and threshold voltages.

In the hybrid structure, the PPA network which is generated by Brent–Kung adder is utilized. The main advantage of this adder when compared with prefix adders is to calculate forward paths and the longest carry. In addition, the fan-out of adder is less than various parallel adders, while the length of its wiring is smaller. One of the improved technique is to reduce the power consumption of digital circuits which are used to reduce the voltage supply due to switching energy on the voltage.

5. SIMULATION RESULTS

The design concatenation and incrementation in this paper has been developed using cadence tool. Adders are key building blocks in arithmetic and logic units (ALUs). All the adders are designed with 64 bit. The simulations were performed using Encounter (Cadence tool). we evaluate the efficiencies of the concatenation and incrementation structures by comparing their delay, power, energy, and area of different adders.

The concatenation and incrementation CI-CSKA structure slightly reduces the area when compared to existing carry skip adder. In addition to this, the number of transistors in the concatenation and incrementation CSKA structure are smaller than the Existing cska structure in both Fixed and Variable Stage Sizes. It has the lower energy and less area in the concatenation and incrementation CSKA structure. As the results shows the highest power, area and delay are decreased.

The performance of the concatenation and incrementation hybrid variable latency CSKA structure is compared with n-variable latency adders.

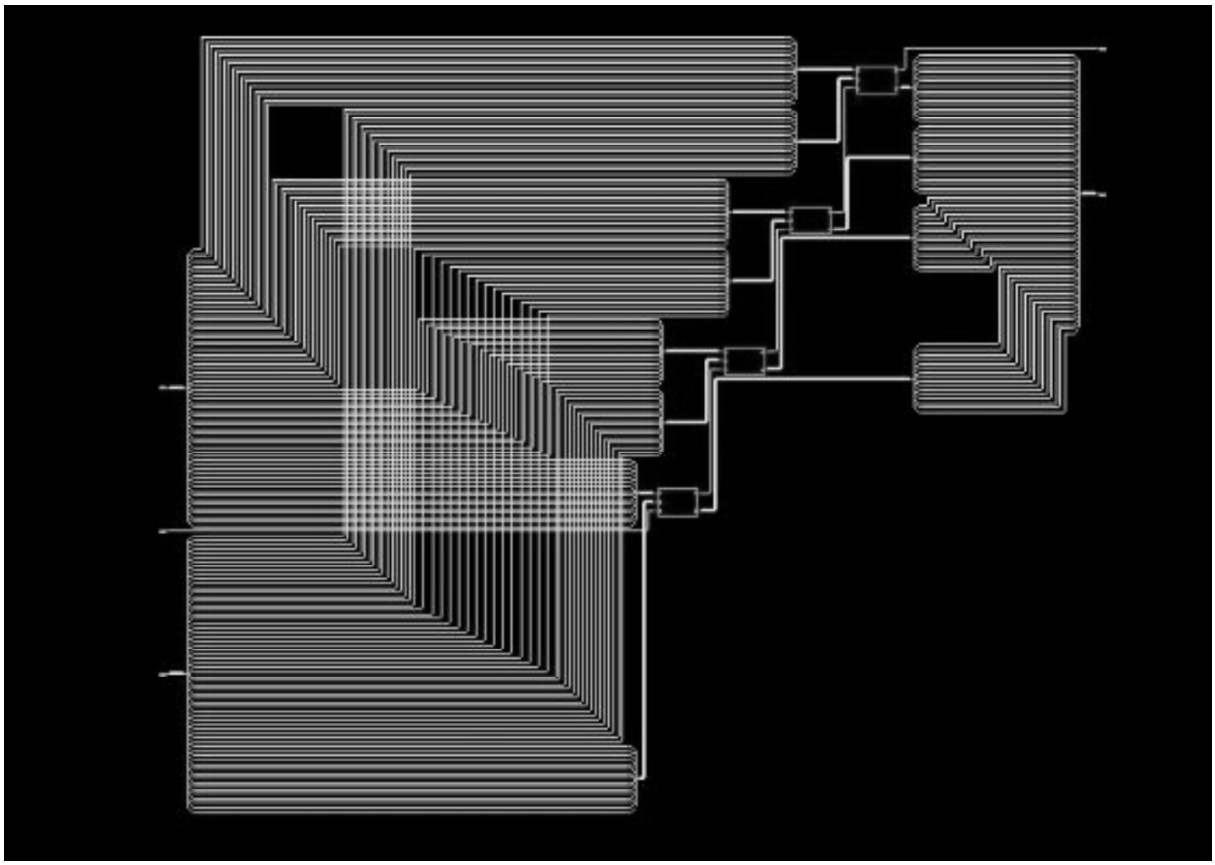

Figure 5: Gate level net-list of conventional carry skip adder

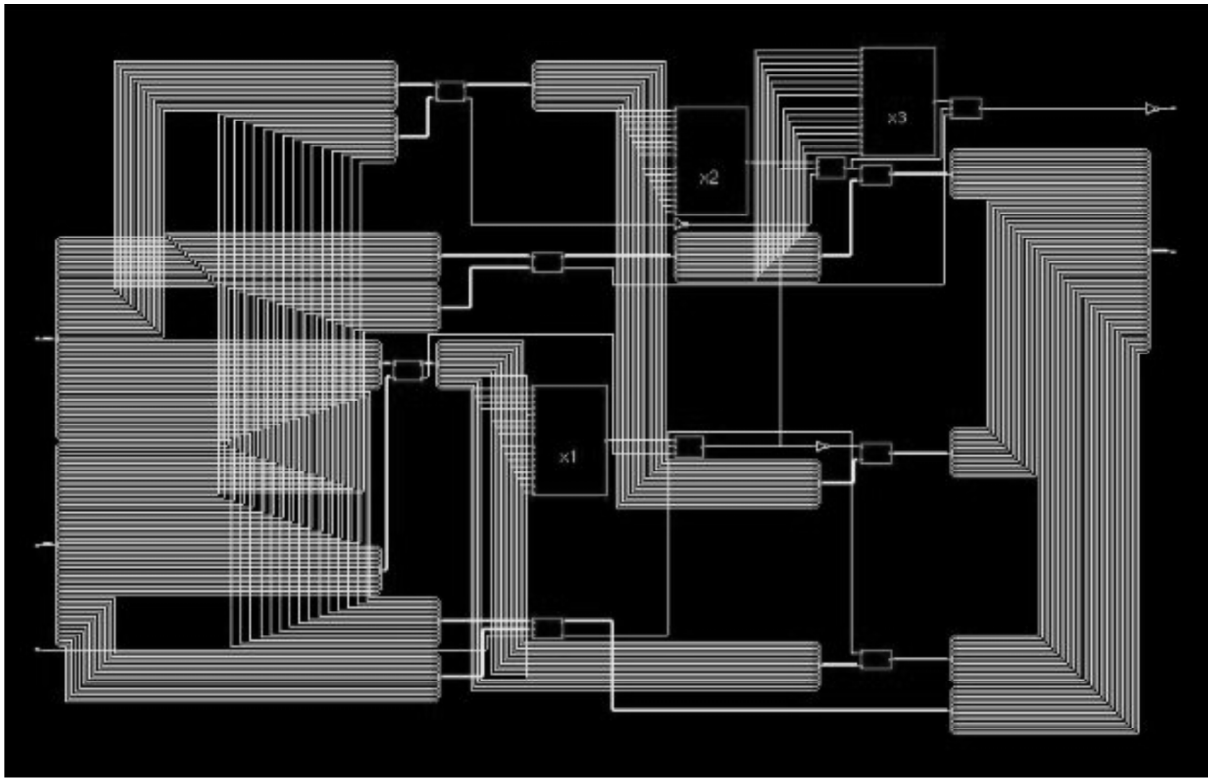

Figure 6: Gate level net-list of concatenation and incrementation carry skip adder

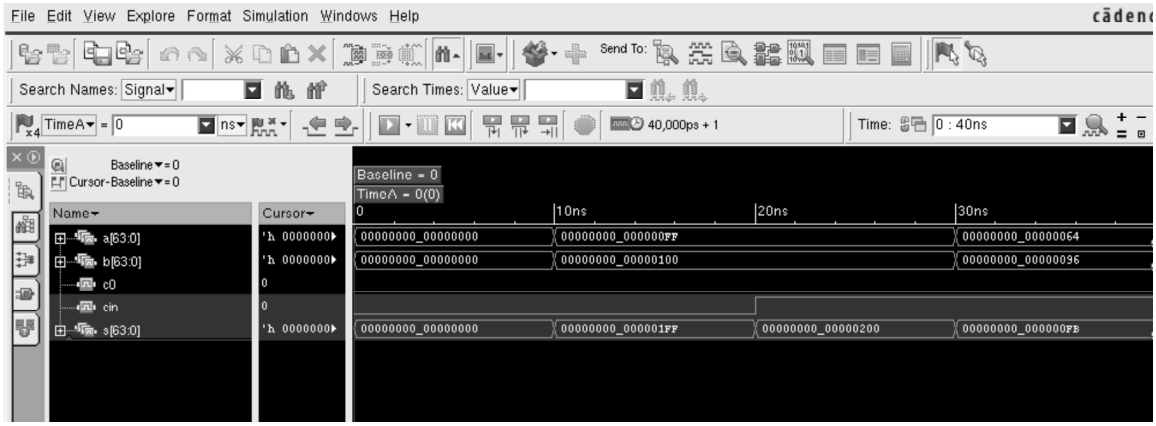

Figure 7: Output of conventional carry skip adder

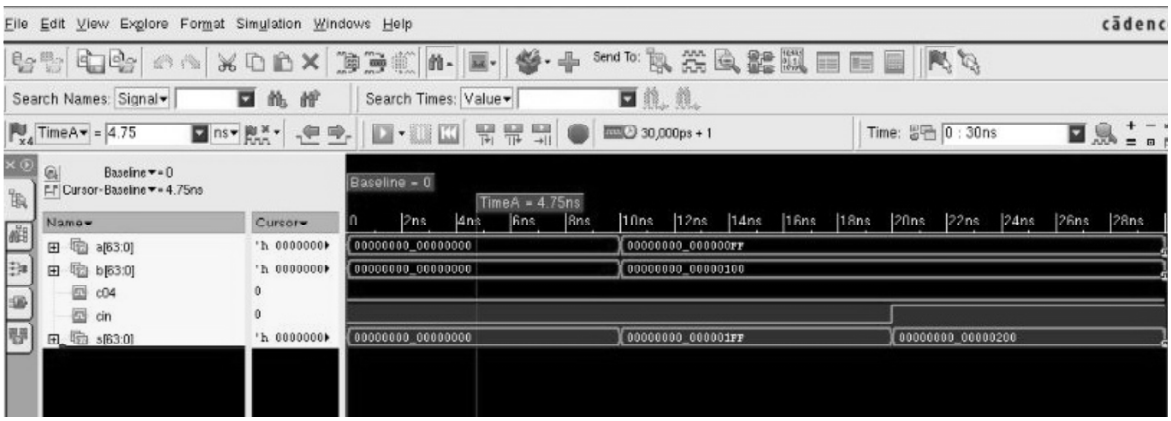

Figure 8: Output of concatenation and incrementa-tion carry skip adder

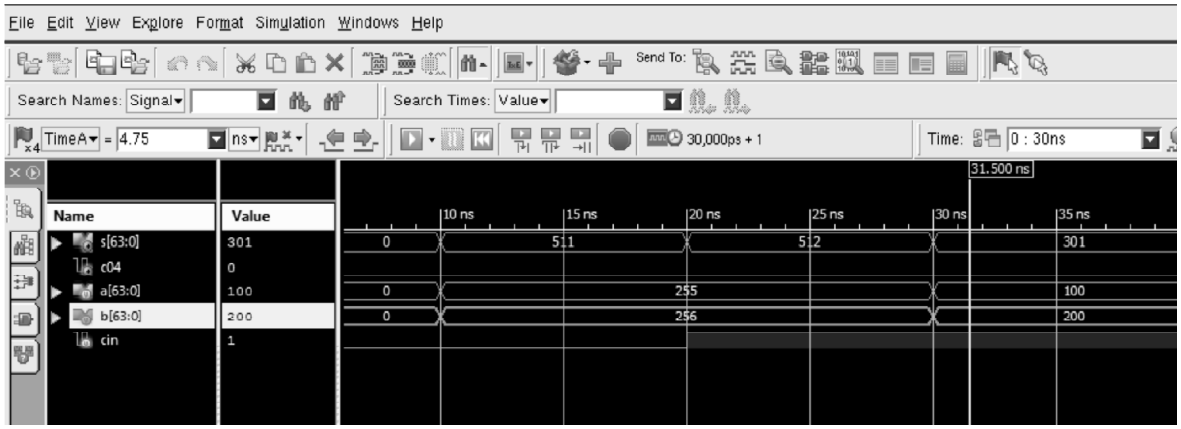

Figure 9: Output of hybrid variable latency carry skip adder

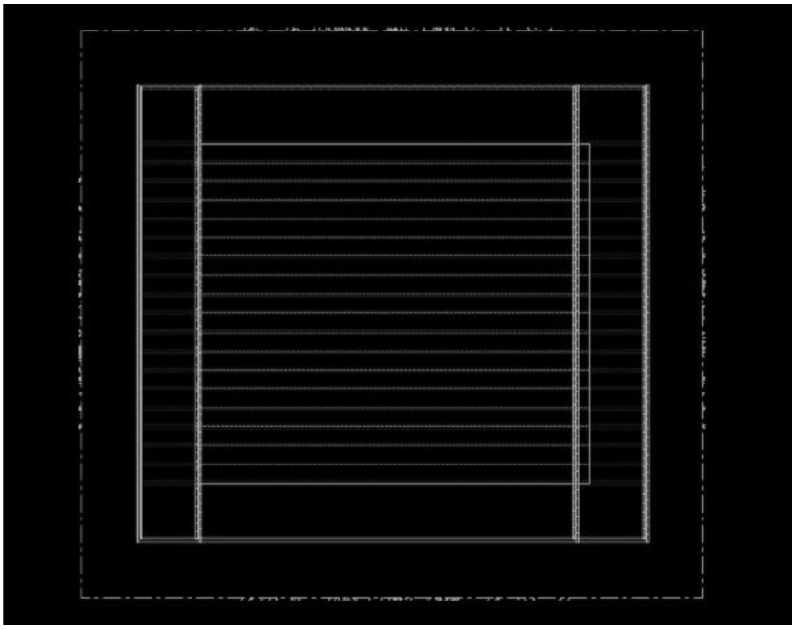

Figure 10: Floorplanning and Placement of carry skip adder

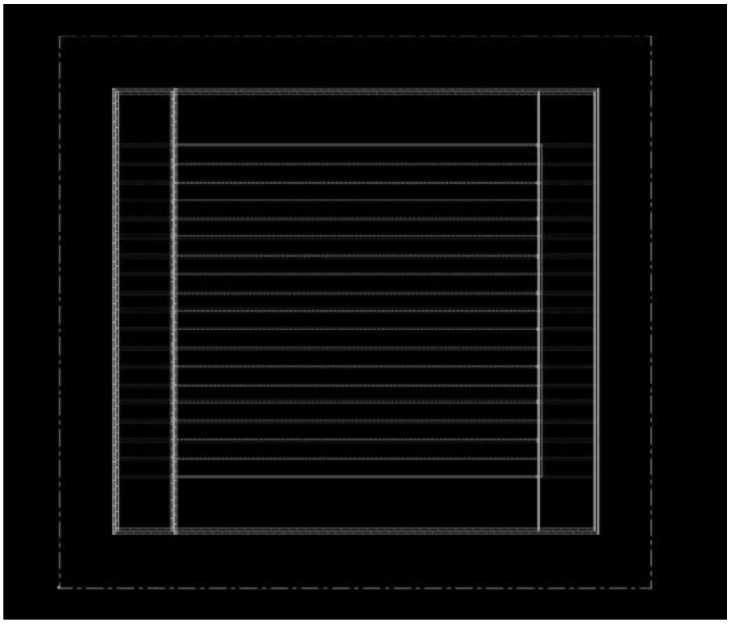

Figure 11: Floorplanning and Placement of Concatenation and Incrementation Carry skip adder

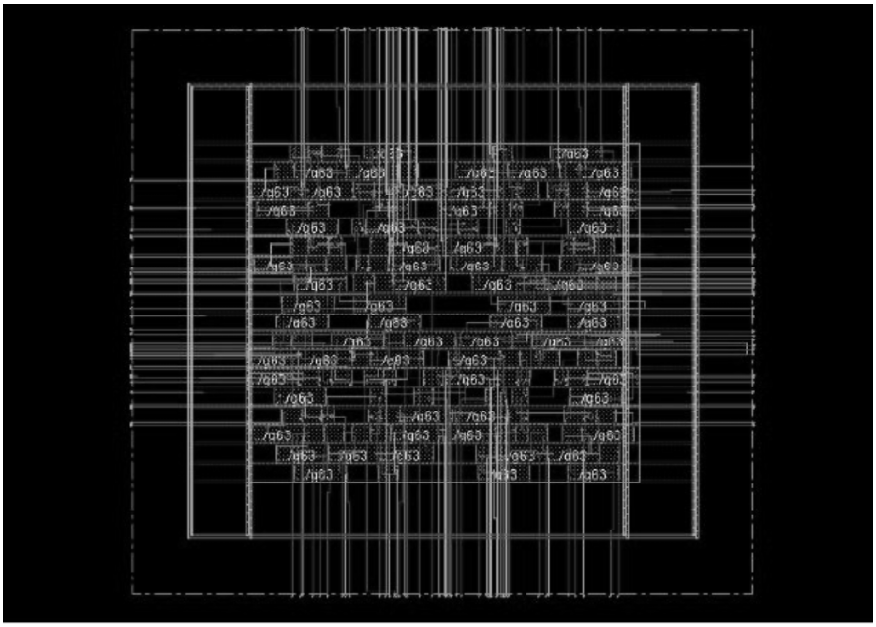

Figure 12: Routing of conventional carry skip adder

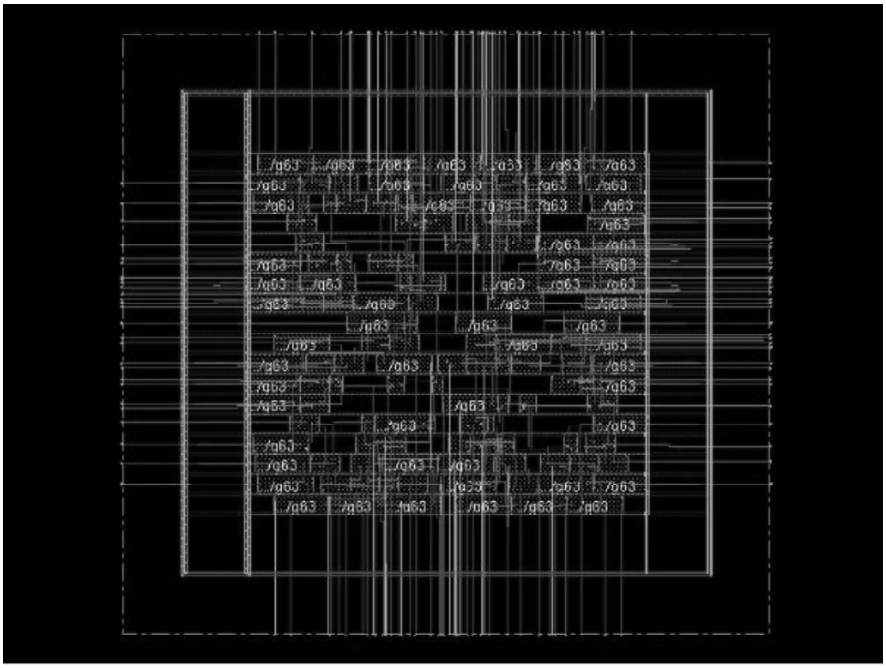

Figure 13: Routing of Concatenation and Incrementation carry skip adder

Table 1

Adder Techniques	*Delay*	*Area*	*Power*
Existing cska Structure	17.46 Ns	1691 μm	57489.16 Nw
Concatenation and Incrementaion CSKA	8.887ns	1612 μm	49376.32Nw
Hybrid variable latency CSKA	4.942 ns	1615 μm	45966.06 nw

CONCLUSION

In this paper, concatenation and incrementation 64-bit Carry Skip Adder (CSKA) structure was proposed which exhibits a higher speed and lower power consumption when compared with the existing structure. In

addition, AOI and OAI compound gates were exploited for the carry skip logics. The efficiency of the concatenation and incrementation structure for both FSS and VSS was studied. The results also suggested that the CSKA structure is a very good adder for the applications where both the speed and energy consumption are critical.

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