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Simulation of Five Level Cascaded Inverter by Using Carrier Based Neutral Voltage Modulation Technique

S. Sarada,* R. Madhan Mohan, and M. Thulasi*****

Abstract: This project proposes a pulse width modulation strategy to achieve balanced line-to-line output voltages and to maximize the modulation index in the linear modulation range where the output voltage can be linearly adjusted in the multilevel cascaded inverter (MLCI) operating under unbalanced dc-link conditions. In these conditions, the linear modulation range is reduced, and a significant output voltage imbalance may occur as voltage references increase. From this analysis, the maximum linear modulation range considering an unbalanced dc-link condition is evaluated. After that, a neutral voltage modulation strategy is proposed to achieve output volt-age balancing as well as to extend the linear modulation range up to the maximum reachable point. In the proposed method, too large of a dc-link imbalance precludes the balancing of the output voltages. In neutral voltage modulation strategy, the total harmonic distortion is reduced.

Index Terms: Harmonic injection, multilevel cascaded inverters (MLCIs), neutral voltage modulation (NVM), phase-shifted (PS) modulation, space vector pulse width modulation (PWM) (SVPWM).

1. INTRODUCTION

Multilevel inverters enable the synthesis of a sinusoidal output voltage from several steps of voltages. For this reason, multilevel inverters have low *dv/dt* characteristics and generally have low harmonics in the output voltage and current. In addition, the switching of very high voltages can be achieved by stacking multilevel inverter modules. Due to these advantages, multilevel inverters have been applied in various application fields. In MLCI applications, a modulation strategy to generate gating signals is very crucial to achieve high-performance control. Regarding this issue, many studies have been conducted, and they are roughly categorized into multilevel selective harmonic elimination pulse width modulation (PWM) (SHEPWM), multilevel carrier-based PWM, and multilevel space vector PWM (SVPWM) methods. Generally, a carrier-based PWM or SVPWM is preferred in applications such as motor drives, where dynamic properties are very important, whereas SHEPWM is preferred in some high-power static power conversion applications. An SVPWM method has been studied to cover the over modulation range in the multilevel inverter.

To reduce the common-mode voltage, a multilevel SVPWM has been proposed. The series SVPWM method has been reported to easily implement SVPWM for the MLCI. An SVPWM is proposed for hybrid inverters consisting of neutral point clamp and H-bridge inverters to improve output voltage quality and efficiency. As with two-level inverters, it is also possible to implement carrier-based SVPWMs which are equivalent to traditional SVPWMs by injecting a common offset voltage to the three-phase references. Some methods to calculate the offset voltages to achieve the optimal space vector switching sequence are addressed. The performances of a carrier-based PWM and an SVPWM are compared, and a PWM scheme is proposed to obtain an optimal output voltage in the multilevel inverter. On the other hand, MLCIs require separated dc links. Therefore, if there is one or

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more faults present in the dc links in each phase, or if the voltage magnitudes of the dc links are unequal, the output voltage of the MLCI can be unbalanced without proper compensation. To resolve this issue, some studies have been conducted.

It is shown that the available modulation index is reduced under faulty conditions on switch modules in multilevel inverters, and compensation algorithms are proposed for phase-disposition PWM and phase-shifted (PS) PWM cases. For a STATCOM application, a zero sequence voltage to decouple a three-phase MLCI into three single-phase MLCIs is applied as well as zero average active power techniques to operate the MLCI under unbalanced source or load conditions. Reference explains why the optimum angles and modulation indexes are necessary to obtain maximum balanced load voltages in the MLCI undergoing a fault on switching modules. A neutral voltage shifting technique has been introduced for balancing the state of charge in the MLCI-based battery energy storage system. A duty cycle modification method has been proposed to compensate an output voltage imbalance caused by single-phase power fluctuations.

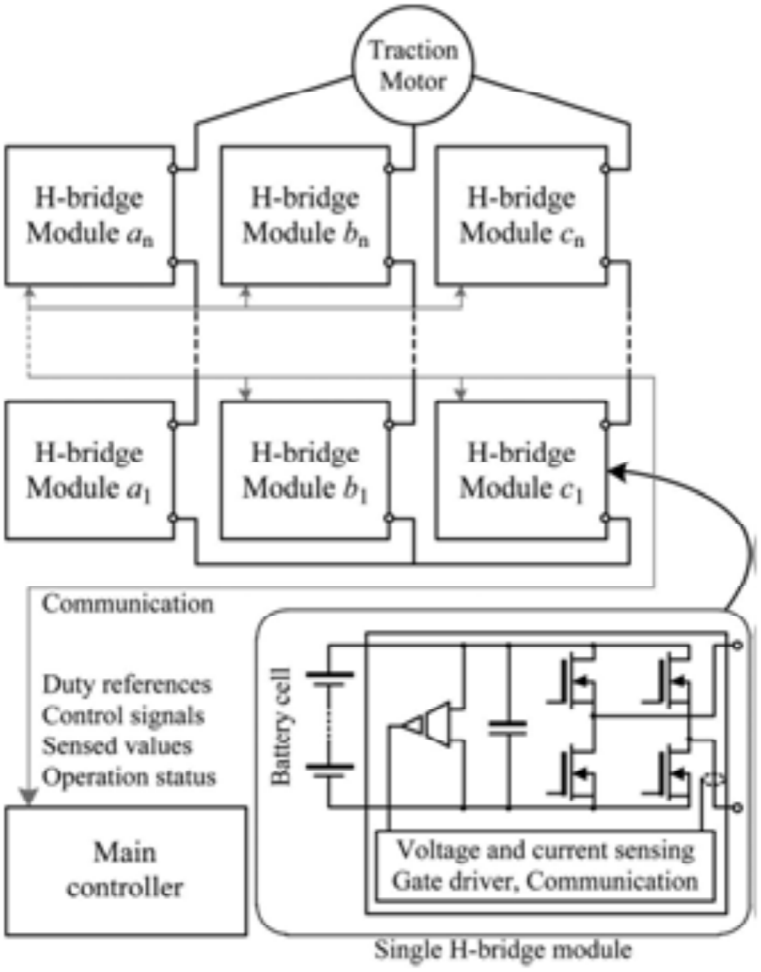


Figure 1: MLCI-based inverter for EV traction drive.

2. SYSTEM CONFIGURATION AND VOLTAGE VECTOR SPACE ANALYSIS

2.1. Configuration of MLCI for EV Traction Motor Drive

Fig. 1 shows the EV traction motor drive system that is dealt with in this paper. In this configuration, various power ratings can be easily implemented by configuring the number of the single H-bridge modules according to a required specification such as a neighborhood EV, full-size sedan, and so on. Here, each H-bridge module incorporates voltage and current sensing circuitries, gate drivers, and communication interfaces between the module itself and

the main controller. In addition, battery cells can be also included in the H-bridge module. The unipolar modulation technique is applied between two switching legs in the H-bridge module. Therefore, the effective switching frequency f_{sw} in a phase is

$$f_{sw} = 2N \times f_c \tag{1}$$

Where N and fc represent the number of the H-bridge modules in each phase and the carrier frequency of PWM, respectively. As an example, Fig. 2 shows the carriers for each module, the duty cycles in unipolar modulation, and the output voltage when $N = 2$.

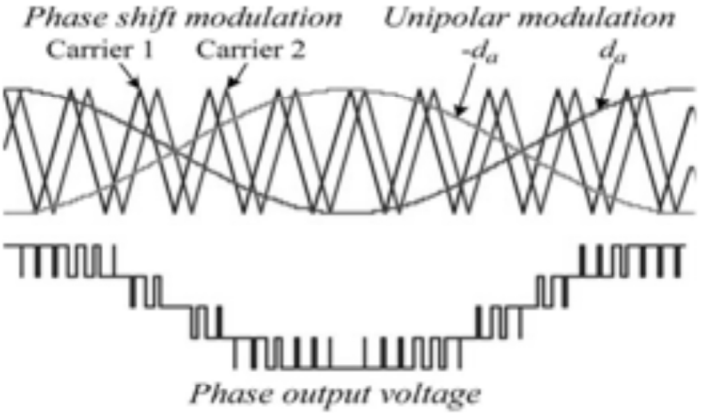


Figure 2: Unipolar and phase shift modulation for single H-bridge module.

B. Voltage Vector Space Analysis

When the dc-link voltage of a single H-bridge module is *V*dc, the output voltage *vpn* has three states, i.e., *V*dc, 0, and –*V*dc,

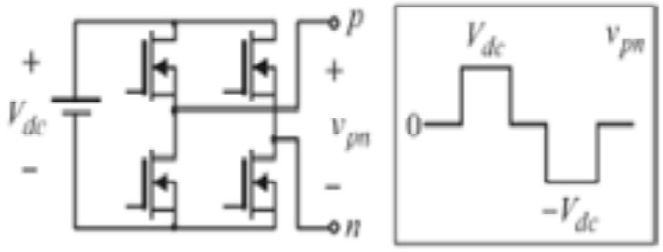


Figure 3: Output voltage of a single H-bridge modu

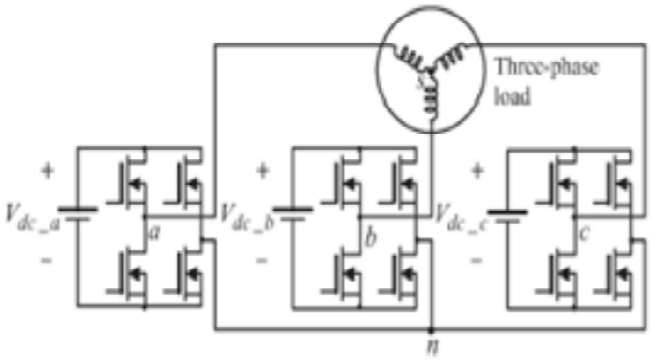


Figure 4: One-by-three configuration MLCI.

As shown in Fig. 3. By adopting the concept of a switching function, it can be represented as

$$v_{pn} = S_p V_{dc}$$
$$S_p \in \{-1, 0, 1\}_{p = a, b, \text{or}, c} \tag{2}$$

Where *Sp* is a switching function and *p* can be replaced with *a*, *b*, or *c*, which represent the phases. Fig. 4 shows a simple one-by-three configuration MLCI. For voltage vector space analysis, the main concept is derived from this simple topology, and then, it is expanded to more levels. In Fig. 4, there are two neutral points *s* and *n* in the MLCI. Here, the voltage between the output point of each phase and the neutral point *n* is defined as the pole voltage. The pole voltages are represented as v_{an}, v_{bn}, and v_{cn}. The voltage between the output point of each phase and the load side neutral point *s* is specified as the phase voltage. The phase voltages include v_{as}, v_{bs}, and v_{cs}. By using this concept, the voltage between the two neutral points is defined as *vsn* and can be written as

$$v_{sn} = -v_{as} + v_{an} = -v_{bs} + v_{bn} = -v_{cs} + v_{cn}. \tag{3}$$

By using the condition that the sum of all phase voltages is zero because the load does not have a neutral line, v_{sn} is rewritten as

$$v_{sn} = \frac{1}{3}\left(v_{an} + v_{bn} + v_{cn}\right). \tag{4}$$

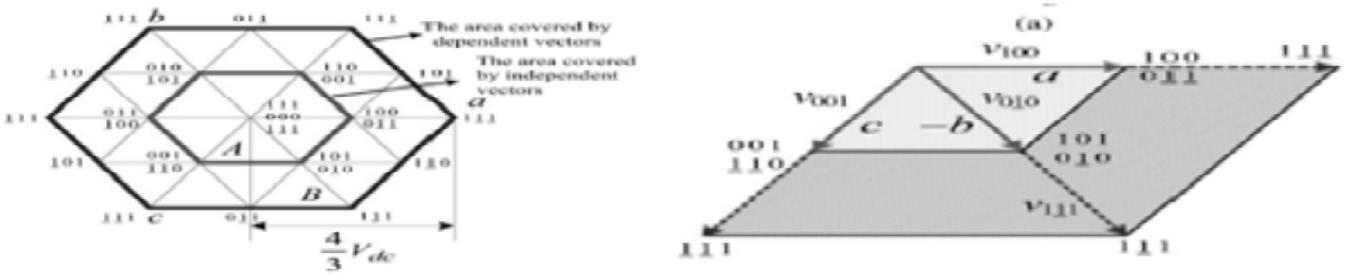


Figure 5: Voltage vector space of one-by-three configuration MLCI.

By substituting (4) into (3), the phase voltage of each phase is represented as follows by using the relationship defined in (2):

$$\begin{aligned} v_{as} &= \frac{2}{3}S_a V_{dc\_a} - \frac{1}{3}S_b V_{dc\_b} - \frac{1}{3}S_c V_{dc\_c} \\ v_{bs} &= -\frac{1}{3}S_a V_{dc\_a} + \frac{2}{3}S_b V_{dc\_b} - \frac{1}{3}S_c V_{dc\_c} \\ v_{cs} &= -\frac{1}{3}S_a V_{dc\_a} - \frac{1}{3}S_b V_{dc\_b} + \frac{2}{3}S_c V_{dc\_c}. \end{aligned} \tag{5}$$

If the magnitudes of three dc links are balanced so that V_{dc_a}, V_{dc_b}, and V_{dc_c} have the same value V_{dc}, the voltage vector space in α–β coordinates is defined in Fig. 5(a) by using (5). In the figure, underbars indicate that the switching function has the value of "1. A part of the hexagon in Fig. 5(a) is shown in Fig. 5(b). In this figure, the vectors *v*010 and *v*111 are placed at the same reference axis, phase *b*. However, the constituents of those vectors are different. For *v*010, this vector can be synthesized without the other two phases' assistance. However, *v*111 cannot be produced without other vectors according to (5). From this, let the vectors which do not require other two phases' assistance to be defined as "the independent vectors." Similarly, the vectors which require other phases' support are defined as "the dependent vectors." According to these definitions, *v*100, *v*001, and *v*010 are the independent vectors, while *v*111, *v*111, and *v*111 are the dependent vectors in Fig. 5(b). Fig. 5(a) also compares the regions that can be composed by the independent and the dependent vectors. Unlike traditional three-phase

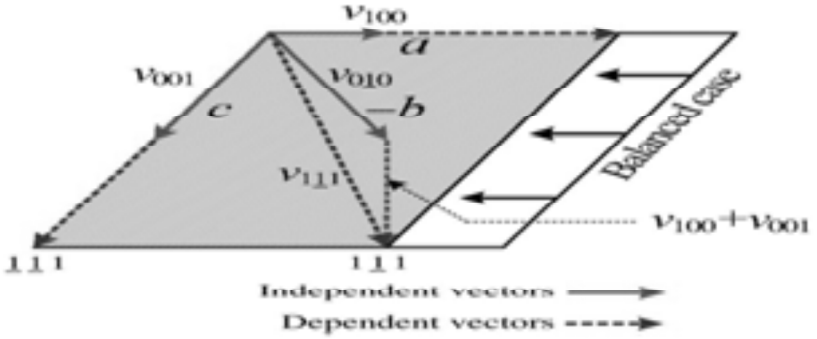


Figure 6: Voltage vector space in an unbalanced dc-link condition.

half bridge inverters, the independent vectors can be fully applied in a switching period because the dc links in each of the three phases are separated in the given system. It should be noted that the maximum voltage is decided by the dependent vectors in the entire voltage vector space. Now, let us consider the case when a three-phase load is supplied by unequal dc links. Fig. 6 shows an extremely unbalanced case where *V*dc_*a* is half of the others. If *V*dc_*a* decreases, the magnitudes of the independent vectors in phase *a* are also reduced. As a result, the magnitude of *v*100 is decreased. Here, the phase angle of *v*111, which is the sum of *v*010, *v*100, and *v*001, is no longer matched with the angle of the independent vectors in phase *b* from the figure. As shown in the figure, if the magnitudes of the independent vectors are reduced, the available voltage vector space is also reduced, and the angles of the dependent vectors are no longer multiples of 60*æ%*.

3. PROPOSED MODULATION TECHNIQUE

3.1. Traditional Offset Voltage Injection Method

The offset voltage injection scheme is a popular technique in three-phase half-bridge inverter applications. The theory behind this is that an offset voltage is incorporated with phase voltage references to implement various PWM schemes in carrier-based PWM by using the fact that line-to-line voltages are applied to a three-phase load.

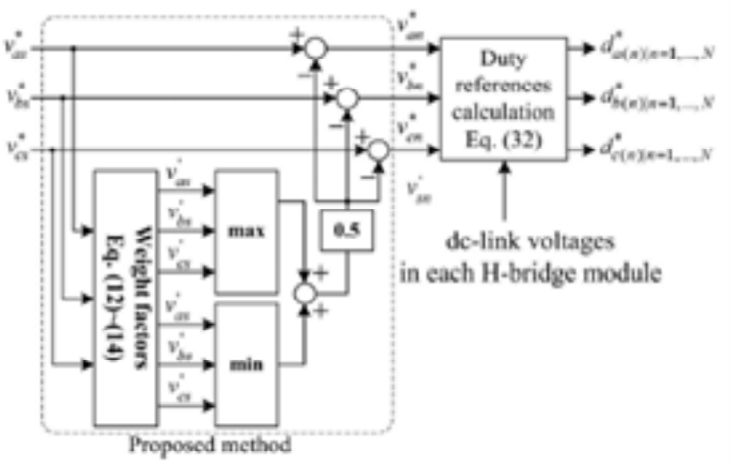


Figure 7: Implementation of the NVM method.

$$v_{sn}^{*}=\frac{v_{\max}^{*}+v_{\min}^{*}}{2} \qquad v_{\max}^{*}=\max\left(v_{as}^{*},v_{bs}^{*},v_{cs}^{*}\right)$$

$$v_{\min}^{*}=\min\left(v_{as}^{*},v_{bs}^{*},v_{cs}^{*}\right) \tag{6}$$

Then, the pole voltage references $v_{an}^{*}, v_{bn}^{*},$ and $v_{cn}^{*},$ which will be converted to PWM duty references, are

$$v_{an}^{*}=v_{as}^{*}-v_{sn}^{*} \qquad v_{bn}^{*}=v_{bs}^{*}-v_{sn}^{*} \qquad v_{cn}^{*}=v_{cs}^{*}-v_{sn}^{*}. \tag{7}$$

However, the aforementioned technique may not maximize the linear modulation range in MLCI undergoing unbalanced dc-link conditions.

3.2. Proposed NVM Method

If the dc links in an MLCI are unbalanced and the traditional offset voltage injection methods are utilized, the three-phase output voltages may become distorted as the phase voltage reference approaches $V_{\text{ph\_max}}$. This is because the traditional methods are not considering unbalanced dc-link conditions. Therefore, even if a phase can synthesize an output voltage reference in the linear modulation range, the other phases can be saturated or go into the over modulation region. In this situation, a neutral voltage can be produced by the saturated or over modulated phase.

In order to resolve this issue and to synthesize the output voltage to V_{ph_max} in the linear modulation range, the NVM technique is proposed in this paper. Fig. 7 shows the concept of the proposed NVM technique. Here, a neutral voltage between the two neutral points *n* and *s* in Fig. 4 is modulated to compensate the output voltage imbalance caused by unbalanced dc-link conditions. To do this, first, the weight constant K_w is defined as

$$K_w = \frac{V_{dc}\ mid + V_{dc}\ \min}{2}. \tag{8}$$

By using (8), the weight factors are calculated as

$$K_{w\_a} = \frac{K_w}{V_{dc\_a}} K_{w\_b} = \frac{K_w}{V_{dc\_b}} K_{w\_c} = \frac{K_w}{V_{dc\_c}} \tag{9}$$

Where K_{w_a}, K_{w_b}, and K_{w_c} represent the weight factors for phases *a*, *b*, and *c*, respectively. Next, the weight factors are multiplied by the phase voltage references, and the new references v'_{as}, v'_{bs}, and v'_{cs} are obtained as,

$$v'_{as} = K_{w\_a} v^*_{as} \qquad v'_{bs} = K_{w\_b} v^*_{bs} \qquad v'_{cs} = K_{w\_c} v^*_{cs}. \tag{10}$$

It should be noted that, depending on dc-link conditions, the sum of v'_{as}, v'_{bs}, and v'_{cs} may not be zero. By using these components, the injected voltage and the pole voltage v'_{sn} references are given as

$$v'_{\max} = \max\left(v'_{as}, v'_{bs}, v'_{cs}\right)\ \ v'_{\min} = \min\left(v'_{as}, v'_{bs}, v'_{cs}\right)$$

$$v'_{sn} = \frac{v'_{\max} + v'_{\min}}{2} \qquad \begin{bmatrix} v^*_{an} \\ v^*_{bn} \\ v^*_{cn} \end{bmatrix} = \begin{bmatrix} v^*_{as} - v'_{sn} \\ v^*_{bs} - v'_{sn} \\ v^*_{cs} - v'_{sn} \end{bmatrix}. \tag{11}$$

From (11), the line-to-line voltages across each phase of the load are represented as

$$\begin{bmatrix} v^*_{ab} \\ v^*_{bc} \\ v^*_{ca} \end{bmatrix} = \begin{bmatrix} v^*_{an} - v^*_{bn} \\ v^*_{bn} - v^*_{cn} \\ v^*_{cn} - v^*_{an} \end{bmatrix} == \begin{bmatrix} v^*_{as} - v'_{sn} - v^*_{bs} + v'_{sn} \\ v^*_{bs} - v'_{sn} - v^*_{cs} + v'_{sn} \\ v^*_{cs} - v'_{sn} - v^*_{as} + v'_{sn} \end{bmatrix} = \begin{bmatrix} v^*_{as} - v^*_{bs} \\ v^*_{bs} - v^*_{cs} \\ v^*_{cs} - v^*_{as} \end{bmatrix}. \tag{12}$$

As it can be seen in (12), v'_{sn} does not appear in the line-to-line voltages, and it is still considered as a hidden freedom of voltage modulation. Now, let us consider the role of the weight factors K_{w_a}, K_{w_b}, and K_{w_c}, which are inversely proportional to the corresponding dc-link voltage. For convenience, let us assume that the magnitudes of the dc-link voltage are under the following relationship:

$$V_{dc\_a} < V_{dc\_b} < V_{dc\_c}. \tag{13}$$

Then, from (9) and (13)

$$K_{w\_a} > K_{w\_b} > K_{w\_c} \qquad K_{w\_a} > 1\ K_{w\_b}, K_{w\_c} < 1. \tag{14}$$

Equation (14) gives

$$\left|v'_{as}\right| > \left|v^*_{as}\right|\ \ \left|v'_{bs}\right| > \left|v^*_{bs}\right|\ \ \left|v'_{cs}\right| < \left|v^*_{cs}\right|. \tag{15}$$

From (11) and (15), it can be recognized that, if v'_{as}, whose dc-link voltage is less than the others, is corresponding to $v'_{\max}$ or $v'_{\min}$, the absolute value of v'_{sn} is greater than v^*_{sn} in (6). On the other hand, the final pole voltage references v^*_{an}, v^*_{bn} and v^*_{cn} are calculated by subtracting v'_{sn} from the original phase voltage references v^*_{as}, v^*_{bs} and v^*_{cs} as in (11). From this reasoning, in this example, it is supposed that, if v'_{as} is corresponding to $v'_{\max}$, then the final pole voltage references v^*_{an}, v^*_{bn}, and v^*_{cn} are less than the original pole voltage references which are not considering v'_{sn} but v^*_{sn}. On the contrary, if v'_{cs} is $v'_{\max}$, then the final pole voltage references are greater than the original pole voltage references. By using this principle, the proposed method reduces the portion of the phase whose dc-link voltage is smaller than the others and increases the utilization of the phase in which the dc-link voltage is greater than those of the other phases. However, as it can be seen in (12), v'_{sn} does not affect the line-to-line voltages. Therefore, the line-to-line voltage is the same as the one derived from the original phase voltage reference. From this analysis, the proposed method enables the maximum synthesizable modulation index in the linear modulation range under the unbalanced dc-link conditions to be achieved. In addition to this, if all of the dc-link voltages are well balanced so that V_{dc_a}, V_{dc_b}, and V_{dc_c} are equal to V_{dc}.

$$V_{dc\_mid} = V_{dc\_min} = V_{dc}. \tag{16}$$

By substituting (16) into (8)–(10)

$$K_w = \frac{V_{dc\_mid} + V_{dc\_\min}}{2} = V_{dc}$$

$$K_{w\_a} = K_{w\_b} = K_{w\_c} = 1$$

$$v'_{as} = v^*_{as} \quad v'_{bs} = v^*_{bs} \quad v'_{cs} = v^*_{cs}. \tag{17}$$

Equation (17) shows that the proposed method gives the same voltage references as the traditional method under balanced dc-link conditions.

4. CONSTRAINTS OF THE PROPOSED METHOD

In this section, the limitation of how unbalanced dc links can be while still being compensated by the proposed method is evaluated. Fig. 8 shows the modulated voltage waveforms with different modulation methods and dc-link conditions. In the figure, cases I and II show the results of traditional sinusoidal PWM (SPWM) and carrier-based SVPWM, while cases III and IV illustrate the waveforms of the proposed method with different ratios of dc-link voltages. In Fig. 8, the vertices at □π/2 and 3π/2 rad almost come in contact with, but do not cross, the zero

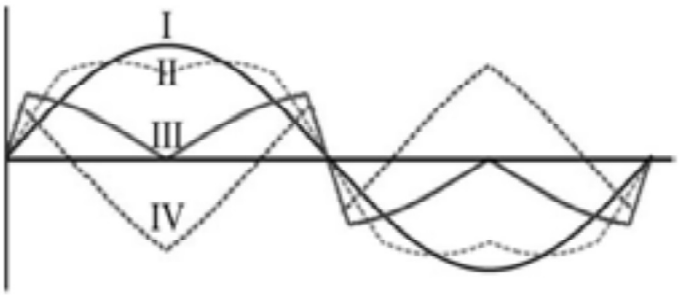


Figure 8: Comparison of modulated waveforms. (I) Without. (II) Traditional carrier-based SVPWM. (III) Proposed NVM with V_{dc_a} = 0.275 V_{dc}, V_{dc_b} = V_{dc}, and V_{dc_c} = V_{dc}. (IV) Proposed NVM with V_{dc_a} = 0.2 V_{dc}, V_{dc_b} = V_{dc}, and V_{dc_c} = V_{dc}.

point. However, the directions of the vertices are opposite the original phase voltage reference in case IV. This means that an excessive and unnecessary voltage is injected into the system.

The maximum linear modulation range is reduced, and the line to line voltage may be distorted. With this basic concept, it is assumed that a phase which has the lowest dc-link voltage commands v^*max and a phase which has the highest dc-link voltage commands v^*min to examine a worst case situation. From (10) and (11), the following equations can be established:

$$v'_{\max} = \frac{V_{dc\_\mathrm{mid}} + V_{dc\_\min}}{2V_{dc\_\min}} v^*_{\max}$$

$$v'_{\min} = \frac{V_{dc\_\mathrm{mid}} + V_{dc\_\min}}{2V_{dc\_\max}} v^*_{\min}$$

$$v'_{sn} = \frac{v'_{\max} + v'_{\min}}{2}. \tag{18}$$

By using (18), the pole voltage reference which is considered as the worst case is

$$v^*_{\max\_n} = v^*_{\max} - \frac{v'_{\max} + v'_{\min}}{2}. \tag{19}$$

By substituting (18) into (19), we have

$$v'_{\max\_n} = \left(1 - \frac{V_{dc\_\mathrm{mid}} + V_{dc\_\min}}{4V_{dc\_\min}}\right) v^*_{\max} - \frac{V_{dc\_\mathrm{mid}} + V_{dc\_\min}}{4V_{dc\_\max}} v^*_{\min}. \tag{20}$$

Unless all three-phase voltage references are not zero simultaneously, near a positive peak of the original voltage reference, the sufficient condition which guarantees the same polarity between v^* max and v^*min is established as follows:

$$v'_{\max\_n} > 0 \quad v^*_{\max} > 0 \quad v^*_{\min} < 0. \tag{21}$$

By substituting (20) into the first condition in (21), the following condition can be written:

$$k_1 v^*_{\max} > k_2 v^*_{\min} \quad k_1 = 1 - \frac{V_{dc\_\mathrm{mid}} + V_{dc\_\min}}{4V_{dc\_\min}} \quad k_2 = \frac{V_{dc\_\mathrm{mid}} + V_{dc\_\min}}{4V_{dc\_\max}}. \tag{22}$$

Here, it is obvious that $k2$ is always positive. Therefore, as long as $k1$ is positive, the condition (22) is always satisfied, and $k1$ can be rearranged as follows:

$$k_1 = \left(\frac{3V_{dc\_\min} + V_{dc\_\mathrm{mid}}}{4V_{dc\_\min}}\right) \tag{23}$$

Equation (24) is then directly obtained from (23) to ensure that $k1$ will always be positive

$$V_{dc\_\min} > \frac{1}{3} V_{dc\_\mathrm{mid}}. \tag{24}$$

Note that (24) is a sufficient condition to meet the conditions in (21) so that the proposed method can be applied. However, even if (24) is not satisfied so that k_1 is negative, there still is a chance to apply the proposed method. To deal with this situation, let us consider the relationship between v*max and v* min as follows at a positive peak point:

$$v^*_{\max} = -2v^*_{\min}. \tag{25}$$

By substituting (25) into (22), we have

$$-2k_1 > k_2. \tag{26}$$

Since k_1 is negative in this case, the following condition is derived from (26);

$$|k_1| < \frac{k_2}{2}. \tag{27}$$

If the relationship between k_1 and k_2 is established as in (27), even if the provision in (24) is broken, the conditions in (25) are satisfied so that the proposed method can be still effective. Let us recall Fig. 9 again here. In the figure, the values of $|k_1|$ and $k_2/2$ for case III are evaluated as 0.1591 and 0.1593, respectively. Although the difference between the two values is very small, (27) is still true with these values. For case IV, the values of $|k_1|$ and $k_2/2$ are calculated as 0.5 and 0.3, respectively.

4.1. Duty Calculation

In Fig. 7, the final voltage references are entered to the duty reference calculation block. In this block, the duty references of each H-bridge module are calculated as follows:

$$d^*_{a1} = d^*_{a2} = ... = d^*_{aN} = \frac{v^*_{an}}{V_{dc\_a}}$$

$$d^*_{b1} = d^*_{b2} = ... = d^*_{bN} = \frac{v^*_{bn}}{V_{dc\_b}}$$

$$d^*_{c1} = d^*_{c2} = ... = d^*_{cN} = \frac{v^*_{cn}}{V_{dc\_c}}. \tag{28}$$

The calculated duty references are compared to PS carriers to generate gating signals, as shown in Fig. 9. It should be noted that the duty references for each H-bridge in each phase are shared in the PS modulation.

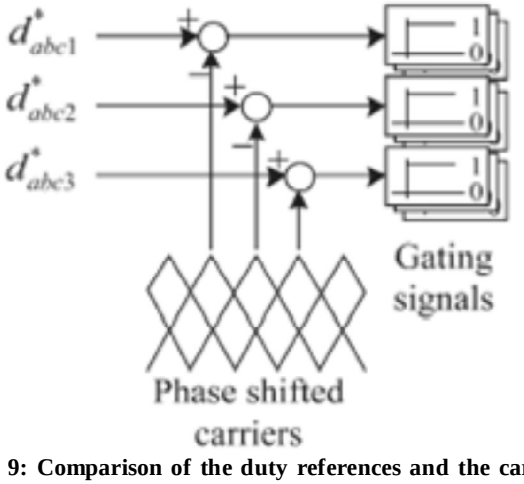


Figure 9: Comparison of the duty references and the carriers.

Fig. 10 compares the voltage vector spaces and the voltage trajectories in the α – β-axes of traditional SPWM, traditional SVPWM, and the proposed NVM method under the given simulation condition. Compared to the balanced dc-link case, the area of the voltage vector space is reduced under the unbalanced dc-link condition. In the figure, the traditional SPWM shows the worst voltage distortion and the minimum voltage vector space. The traditional SVPWM gives more area than SPWM, but still, the voltage distortion is not avoidable. The proposed method shows no distortion on the output voltage and maximizes the voltage vector space compared to other methods.

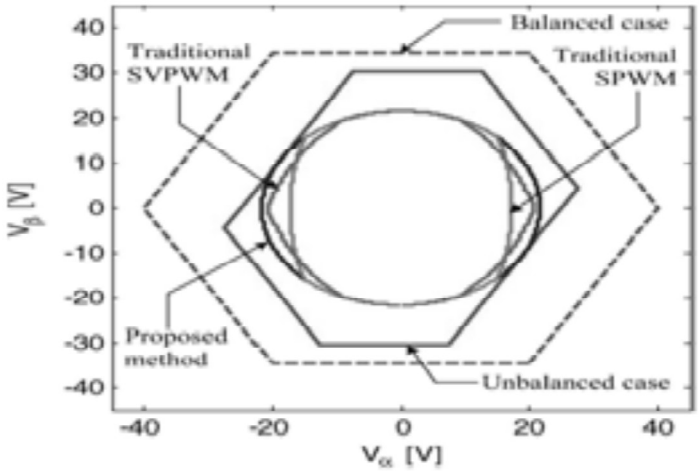


Figure 10: Comparison of the voltage vector trajectories.

5. RESULTS AND DISCUSSION

A simple one-by-three configuration MLCI model is built in MatlabSimulink. The three-phase *RL* load with $R = 0.1\Omega$ and $L = 1$mH is employed. The dc-link voltages for each phase are $V\text{dc}\_a = 0.5 \times 30$ V, $V\text{dc}\_b = 0.75 \times 30$ V, and $V\text{dc}\_c = 30$ V. The maximum synthesizable phase voltage in linear is

$$V_{ph\_\max} = \frac{0.75\times 30 + 0.5\times 30}{\sqrt{3}} = 21.65V. \tag{29}$$

The voltage references are given by

$$\begin{aligned} v_{as}^{*} &= V_{ph\_\max}\sin(100\pi t) \\ v_{bs}^{*} &= V_{ph\_\max}\sin(100\pi t - 2\pi/3) \\ v_{cs}^{*} &= V_{ph\_\max}\sin(100\pi t + 2\pi/3) \end{aligned} \tag{30}$$

The general simulation model for the traditional SPWM, traditional SVPWM, and the neutral voltage modulation is shown in fig.11.

Fig. 12 shows the time-domain simulation results with the same simulation condition. From $t = 0.0$ *s* to $t = 0.05$ *s*, traditional SPWM is used. From $t = 0.05$ s to $t = 0.1$ *s*, traditional SVPWM is used. After $t = 0.1$ s, the proposed method is applied. When traditional SPWM is applied, v_{sn}^{*} is zero, and the pole voltage references are identical to the ones in (30). With traditional SVPWM, v_{sn}^{*} is no longer zero, and the peak voltage of the pole voltage references is reduced compared to SPWM. However, the duty reference of phase *a*, where the dc-link voltage is minimum among the three phases, is saturated in both cases. Whereas with the proposed method, the fundamental frequency component of the neutral voltage is included in v_{sn}^{*}, and the duty references

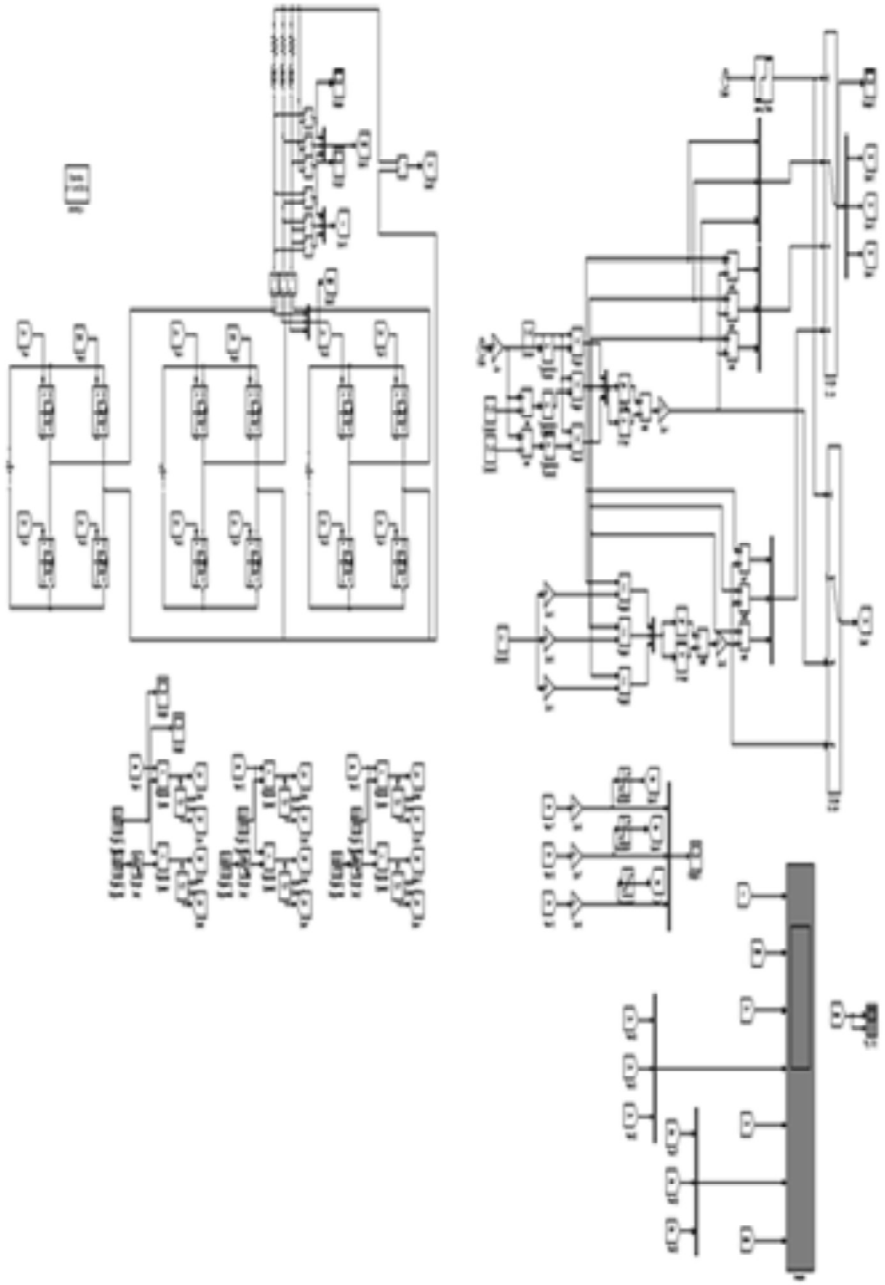


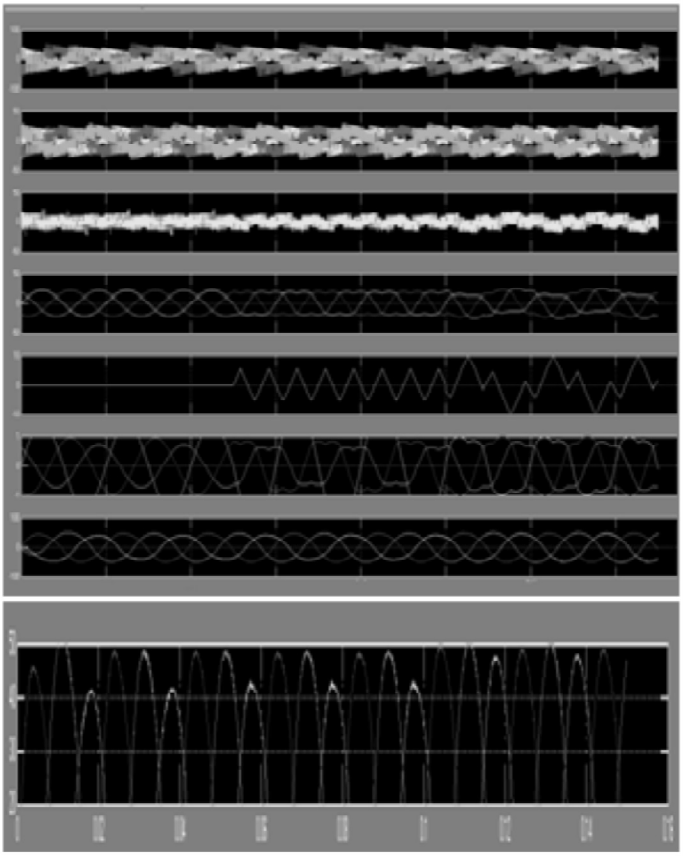
Figure 11: simulation model of 3 level cascaded inverters using traditional SPWM, traditional SVPWM, and the neutral voltage modulation.

are not saturated. The benefit of the proposed method can also be observed from the peak value of the phase current in the last section of the figure. Under traditional methods, the phase currents are unbalanced. However, the phase currents are well balanced with the proposed method. From the simulation results, it can be seen that the proposed method can synthesize the maximum available phase voltage in the linear modulation range under unbalanced dc link.

The NVM is utilized as shown in Fig.11; the phase current imbalance is compensated. At t=0.1sec the NVM is applied, and the measured THD is about 4.18%.

6. EXTENSION WORK

The NVM method 3 level cascaded inverters used. The extension work for the proposed NVM 5 level cascaded inverters used, the NVM is able to balance line-to-line output voltages as well as to maximize the linear modulation



[Sec]

Figure 12: simulation result of traditional SPWM, traditional SVPWM, and the proposed method.

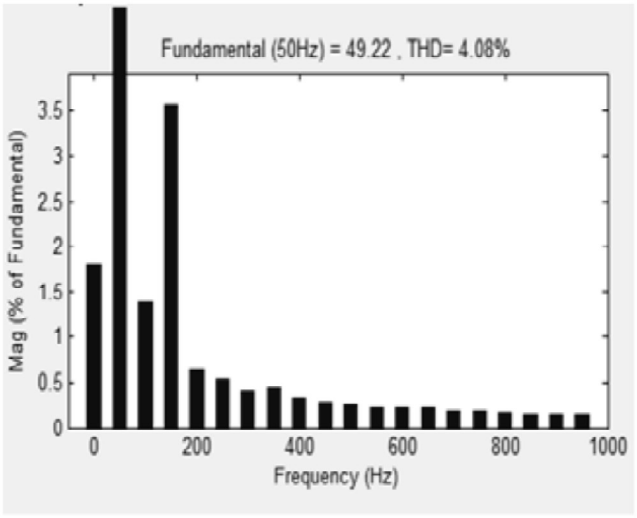


Figure 13: THD result of NVM

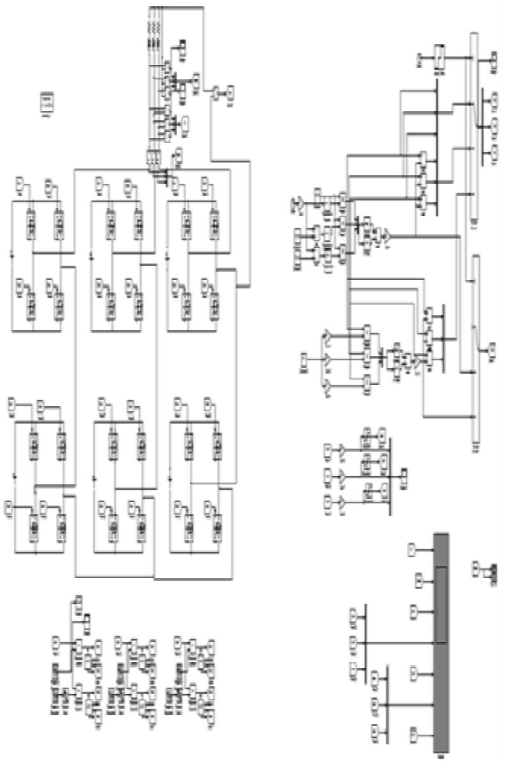


Figure14: simulation model of 5 level cascaded inverters using traditional SPWM, traditional SVPWM, and the neutral voltage modulation.

range under un balanced DC-link conditions. The THD may also reduced by using NVM. The simulation model for the extension NVM is shown in fig.14.

The simulation results of 5 level cascaded inverters using traditional SPWM, traditional SVPWM, and the neutral voltage modulation as shown in fig.15. From $t = 0.0$ *s* to $t = 0.05$ s, traditional SPWM is used. From $t = 0.05$ *s* to $t = 0.1$ *s*, traditional SVPWM is used. After $t = 0.1$ *s*, the proposed method is applied.

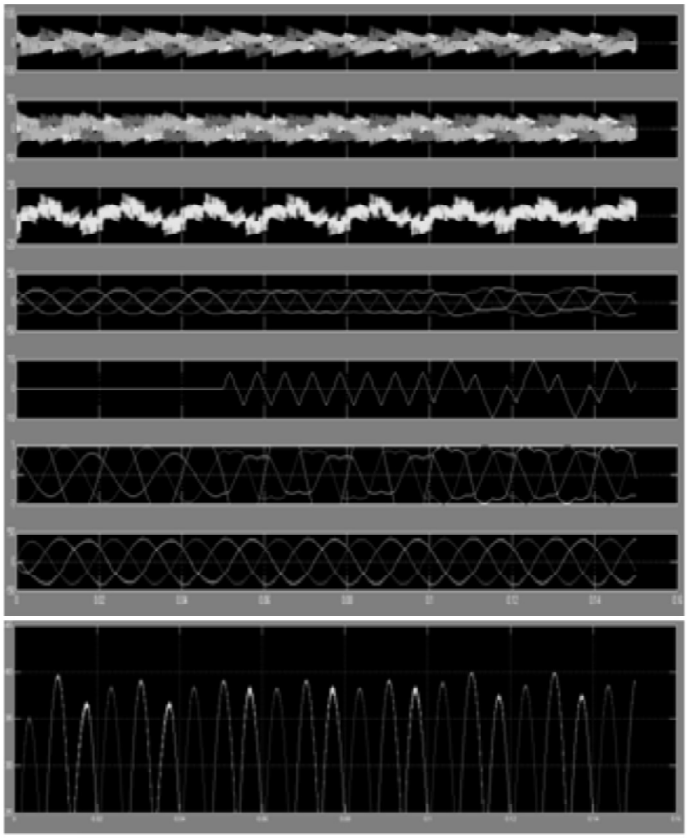


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Figure 15: simulation result of 5 level cascaded inverters using traditional SPWM, traditional SVPWM, and the NVM method.

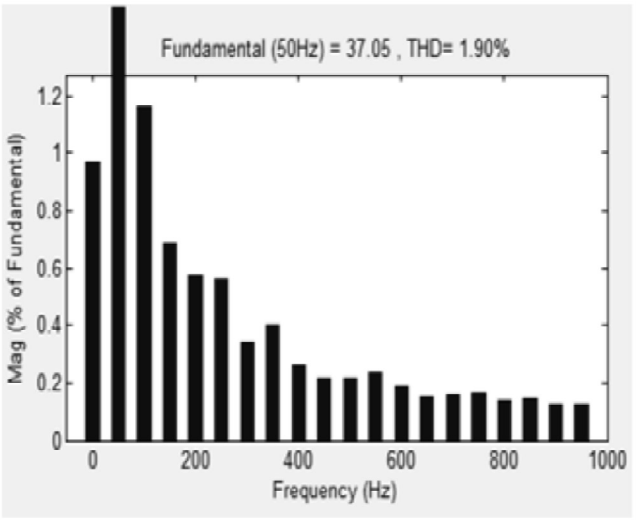

Figure 16: THD result of NVM

The 5 level cascaded inverters NVM is utilized as shown in Fig.14; the phase current imbalance is compensated. At t=0.1sec the NVM is applied, and the measured THD is about 1.90%.

7. CONCULSION

From the analysis, the maximum linear modulation range was derived. The proposed NVM technique is applied to achieve the maximum modulation index in the linear modulation range under an unbalanced dc-link condition as well as to balance the output phase voltages. Compared to the previous methods, the proposed technique is easily implemented and improves the output voltage quality under unbalanced dc-link conditions. Both simulations results based on the IPM motor drive application verify the effectiveness of the proposed method. The NVM method compensates the voltage and current imbalances under unbalanced dc-link conditions. The THD is reduced.

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