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Metal-Insulator-Metal Capacitors for Analog/Mixed Signal Circuits: A review

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ABSTRACT

This paper describes a thorough research on high-k metal-insulator-metal capacitors using various dielectric materials. Also, summarizes the works being carried out in MIM Capacitor fabrication and its characterization of the device parameters such as capacitance, leakage current, Reliability, Voltage coefficient of capacitance parameters etc. This paper reviews the progress and efforts made in the recent years for high-k dielectrics.

Keywords: Metal-Insulator-Metal Capacitor, High-k, Voltage co-efficient of capacitance, Reliability, Multilayer, Gate stack.

1. INTRODUCTION

Over the past 40 years, remarkable progress has been made in the silicon technology. In order to develop ICs with good functionality, improved performance and with increased levels of integration, the semiconductor industry has been pushed by the drive to develop modern electronic systems such as mobile phones, computers etc. This is accomplished by the way the devices are scaled down which in turn results in a constant increase in the number of components per chip. This trend is phenomenally called as "Moore's Law" which predicts that the number of components per chip doubles in every 18 months [1].

However, to develop modern electronic systems, parameters such as frequency of operation, power consumption are also important. But, it is observed that most of the areas in chip is occupied by passive components itself. Therefore, performance of these passive components plays a significant role in determining the overall characteristics of entire circuits. In particular, MIM capacitors are the key passive components which are being used in the analog and mixed signal ICs. Initially, MIS structure was used in the silicon ICs. Later, it was replaced by polysilicon-oxide-polysilicon capacitors due to the small variation of capacitance with voltage. But, the performance of this capacitor degrades when they are used at high RF frequencies. This is due to the large resistive loss from the electrodes, and parasitic capacitance [2].

Later, MIM capacitors were favoured due to its highly conductive electrodes which in turn reduce the contact resistance and low parasitic coupling to the silicon substrate [3-4]. MIM capacitors have generated considerable amount of interest for applications such as AMS ICs and RF ICs [5] compared to the other capacitor structures due to its low leakage current density, low voltage and temperature coefficients, and has the ability to withstand higher application voltage [6].

Figure 1 shows the cross-sectional schematic view of the integration of MIM capacitors into the AlCu Back-End of Line (BEOL). The MIM capacitor is integrated between the top metal layer and Standard BEOL metal layer. The capacitor's bottom electrode is a metal stack consisting of metal layer of Ti/TiN/AlCu.

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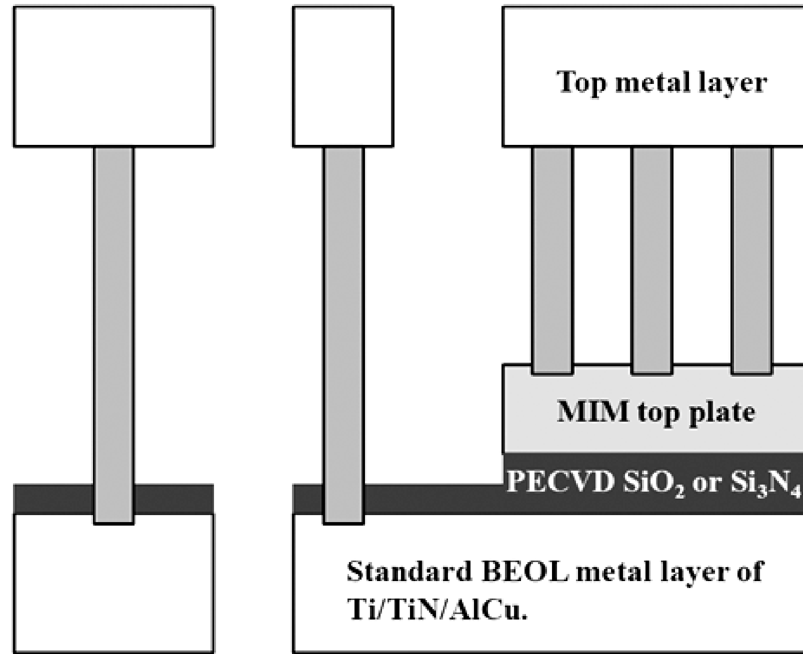

Figure 1: Cross-sectional schematic of MIM capacitor used in the AlCu BEOL

2. EVOLUTION OF MIM CAPACITORS

The metal-insulator-silicon (MIS) capacitors were initially used in Silicon ICs. Figure 2 shows the development of capacitors for silicon ICs. Later, it was replaced by the polysilicon-insulator-polysilicon (PIP) capacitors due to the better electrical characteristics. Though this capacitor showed good electrical characteristics, it suffered from poor quality factor (<50) due to the resistive losses in the contacts and plates, poor RF compatibility. Also, PIP capacitors caused undesirable variation of capacitance with voltage

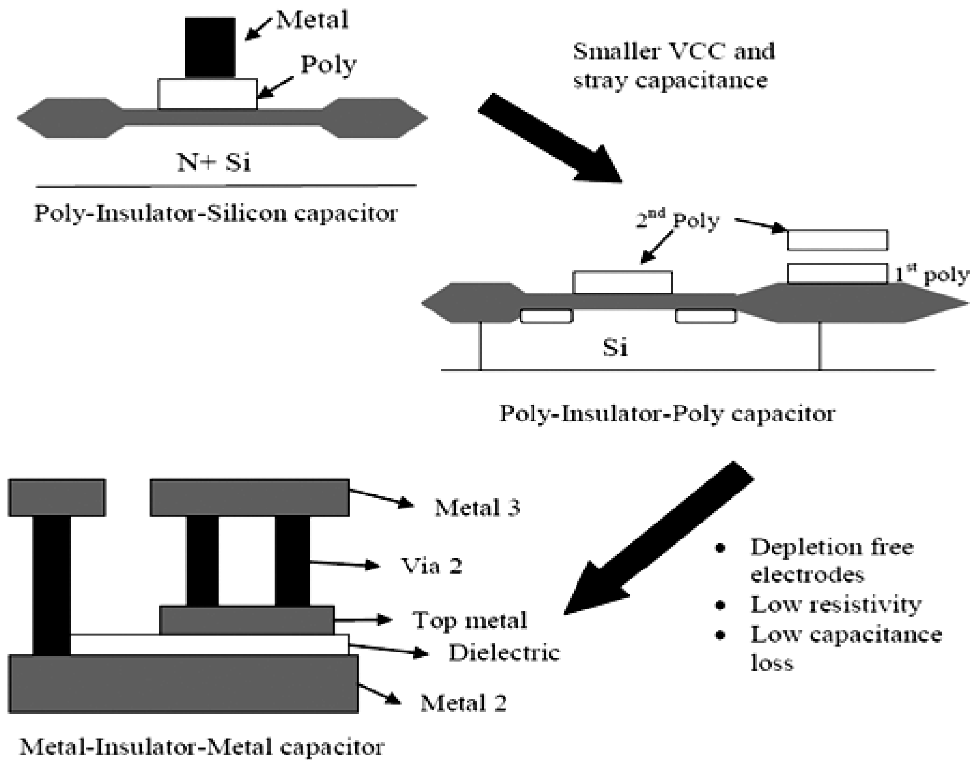

Figure 2: Development of capacitors for silicon integrated circuit from poly-insulator-silicon structure [7] to poly-insulator-poly [8] and metal-insulator-metal structures.

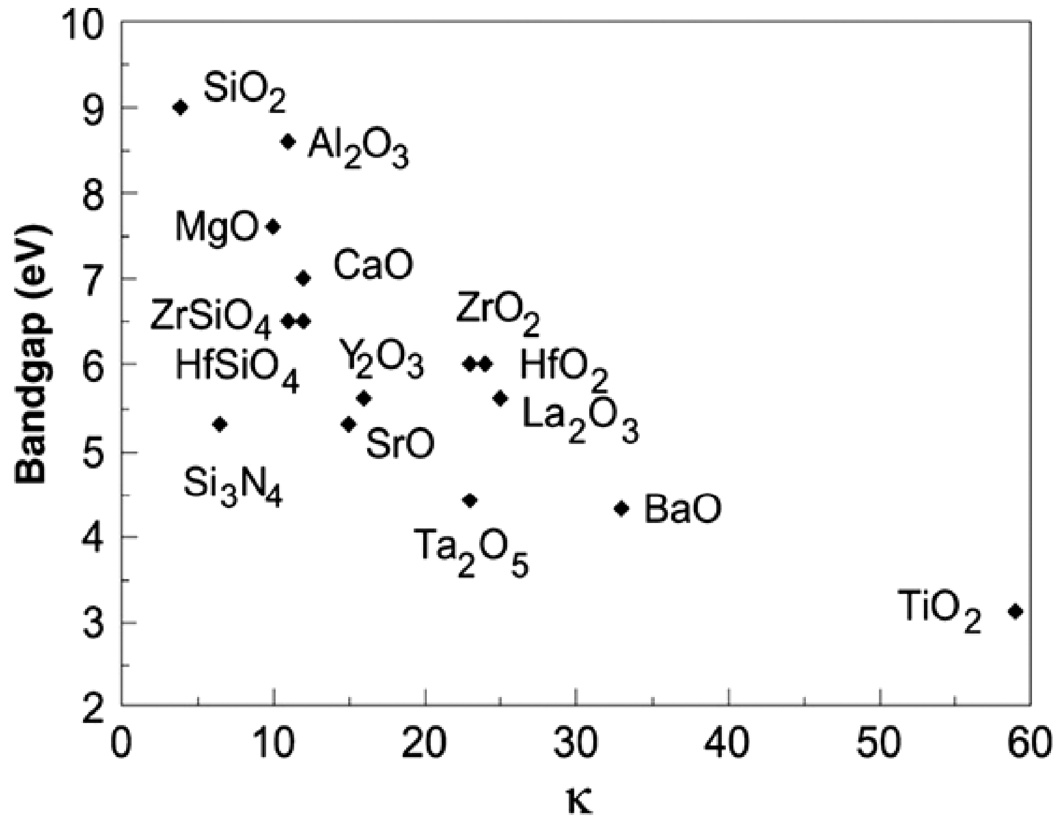

Figure 3: Dielectric constant κ versus band gap for oxides [9].

due to the depletion effect at polysilicon/substrate interface and associated parasitic capacitance [2]. This type of variations is not acceptable in high precision circuits such as analog-digital and digital-analog converters [10-11].

In PIP capacitors, an upper electrode and a lower electrode are made of conductive polysilicon, thus causing oxidation reactions on the interfaces between dielectric thin film and the upper and lower electrodes. The oxidation reaction causes formation of native oxide films, thus disadvantageously reducing overall capacitance. The top and bottom polysilicon contacts can be replaced by metal electrodes, particularly TiN or Pt [11]. After replacing the top and bottom layers with metal electrodes, this was called as Metal-Insulator-Metal Capacitors. This capacitor was used to mitigate the disadvantage of PIP capacitors. A MIM capacitor has a structure in which a lower metal, an insulating layer and an upper metal are laminated, in that order. The MIM capacitor has a low specific resistance and is free from parasitic capacitance by depletion, thus being generally applicable in high performance semiconductor devices. It was constructed over top of metal lines to avoid series resistance and cross talk between silicon substrate. Figure 3 shows the dielectric constant values of various oxides. The k values vary inversely with the band gap [9]. Higher dielectric constant materials give high capacitance density but lead to high leakage.

3. PARAMETERS OF MIM CAPACITORS

The performance of the MIM capacitors can be evaluated by many physical parameters. The key parameters for MIM capacitors are capacitance density, leakage current density, frequency dependence of capacitance, voltage linearity, dielectric reliability, and quality factor.

3.1. Capacitance density

Capacitance density is an important parameter of MIM capacitor. The integrated MIM capacitors are parallel plate capacitors. For the parallel plate capacitors, the capacitance density can be estimated by the general formula,

$$C = \frac{\varepsilon_o \varepsilon_r A}{d} \tag{1}$$

where, ε_r and ε_o are the relative permittivity and permittivity of free space (8.85×10^{-12} F/m) respectively. A is the electrode area of the capacitor, C and d are the capacitance and thickness of the dielectric layer. The capacitance density (C/A (fF/μm^2)) displays the capacitance per unit area in MIM capacitors. The dielectric constant (*k*) is also represented as ε_r. The dielectric constant specifies the ability of the dielectric material to store charge. It is determined by the polarizability of the dielectric material under the influence of applied electric field. The dielectric constant of the material is inversely proportional to the dielectric thickness 'd' and the capacitance of the MIM device is directly proportional to the electrode area 'A' of the capacitor. To achieve high capacitance density, selection of high-*k* material is an important parameter. Higher the dielectric constant value more will be the capacitance density. On the other hand, thickness 'd' of the dielectric layer should be as small as possible. This highly depends on the limitations of dielectric deposition technology.

3.2. Leakage current density

Leakage current density is one of the most critical performance parameters of MIM capacitor. It is proved, experimentally and mathematically, that the leakage current density is higher at high-*k* materials due to low Schottky barrier height and low effective barrier thickness [12]. The conduction mechanisms can be either bulk limited or electrode limited. The electrode limited conduction is more effective and suitable in case of thinner films and are electrode dependent. The conduction/transport of charge carriers occurs in the insulator itself. However, bulk limited conduction deals with the transport of charge carriers from the cathode into the insulator and is dominant in thicker films. Schottky emission (SE), Poole-Frenkel (PF) emission, Trap assisted tunneling (TAT) and Fowler-Nordheim (FN) tunneling are some of the dominant leakage conduction mechanisms. Each mechanism will dominate the other at various applied voltages depending on the trap distributions at the interface and bulk.

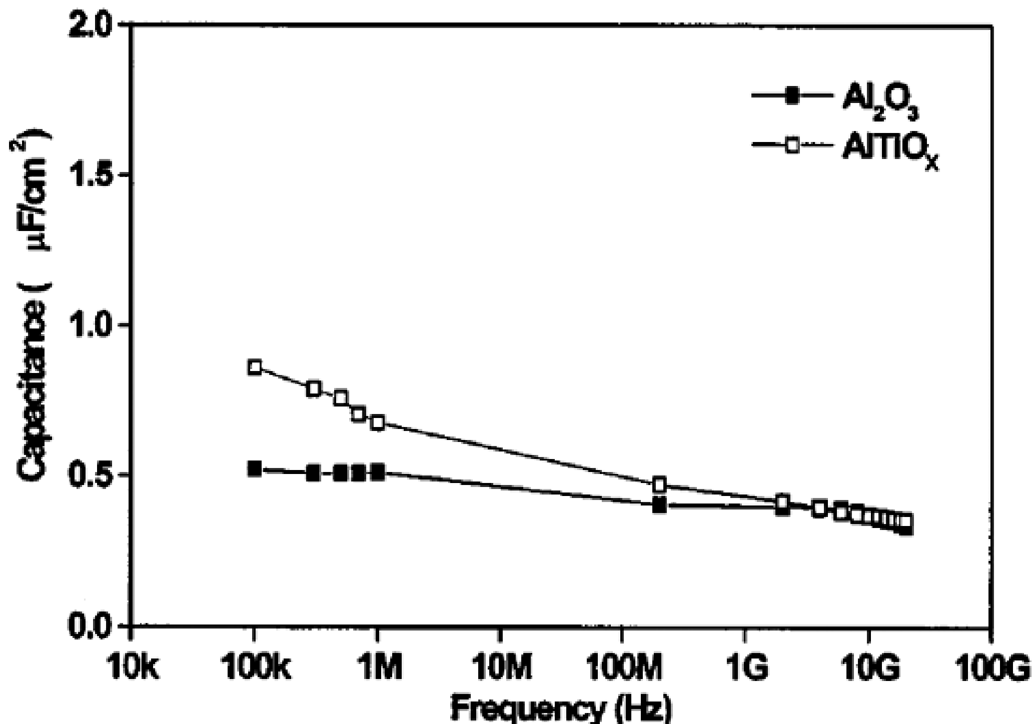

Figure 4: Frequency dependent capacitance characteristics of Al_2O_3 and $AlTiO_x$ [13].

3.3. Frequency dependence

When an AC signal passes through the MIM capacitor, the dipoles of dielectric material polarize according to the positive and negative half cycles. This rotation or polarization with electric field direction is a mechanical phenomenon which can't follow the high frequency signal, thus the polarization and polarizability of material reduces. This results in the reduction of dielectric constant with frequency increment. This effect is referred to as frequency dependence of capacitance. The rate of change of reduction in the dielectric constant with increment in frequency depends on the atomic arrangement of the dielectric material and defects. Chen *et al* showed the dependence of capacitance with frequency for Al_2O_3 and $AlTiO_x$ MIM capacitors. It shows a different rate of reduction in capacitance for the increase in frequency [13] which are shown in Figure 4. It is observed from Figure 4 that, the reduction in capacitance with frequency increment for $AlTiO_x$ capacitors is due to the high density of defects/traps and low time constant of traps available at the metal-to-oxide interface [13].

3.4. Voltage linearity

The variation of capacitance with the applied voltage is known as the voltage coefficient of capacitance (VCC). For a MIM capacitor device, the capacitance variation with voltage variation should be as small as possible. This variation of capacitance is not acceptable in few circuits, such as RF and mixed signal circuits. Voltage coefficient of capacitance is extracted using, where C_0 is the capacitance at bias voltage of zero, α, and β are the quadratic and linear coefficient of capacitance, respectively [10]. VCC of capacitors is a trade-off factor for the dynamic range of AMS circuits which should be less than 100ppm/V^2 to meet the ITRS requirements [14]. Gonon *et al* has reported on the modeling of VCC with frequency, temperature and trap density based on electrode polarization mechanism [15]. The dependence of thickness on the quadratic VCC value can be explained by the free carrier model in which the quadratic VCC is inversely proportional to the relaxation time [16]. As the thickness increases, the electric field across the dielectric decreases which results in a smaller α value.

3.5. Dielectric reliability

Breakdown voltage of the device determines the lifetime of the device. Reliability studies of the device give us the information about device performance under various conditions, such as temperature, and electrical stress. Reliability of the MIM device mainly deals with the stress applied on to the device under various time, voltage and temperature. This results in an increase in leakage current which is due to the increase in trap evolution in the dielectric layer. This phenomenon is called as Stress induced leakage current (SILC). Highly reliable MIM devices require high breakdown voltage.

3.6. Quality factor

The reciprocal of the dissipation factor is called the quality factor (Q). The dissipation factor is a measure of how much energy is lost in the dielectric under the influence of AC operation. The dielectric undergoes resistive losses when the charges in the dielectric cannot react to the applied electric field spontaneously. The voltage and current might deviate from the ideal value of 90°. This angular difference is called the loss angle (δ). It is zero for capacitor that dissipated no wasted energy.

$$Q = \frac{1}{\tan \delta} \tag{2}$$

4. CHALLENGES IN SCALING OF MIM CAPACITOR

Scaling down the size of the device is a major problem in MIM capacitor fabrication. Scaling down the thickness of the dielectric mainly depends upon the fabrication technology. It is essential to reduce the area

of the capacitor significantly as the MIM capacitors occupy a large amount of area in the digital circuits. If the chip area is reduced, this would lead to more number of compact designs at high speed with improved performance, smaller die size and at low cost [17].

The need to incorporate high density MIM capacitors with in a cost effective manner follows the standard published by International Technology Roadmap for Semiconductors (ITRS). Table 1 shows the ITRS requirements upto year 2018. According to the ITRS recommendations [14], near future devices should attain high performance characteristics (high capacitance density, low leakage current density, high breakdown voltage and high voltage linearity) as shown in Table 1. However, various high-*k* materials have been used in MIM capacitors. In spite of using the high-*k* materials in MIM capacitors, the status is that no existing high-*k* material matches with the ITRS requirements completely. Consequently, many alternative dielectric structures such as stacked or sandwiched multilayer dielectrics have been developed to optimize the properties of MIM capacitors. Achieving all the key parameters of MIM capacitors in the desired range using high-*k* dielectric materials is not a straightforward task. Using these high-*k* dielectric materials may result in high capacitance densities, but also gives us some of the challenging tasks such as high leakage current and capacitance – voltage linearity [18].

Table 1
ITRS requirements in MIM Capacitor for RF and Mixed-signal applications [14]

Year of Production	*2012*	*2013*	*2014*	*2015*	*2016*	*2018*
Capacitance density (fF//µm^2)	5	5	5	7	7	10
Voltage Linearity (ppm/V^2)	<100	<100	<100	<100	<100	<100
Leakage current density (A/cm^2)	$<10^{-8}$	$<10^{-8}$	$<10^{-8}$	$<10^{-8}$	$<10^{-8}$	$<10^{-8}$
Q Factor	>50	>50	>50	>50	>50	>50

Also, deposition technology is an important parameter in scaling. Many high-*k* dielectric materials require high temperature processing. It is known that material properties in terms of crystallinity of the dielectric material can be improved by high temperature processing [19-20]. However, high temperature processing also has some disadvantages in CMOS technology as the BEOL process is limited to a temperature of 400°C. Secondly, interface quality between the layers of the MIM capacitor stack can be degraded. Keeping all the challenging aspects discussed above in mind, one should also consider the physical and electrical characterization for the development of future MIM capacitor structures.

5. MIM CAPACITORS IN THE RF AND MIXED SIGNAL APPLICATIONS

Among the various passive components used in RF and AMS circuit applications, capacitors are the primary component needed in the phase shifter, oscillator, coupling and decoupling circuits, filter, analog - digital and digital - analog converters etc [21]. Capacitors are widely used in filters, such as high pass, band pass and low pass filters. The capacitors in general are also used to decouple a circuit from another such that the noise from one circuit is shunted and does not affect the rest of the circuit. Figure 5 shows various sub-circuits in RFICs, such as oscillator, phase shifter, decoupling capacitor, analog-digital converters. Arrays of capacitors are used in analog-digital converters to digitalize the analog signal into different discrete digital signals [22].

5.1. DRAM applications

MIM capacitors are widely used in Dynamic random access memories (DRAM). For RF and AMS applications, MIM capacitors should hold high capacitance density, low leakage current density and low voltage linearity. However, the requirements are different for DRAM. In DRAM applications, each capacitor should posses a cell size < 0.0061 µm^2 and should attain a capacitance density of 25 fF/cell and most

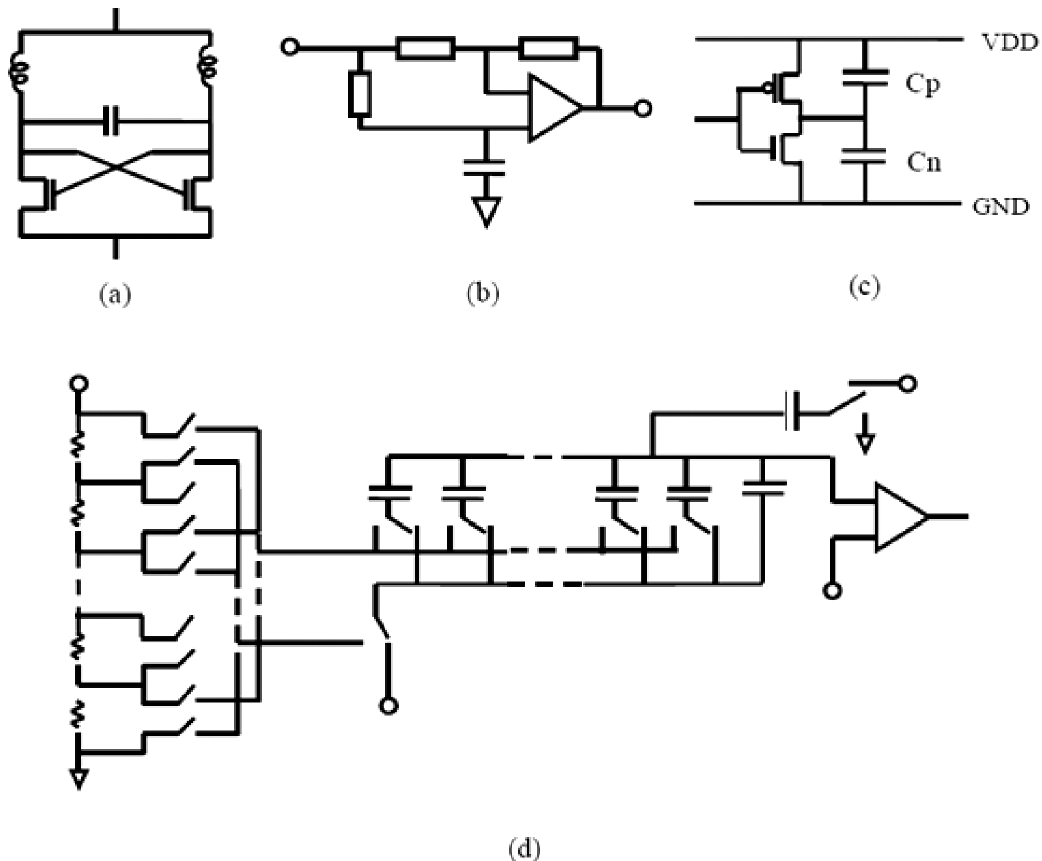

Figure 5: Applications of MIM capacitors (a) Cross coupled LC oscillator, (b) Phase shifter circuit, (c) Decoupling capacitors, and (d) Analog-digital converters.

importantly small VCC is not a prerequisite. In DRAM applications, high temperature fabrication process is required to mainly increase the capacitance density and reduce the leakage current.

6. HIGH-*K* DIELECTRICS FOR MIM CAPACITOR APPLICATION AND THE IMPORTANT CRITERIA FOR MATERIAL SELECTION

SiO_2 (k~3.9) and Si_3N_4 (k~7) materials were used in conventional MIM capacitors [23, 24, 11]. These capacitors exhibit good electrical properties but their capacitance densities are not high due to their low dielectric constants. These capacitors could not achieve the required capacitance density value projected by the ITRS roadmap [14]. However, scaling down the dielectric thickness of SiO_2 and Si_3N_4 can increase the capacitance density. But, this may offset the breakdown voltage, leakage current and voltage linearity problem [3, 25]. Van Dover *et al* demonstrated a SiO_2 MIM capacitor showing a capacitance density of 2.5 fF/µm^2 [26]. However, the achieved capacitance density is low compared to the ITRS recommendations [14]. As a result, the adoption of high-*k* materials is vital to meet the ITRS requirements of MIM capacitors for analog and mixed signal applications. Adoption of physical high-*k* dielectric films may potentially improve the electrical characteristics of the device.

Figure 6 shows the collection of a few high-*k* dielectric materials showing the relationship of band gap versus dielectric constant [9]. This provides a straight forward criterion of selecting suitable high-*k* materials as the dielectrics for MIM capacitors. It should be noted that lower band gap materials may result in the reduction of breakdown voltage [27]. High-*k* dielectrics are critically important to meet the technology demands in near future.

It has been proved that SiO_2 is the best dielectric material as an interface between Si-SiO_2. So, to be compatible with Si substrate, high-*k* dielectric materials should possess the following features [28].

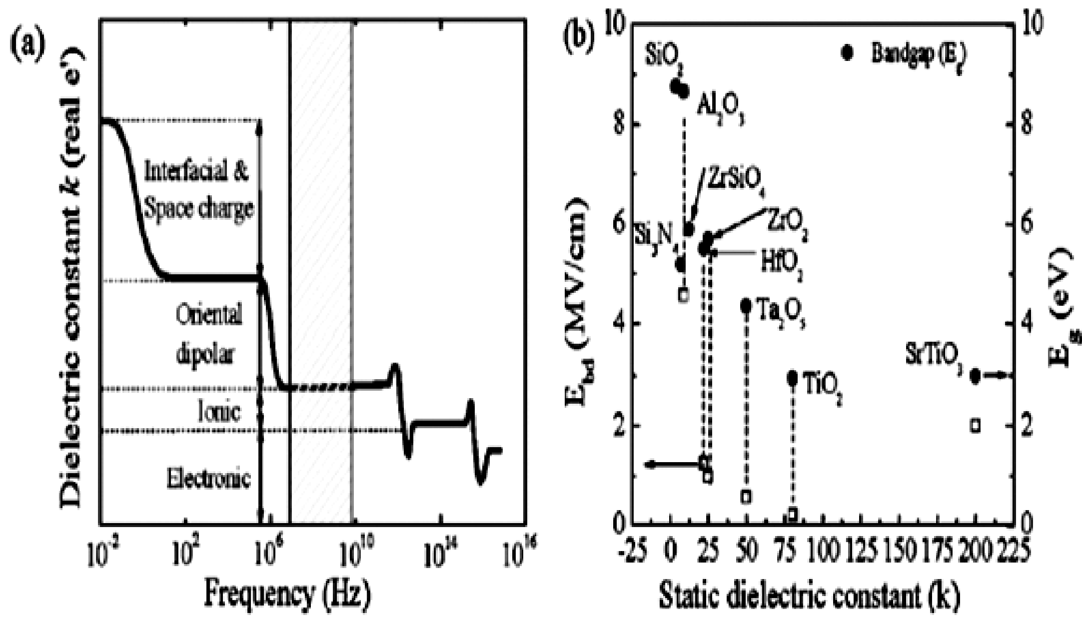

Figure 6: (a) A schematic diagram illustrating the dependence of static dielectric constant on frequency, (b) Bandgap (Eg) versus static dielectric constant (*k*) and electrical breakdown field (E_{bd}) for representative high–*k* materials [29]

Electrical properties

- High dielectric constant
- High band gap
- Low leakage currents
- Reduced charge trapping characteristics
- Negligible frequency dispersion
- High reliability at operating conditions

6.1. Material requirements and selection

The electrical characteristic of every material is dependent on its dielectric properties. Measurements of these dielectric properties can provide valuable information of material characteristics, design parameters for many electronic applications. The electrical properties of material are mainly the permittivity and permeability. The permittivity and permeability of a material are not constant, but can change with frequency, temperature, orientation, mixture, pressure and molecular structure of the material [29]. The initial evaluation for gate oxides focused on the dielectric constants, which are attributed due to polarization of ionic and electronic dipoles in the GHz frequency frame which is needed for RF and Analog/Mixed signal devices, as shown in Figure 6 (a) [29]. The dielectric response is mainly based on ionic and electronic polarization at high frequencies, which guides a metal element that forms an ionic bond with oxygen and has a large atomic number (number of electrons). Each of these polarization mechanisms are a function of the frequency of the applied field. When the frequency of the applied field is sufficiently low, all types of polarizations can reach the value they would have at steady field equal to the instantaneous value of alternating field. But as the frequency increases, the polarization no longer has time to reach its steady peak value. Electronic, atomic, and orientation polarization occur when charges are locally bound in atoms, molecules, or structures of solids or liquids. Some of the charge carriers may migrate over a distance through the material when a low frequency electric field is applied. Interfacial or space charge polarization occurs when the motion of

these migrating charges is impeded. The charges can become trapped within the interfaces of a material. Motion may also be impeded when charges cannot be freely discharged or replaced at the electrodes. The field distortion caused by the accumulation of these charges increases the overall capacitance of a material. A relaxation effect is usually associated with orientation polarization. Relaxation time *ô* is a measure of the mobility of the molecules (dipoles) that exist in a material. It is the time required for a displaced system aligned in an electric field to return to 1/e of its random equilibrium value (or the time required for dipoles to become oriented in an electric field). Transition metal oxides thus emerged as promising candidates, especially for those of heavy metal elements to maximize the dielectric constants [29].

Dielectric constant, Energy band-gap, electron affinity, and frequency dependent dielectric constant are some of the intrinsic parameters involved in the selection of a good dielectric material. These parameters are related to each other by their atomic interactions which are determined by their phase and chemical compositions. The material can be either amorphous or crystalline depending upon the process conditions. However, it is realized that a general compromising relationship exists for these materials between the static dielectric constant (k), the attainable bandgap (E_g), and the electrical breakdown field (E_{bd}), as shown in Figure 6 (b). This behaviour is expected qualitatively since stronger polarizability implies weaker bonding, and weaker bonding implies a small separation between bonding and anti–bonding energies [30]. Therefore, it is not possible to maximize k, E_g and E_{bd} simultaneously for a simple binary oxide. They need to be carefully balanced to optimize the performance of different devices and circuits. In general, a promising high–*k* material should have a dielectric constant between 10 and 30, a bandgap above 5eV, and band offsets with a semiconductor substrate above 1eV to minimize carrier injection.

Several high–*k* materials have been investigated as alternative to SiO_2 gate oxide such as Si_3N_4, Ferro–electric materials such as ferroelectric titanates ($Ba_xSr_{1-x}TiO_3$ and $SrTiO_3$. Metal oxides such as Ta_2O_5, TiO_2, Al_2O_3, ZrO_2, and HfO_2; and silicates such as $HfSi_xO_y$ and $ZrSi_xO_y$ [31-38]. Unfortunately, each of these materials is found to have its drawbacks. A particularly important consideration is that the selection of high–*k* dielectric materials should be scalable to future technology generation. Because of immense cost associated with developing high–*k* dielectric materials in replacing the SiO_2. Though a careful balance of all important requirements for a gate dielectric material, hafnium based materials emerged over the last decade as the designated dielectrics for future generation of nano scale devices and was successfully introduced into production in 2007 [39].

7. REVIEW ON HIGH-*K* MATERIAL BASED MIM CAPACITORS

This section explains the various high-*k* dielectric materials used in single and multilayer MIM capacitors.

7.1. Silica or Si based oxides

The bandgap of dielectric material is inversely proportional to the dielectric constant [40,41]. It is shown that effective barrier thickness of high-*k* MIM structure decreases with increment in permittivity [41]. High-*k* dielectric stack engineering in fabrication of MIM capacitor was used to address these issues. Usually, a thin barrier layer of large bandgap dielectric material (Al_2O_3, SiO_2) is stacked with very high dielectric constant material (ZrO_2, TiO_2 and HfO_2). Most of the quadratic VCCs of the MIM capacitors using single layer high-*k* dielectric are positive while the MIM capacitor with SiO_2 has a negative quadratic VCC. The positive quadratic VCC can be explained by using ionic polarization or electrostriction models [42-43]. However, these models cannot explain the negative quadratic VCC of SiO_2. But, the negative quadratic VCC of SiO_2 was modeled by Phung *et al* [44]. This model was explained by summing electronic, ionic and orientation polarizations. However, ionic and orientation polarization is independent of electric field. The orientation polarization was reduced by increasing electric field there by giving rise to a negative quadratic VCC in SiO_2. It is demonstrated that quadratic VCC of SiO_2 is inversely proportional to the

square root of its thickness [44]. Also, it was observed that a post deposition anneal at 400°C reduced the value of quadratic VCC significantly [44]. Si_3N_4 displayed a negative quadratic VCC under certain processing conditions [45].

Few works exploited the SiO_2 characteristic of having negative quadratic VCC to achieve a small quadratic VCC. Kim S J *et al* have stacked 12nm ALD HfO_2 on 4nm PECVD SiO_2 and demonstrated an MIM capacitor which resulted in a capacitance density of 6fF/µm^2 and a quadratic VCC of 14ppm/V^2 [46]. Dielectric stack of $Pr_2Ti_2O_7/SiO_2$ MIM capacitor was demonstrated to show a smaller quadratic VCC less than 100ppm/V^2. However, this capacitor showed a capacitance density of 3.2fF/µm^2 [47]. This was due to the change in the thickness ratio of stacked materials. By slightly changing the thickness ratio of both the materials, a high capacitance density and low quadratic VCC can be simultaneously obtained. However, this method may cause high leakage current in the device which can be reduced by improving the quality of the high-*k* dielectric material.

Recently, MIM capacitors with crystalline-TiO_2/SiO_2 dielectrics have received attention. These capacitors show a high capacitance density of ~11.9fF/µm^2 and a low quadratic coefficient of capacitance 90ppm/V^2 [48]. The high dielectric constant value of crystalline TiO_2 increases the capacitance density [48]. Amorphous SiO_2 provides a negative quadratic VCC to cancel out the positive quadratic VCC from the crystalline TiO_2. Additionally, an effect of N_2 plasma treatment on the TiO_2 film reduces the quadratic VCC by 30ppm/V^2 with a slight degradation in capacitance. Park *et al* demonstrated the Quadratic VCC for ZrO_2-SiO_2 multilayered dielectric MIM capacitors [49]. It was demonstrated that quadratic VCC value depends up on the stacking sequence of the layered dielectrics. This fabricated capacitor showed a stacking sequence of $SiO_2/ZrO_2/SiO_2$ and $ZrO_2/SiO_2/ZrO_2$ which obtained a quadratic VCC of +42 and -1094ppm/V^2 [49]. This difference was observed in the stacking sequence and was explained by taking into account both the interface and bulk dielectric reactions to the applied voltage. It also explained the effect of interface on VCC by considering single layer SiO_2 MIM capacitor.

7.2. Dielectrics with Hf based oxides

Significant interest has been paid to IV–B metal oxides, especially HfO_2, ZrO_2 and TiO_2 as alternative gate dielectrics to SiO_2. But compared to ZrO_2 and TiO_2, HfO_2 is considered the most promising due to its large band-gap (5.5 - 6.0), relatively high dielectric constant (22-25), high breakdown field (3.9–6.7 MV/cm), high thermal stability and large heat of formation (271 kcal/mol). The effect of crystal structure on material properties including stability, dielectric constant, and bandgap has been recognized to be of great fundamental and technological importance. Most commonly, HfO_2 material has been used in single layer, multi-layer laminate structures due to its very good material properties.

Reports are available on HfO_2 stacked on Al_2O_3 dielectric based MIM capacitor for RF applications [19, 50]. The $Al_2O_3/HfO_2/Al_2O_3$ (AHA) MIM capacitor fabricated using ALD showed a low leakage current density (1×10^{-9} A/cm^2 at 3.3V), high capacitance density (3.13fF/µm^2) with low VCC (100ppm/V^2) and high reliability (3.3 MV/cm) [50]. Similarly, a high capacitance density (12.8fF/µm^2), low leakage current density (7.45×10^{-9} A/cm^2 at 2V) and high quadratic VCC (1990ppm/V^2) were demonstrated with A-H-A-H-A laminated dielectric structures using ALD method, The thickness of the materials A (Al_2O_3) and H (HfO_2) are 1nm and 5nm respectively [19]. Sung Kyun *et al* demonstrated $Al_2O_3/HfO_2/Al_2O_3$ (1nm/15nm/1nm) based MIM capacitors using PECVD method. This capacitor exhibited a capacitance density of 8fF/µm^2, and quadratic VCC of 1000ppm/V^2. It is demonstrated that quadratic VCC can be reduced by tuning the Al_2O_3 to HfO_2 ratio. But, this is traded off by a lower breakdown voltage [51].

Jeong Yong-kuk *et al* have demonstrated $Ta_20_5/HfO_2/Ta_20_5$ based MIM capacitor using MOCVD method [52].This capacitor exhibited a capacitance density of 4fF/µm^2, low leakage current density of 100nA/cm^2 at 125°C and quadratic VCC of 16.9ppm/V^2. Pernga Tsu-Hsiu *et al* demonstrated a single layer HfO_2 MIM

capacitor using Sputtering method. The capacitors with different top electrodes like Aluminium, Tantalum, and Copper were deposited on HfO_2 dielectric and the electrical properties were compared. It is observed that capacitors with Al as the top electrode exhibited a low leakage current and low capacitance compared to Ta and Cu [53]. This was due to the formation of Al_2O_3 layer between Al and HfO_2. $HfO_2/HfO_xC_yN_z/HfO_2$ (HNH) MIM capacitor using PEALD method was demonstrated by Park *et al*. This capacitor resulted in a capacitance density of 8.8fF/μm^2, a leakage current density at 3V of 1.5×10^{-8}A/cm^2 and a quadratic VCC of 700 ppm/V^2. This capacitor exhibited an enhanced time dependent dielectric breakdown (TDDB) characteristic and low quadratic VCC compared to Al_2O_3/HfO_2 MIM capacitor. This was due to the $HfO_xC_yN_z$ layer which suppressed the crystallization of HfO_2 [54].

Kamel *et al* studied the electrode effects on the leakage current conduction mechanisms in HfO_2 based MIM capacitors [55].In his work, top electrodes such as aluminium, chromium and gold were used by keeping platinum as the bottom electrode for all the structures. It was shown that an Al/HfO_2 and Cr/HfO_2 interface were governed by the Fowler–Nordheim tunneling. The MIM capacitors with HfLaO/$LaAlO_3$/HfLaO (HLH) dielectric stack was deposited by ALD. This capacitor showed to have similar quadratic VCC and superior leakage current compared to those of MIM capacitors with AHA stacked dielectric [56]. This capacitor displayed a capacitance density of 7.4 fF/μm^2 and had a leakage current at 3.3V of 3×10^{-9}A/cm^2, and a quadratic VCC of 700 ppm/V^2 [56]. HfO_2 MIM capacitor was fabricated using ALD [57]. The structural properties were improved by H_2O prepulsing treatment on bottom electrode before the deposition of HfO_2. This treatment leads to the reduction of oxygen vacancies in the bottom Pt electrode which improves the quadratic VCC and leakage.

Kwak Ho-Young *et al* have demonstrated Al_2O_3–HfO_2–Al_2O_3 sandwiched MIM capacitor using ALD method and studied its electrical properties under AC and DC stress. It was observed that variation of capacitance ($\Delta C/C_o$) increases and the variation of voltage linearity (α/α_o) decreases with stress time which was due to the charge trapping behavior [58]. The trapped charges resulted in the decrease of carrier mobility in the dielectric material due to the electrostatic scattering. This in turn reduced the quadratic VCC. This behaviour obeys the free carrier injection model [59] .This variation was observed at both positive and negative bias regions.

Recently, Park In-Sung *et al* have demonstrated the effect of Al_2O_3 and HfO_2 dielectric stack in MIM capacitors using ALD method. It is reported that to achieve a higher capacitance, a thin layer of Al_2O_3 and a thick layer of HfO_2 should be employed. 3, 5 and 7 layer stacking sequence was shown. They concluded that compared to single layer; the three layer structure improves the dielectric permittivity and voltage linearity. Whereas stacking over five layers reduces the leakage current density and breakdown voltage characteristics. This was due to the blocking of current through the grain boundary channels which attributed to the enhancement of leakage current. Also, interfaces between the dielectric layers play a role to avoid the charge from flowing at the end of the conduction path [60].

7.3. Dielectrics with Al based oxides

Al_2O_3 material has achieved considerable amount of interest in fabrication of MIM, MOS capacitors [13, 61]. This material exhibits good characteristics in terms of low TCC, lesser frequency dispersion, low leakage and low loss tangent [13,62].Although Al_2O_3 has a comparable band-gap (~8.7eV) with that of SiO_2 (~8.9eV), its dielectric constant is low (k~9) to achieve high capacitance density. But, it results with low leakage current density due to its high band-gap [63]. However, its dielectric constant is too low compared to other dielectric materials such as TiO_2 (60-100), HfO_2 (~25), Ta_2O_5 (~26). To achieve a high capacitance density, many efforts were put to increase the capacitance density by intermixing or combining this dielectric material with other dielectric materials to exploit the advantages of their own materials so that the voltage linearity and leakage current density can be improved. Chen *et al* has demonstrated the single layer Al_2O_3 MIM capacitor using sputter (PVD) [13]. The quadratic and linear voltage co-efficient of

capacitance reported are 2051ppm/V^2 and 1888ppm/V at 1MHz respectively. It showed a capacitance density of 5.2fF/µm^2 and low leakage current density of 4.3×10^{-8} A/cm^2 at 1V.

Hang H *et al* has investigated the intermixing of HfO_2 and Al_2O_3 to form Hf-Al-O dielectric. The combination of these materials was done to investigate the merits of high permittivity of HfO_2 and high energy band-gap of Al_2O_3. It resulted a capacitance density of 3.5fF/µm^2 and low quadratic VCC of 190ppm/V^2 [64]. $AlTiO_x$ MIM capacitor was reported to have high capacitance density of ~10fF/µm^2. But, the leakage current density is still poor (Chen S B *et al* (2002)). However, stacks of Ta_2O_5/HfO_2/Ta_2O_5 MIM capacitors were investigated [52].It is demonstrated that laminating or sandwiching the dielectric materials of Ta_2O_5/Al_2O_3 or Ta_2O_5 between Al_2O_3 can effectively result in a reduction of leakage current density [65]. This is due to the Al_2O_3 layer which can be a barrier for diffusion of oxygen ions into the bottom metal contact interface at the time of Ta_2O_5 deposition. Hang *et al* demonstrated a multiple laminated Al_2O_3/ HfO_2/ Al_2O_3/HfO_2/Al_2O_3 (1nm/5nm/1nm/5nm/1nm) stacked MIM capacitor using ALD method [64].The objective of this structure was to reduce the leakage current density by increasing the energy band-gap in the intermixed film after the addition of Al_2O_3 layer. Also the use of Al_2O_3 layer on both the sides improves the metal/dielectric interface quality.

Wenger *et al* demonstrated the laminated Al_2O_3/Pr_2O_3/Al_2O_3 MIM capacitor for RF applications using electron beam evaporation [47]. This capacitor exhibited a capacitance density of 5.7 fF/µm^2 and low leakage current density of 5×10^{-9} A/cm^2 at 1V. Wu Yung-Hsien *et al* demonstrated the MIM capacitor using dielectric stacks of ZrO_2/Al_2O_3/ZrO_2 for Analog and RF applications using ALD method. It is observed that a high capacitance density of 21.54 fF/µm^2 is achieved due to the high dielectric constant of ZrO_2 (~38.7). Also, it resulted in a low leakage current density of 2.11×10^{-6} A/cm^2 at 2 V which due to the presence of high band-gap Al_2O_3 layer [66].

Single layer $SrTiO_3$ and stacked Al_2O_3/$SrTiO_3$/Al_2O_3 structure have been fabricated on different electrodes using ALD. The electrical characteristics of both single layer and stacked layer structure were analyzed and compared [67]. Reduction of leakage current was observed in multi-layer stacked dielectrics compared to single layer $SrTiO_3$ dielectric. Also, reduction in capacitance density was observed in multi-layer structure due to the amorphous $SrTiO_3$. Al_2O_3 on both the sides prevented the crystallization of SrTiO3. This amorphous structure reduces the effective dielectric constant of the stacked structure and also reduces the leakage current [67].

Lee Jung-Hsiang *et al* demonstrated the Ni/Nb_2O_5/Al_2O_3/Ni_2Si MIM capacitor using ALD (Al_2O_3) and RF Sputtering (Nb_2O_5). This capacitor showed a capacitance density of 31fF/µm^2 and leakage current density of 3.3×10^{-7} A/cm^2 at 1V. For this capacitor structure, Laser annealing process has been carried out to enhance the capacitance density. It was observed that capacitance density values changed with increasing laser energy [68]. Recently, Woo Jong-Chang *et al* have demonstrated the MIM capacitor with Al_2O_3/TiO_2/Al_2O_3 as dielectric materials using PEALD (Plasma-enhanced atomic layer deposition). This capacitor was fabricated for different thickness and its electrical properties were analyzed. Al_2O_3/TiO_2/Al_2O_3 (3/20/3 nm) and (6/20/6 nm) thin films resulted in a capacitance density of ~19.48, 20.13fF/µm^2 and leakage current density of 5.2×10^{-13}, 1.5×10^{-13} A/cm^2. With the advantage of Al_2O_3 (high band-gap) and TiO_2 (high dielectric constant), the fabricated capacitors exhibited good electrical properties [69].

7.4. Dielectrics with Ti based oxides

Titanium oxide or Titania (TiO_2) is an attractive material evolved with considerable amount of interest in MIM capacitor fabrication. TiO_2 has a high dielectric constant (40-170) and naturally exists in 3 crystalline phases namely rutile, anatase and brookite with energy band-gap (~3.0eV) [70]. The capacitance value can be high due to the high dielectric constant. But, this material has a relatively lower band-gap which in turn results in a high leakage current.

TiO_2 MIM capacitors have been fabricated using thermal oxidation [71] and DC magnetron sputtering [72]. Thermal oxidation and DC magnetron sputtering yield MIM capacitor with high leakage current density (>10^{-4} A/cm^2) and capacitance variation $\Delta C/C_0$ of more than 104ppm [71-72] This is due to the structural defects/traps available in bulk oxide and near to metal/insulator interface. MIM capacitor with TiO_2 as the dielectric material was fabricated using electron beam evaporation method processed at 300°C [73]. This capacitor exhibited a capacitance density of 28 fF/µm^2 and leakage current density of 3×10^{-8} at -1V. Lin *et al* fabricated TiO_2/ZrO_2 stacked dielectric structure for MIM capacitor applications using ALD (ZrO_2) and PVD (TiO_2). This capacitor exhibited a capacitance density of 38fF/µm^2 and leakage current density of 3×10^{-8} A/cm^2 at 1V. To improve the dielectric property, an O_2 post deposition annealing (PDA) at 400°C was employed [74].

8. CONCLUSION

This paper presents a detailed review of MIM capacitors with various high-*k* dielectric materials. It gives a comparative observation of performance parameters and limitation of recent fabrication trends in MIM capacitors.

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