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Design of an Ultra-low Power Multiplier using Dual Mode Transmission Gate Diffusion Input

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ABSTRACT

This paper enlightens an ultra-low power Dual Mode Transmission Gate Diffusion Input (DMTGDI) Logic design of a two-bit binary multiplier. This logic aggrandizes the main attributes of Gate Diffusion Input (GDI) and Dual Mode Logic (DML). An archetypal processor's central processing unit apportions a considerable amount of processing time in executing arithmetic operations, notably multiplication executions. Nearly 9% of all the instructions in an archetypal processing unit are utilized for multiplication. It is observed that the multiplier designed with DMTGDI technique consumes very less power when compared to the conventional CMOS multiplier. With such low power consumption, delay is least affected and we have achieved an acceptable results for power delay product (PDP). Also, there is 40% reduction in total transistor count for DMTGDI multiplier. The simulations are performed using Pyxis Tool in Mentor Graphics.

Keywords: Binary Multiplier, DML, DMTGDI, GDI, Mentor Graphics, Pyxis Tool.

1. INTRODUCTION

Battery operating mobile devices have been fabulously developed in recent years and the modern portable technologies reflex almost every aspect of our lives. So, design of ultra- low power devices and circuits is exceedingly important nowadays. Designing a sub-threshold circuit design is a trivial method for reducing power consumption, because the minimum energy point (MEP) of a digital system, if available, is assuredly located in sub-threshold region [1]. But the constraints and sensitivities of the circuits in sub-threshold region increases when compared with above threshold operation [2,3]. One of the most convincing limitations is the performance of the circuit that is afflicted by supply voltage and markedly depraved in sub-threshold region. Hence, the vital demand is to improve the performance of sub-threshold circuits. So, numerous logic families have been introduced in [4,5] and [6]. One of the most compelling logic families is Dual Mode Logic (DML) can switch between static and dynamic modes [7]. DML gates can be implemented using standard static CMOS logic. An additional mode select transistor is present and therefore a large number of transistors are required to design the circuit, especially for creating complex functions.

Gate Diffusion Input (GDI) is another low power logic in the logic family and is composed of just two transistors. An ample range of dual input logic functions can be implemented with a greater pace and less power consumption when compared to standard CMOS or pass transistor logics [8]. The drawback of the GDI cell is that it gives a reduced output swing for some combinations, but this can be rectified using two buffers, which in turn increases the power consumption [9]. Another solution to this is using transmission gate diffusion input logic (TGDI) which is an enhanced version of GDI logic family, which rectifies the problem of reduction in the output voltage without any addition of buffers. In the next step, we use Dual Mode TGDI

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logic or DMTGDI logic [18]. Finally performance and power consumption of a conventional CMOS has been investigated and compared to DMTGDI logic for implementation of a 2-bit binary multiplier block.

2. TGDI CELL STRUCTURE

Basic structure of a TGDI cell is created by substituting each transistor of GDI cell with a transmission gate. Fig.1 and Fig.2 depicts the GDI and basic TGDI dual input cells respectively. As TGDI logic functions on complementary inputs, it would be more agreeable to have complementary outputs as well. The size of the transistor used in the logic is analogous to that of an inverter in standard CMOS logic.

Also, we apply forward body biasing (NMOS body to GND and PMOS body to VDD) to this structure so regular p-well CMOS processes can be used for its fabrication [9]. An ample range of complex logic functions can be implemented with GDI cell by the use of only two transistors. At ûrst glance, GDI structure (Fig.1) looks identical with the standard CMOS inverter but main variation is that there are three inputs in a GDI cell (G, P and N) and by changing the input conûguration of the simple GDI cell, we can obtain different Boolean functions whereas most of these functions become complex to be designed using CMOS method [8].

GDI (and also TGDI) logic can be considered as some kind of pass transistor (or transmission gate) logic but the main contrasting feature is that in a traditional pass transistor or transmission gate logic, the top-down logic design is very complex. This impedes production of a simple and universal cell library with these logics [8].

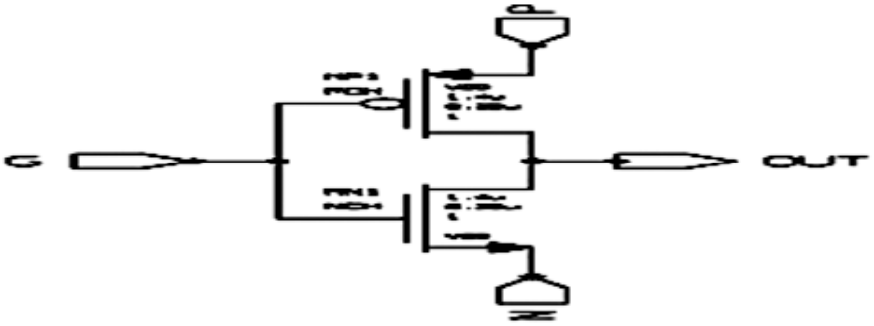

Figure 1: GDI cell [8]

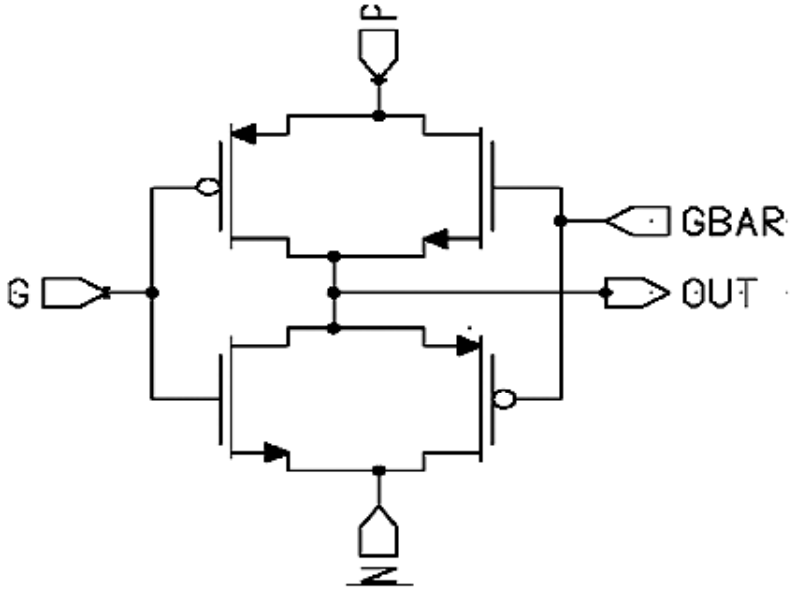

Figure 2: TGDI cell [18]

GDI logic is apt for the design a low power fast circuit that uses an abridged number of transistors (as compared to CMOS logic), but the output voltage swing is reduced for some input combinations. So, we require additional buffer stage to tackle this issue which in turn results in increased power consumption [9]. So an augmented version of GDI logic family called transmission gate diffusion input (TGDI) logic is introduced, in which rectifies the problems of output voltage swing without using additional buffer stage.

Analytical expressions of the GDI logic cell have been discussed in [8]. Here the main focus is on the differences between TGDI and GDI logics. The ûrst leverage is the commensurable structure of TGDI logic for P and N inputs. Different functions can be realized with the same delay and power consumption in TGDI logic. Thus, it is viable to analyze only the upper half of TGDI cell and broaden its outcome to the entire circuit.

In Fig. 3, when both NMOS and PMOS transistors are ON and the output node will be charged or discharged depending on P-input level in this circuit. The drain and source terminals of the transistors at the time of charging and discharging are shown in Fig. 4.

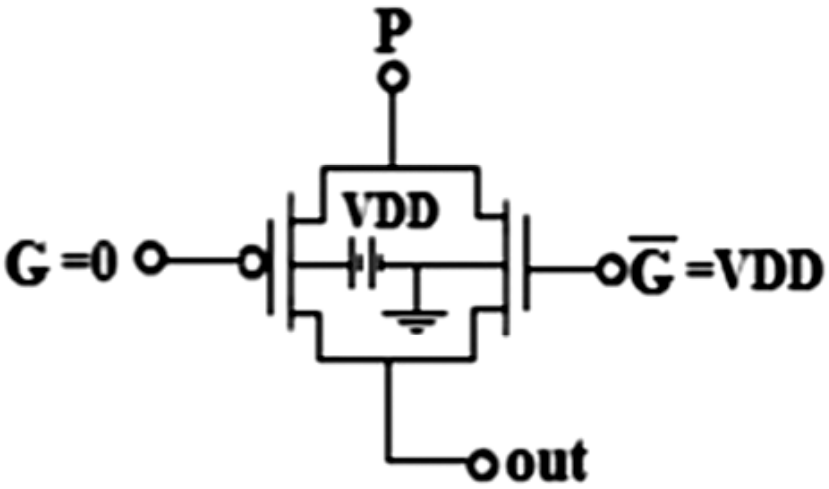

Figure 3: Upper half of TGDI circuit [18]

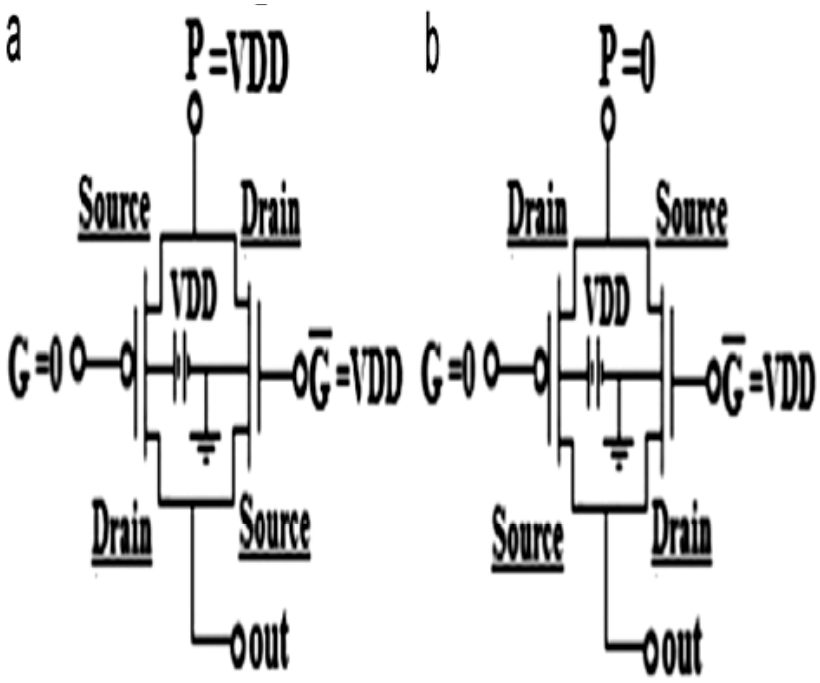

Figure 4: Drain and source terminals during (a) Charging (b) Discharging [18]

As only a single NMOS and PMOS transistor is present in GDI during charging or discharging, the switching speed lessens considerably during one of the charging or discharging events. It can be marked as the 2nd advantage of TGDI logic. Furthermore, the pass output swing and the noise margin would be dramatically dwindled if only one transistor is used in charging (discharging).

It should be quoted that TGDI requires more number of transistors when compared to the un-buffered GDI logic. However at this level of voltage, a buffer stage is required by GDI after two stage logic in order to produce a booming output signal. Also, there is a tradeoff between delay and power due to the reduced delay of TGDI. This infers that, in AND gate, for example, if we decrease the supply voltage by 40% in TGDI logic, we will be able to achieve similar delay in GDI and TGDI, while power consumption of TGDI is reduced by 60% which is almost 66% percent lower than average power of GDI logic. Since only a single NMOS or PMOS transistor is used in GDI during charging or discharging, during one of the charging or discharging events switching speed deteriorates considerably. This can be marked as the second advantage of TGDI logic. Furthermore, the output voltage swing and noise margin will be adequately reduced if we use only one transistor for charging (discharging) cell.

3. DUAL MODE TGDI

We can effectively enhance the performance of digital circuits by using dynamic logics like domino logic [13]. But they become unsuitable for nanoscale technologies because of their high sensitivity to process variations. DML is a recently introduced logic in the logic family that has the capability to switch between static and dynamic modes of operations depending upon the clock applied as input [7]. When compared to standard CMOS logic, DML has surpassing performance and subjacent power dynamic and static mode respectively. The conventional DML structure is shown in Fig. 5.

In DML, the transistor M1 and all parallel transistors with M1 in pull-up or pull-down network should be designed to have the minimum size, at the same time, the remaining other transistors in complementary network are sized according to the standard CMOS logic [11]. In static mode, M1 goes off (clk¼ VDD) and DML structure becomes similar to standard-static CMOS logic with an extra parasitic capacitance (M1). But when we use the above mentioned sizing, it results in less power consumption. Also in dynamic mode,

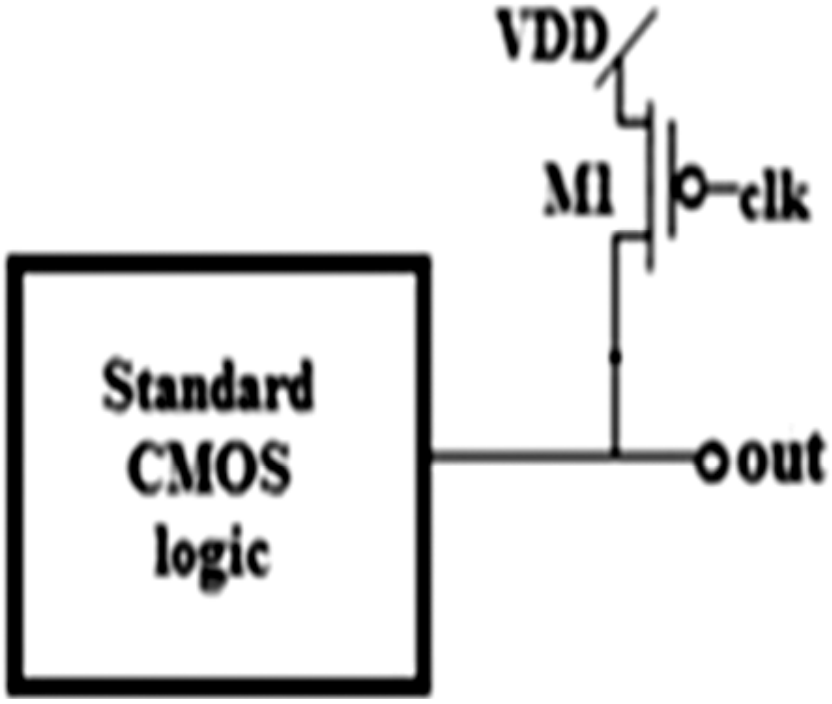

Figure 5: Conventional Dual Mode Logic Cell [7]

an asymmetric clock is applied to M1 and creates pre-charge and evaluation phases. By replacing the standard CMOS block with TGDI network we can obtain DMTGDI logic as depicted in Fig. 6.

4. 2-BIT BINARY MULTIPLIER

A binary multiplier is a circuit used in digital electronics, such as a computer, to multiply two binary numbers. A two bit binary multiplier contains and two AND gates and two half adders. The techniques involved here are computing a set of partial products from the adders and the AND gates, and then summing these partial products together.

This process is similar to the long multiplication on base-10 integers, but are modified here for applying to a base-2 (binary) numeral system. The first stage of most multipliers involves generation the partial products which involves nothing but AND gates. The partial products are then added to give the final results.

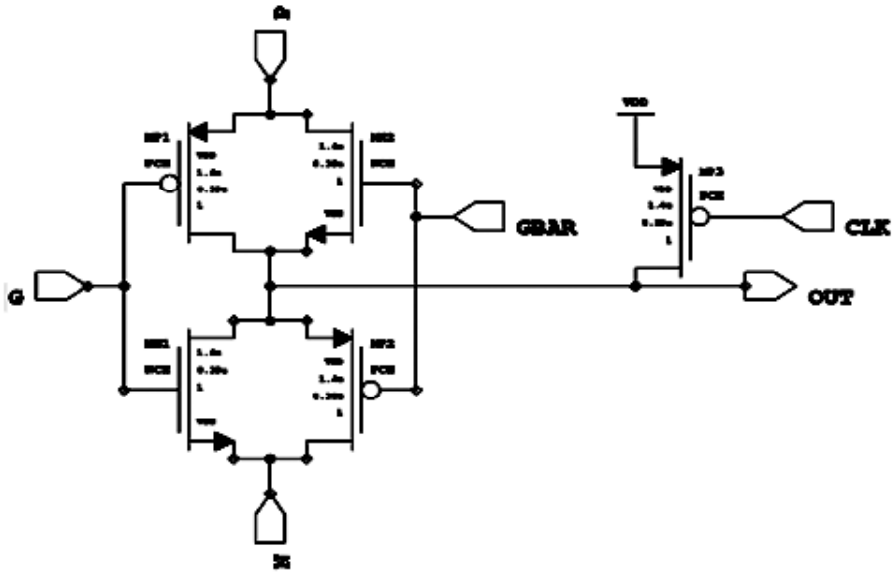

Figure 6: DMTGDI logic Cell [18]

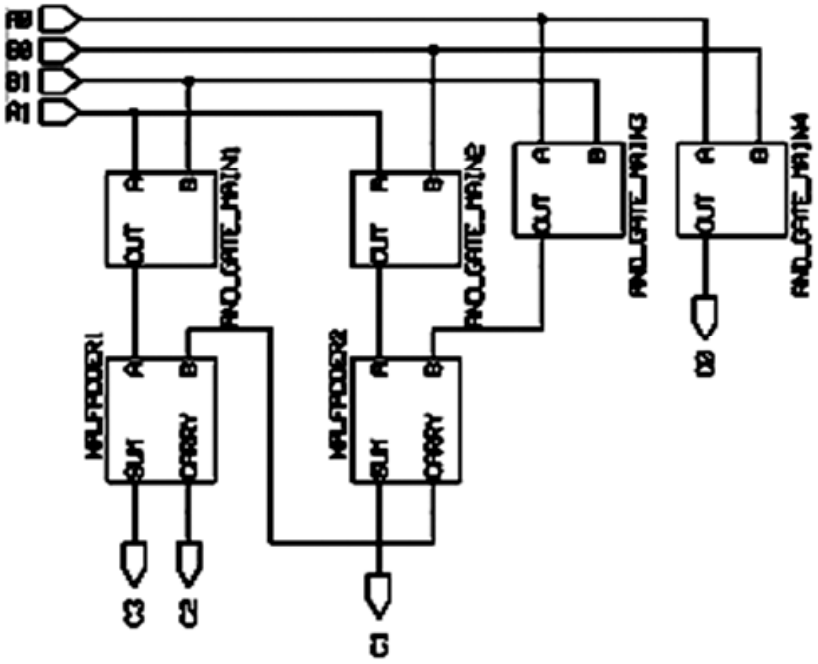

Figure 7: Block Diagram of 2-Bit Binary Multiplier using CMOS

The block diagram of a 2-bit binary multiplier is shown in Fig. 7. The operations performed are as follows:

$$C_0 = A_0.B_0 \quad (1)$$

$$C_1 = A_0.B_1 \oplus A_1B_0 \quad (2)$$

$$C_2 = C_1 \oplus A_1B_1 \quad (3)$$

$$C_3 = A_1B_1C_1 \quad (4)$$

Here, (1) gives the output C_0 from the AND gate which takes A_0 and B_0 is its input. The third AND gate takes A_0 and B_1 as input and its output is fed as second input to the second half adder. Similarly the second AND gate takes A_1 and B_0 as its input and its output is fed as the first input to the second half adder. The second half adder generates two outputs SUM C_1 and CARRY, of which the CARRY output is fed as one of the inputs to the first half adder. (2) Shows the output C_1 generated from the second half adder. The first AND gate takes A1 and B1 as input and its output is fed as input to the first half adder. This first adder generates output as C2 and C3 as shown in (3) and (4).

The schematic of a two input AND gate is shown in fig. 8. This is designed using standard CMOS logic and uses a total of six transistors.

The schematic of two input XOR gate is shown in Fig. 9 and is designed using standard CMOS logic.

A half is designed using a two input XOR gate which gives SUM as its output and an AND gate which generates CARRY output for the circuit as depicted in Fig. 10. A two input AND gate is designed using DMTGDI logic and is depicted in Fig. 11.

Fig. 12 depicts a half adder circuit using DMTGDI logic. It uses an extra clock input to the transistor connected at the output terminal of the circuit. This extra transistor is helpful in switching the circuit between static and dynamic mode. The XOR gate gives SUM as its output and the AND gate generates CARRY output for the circuit.

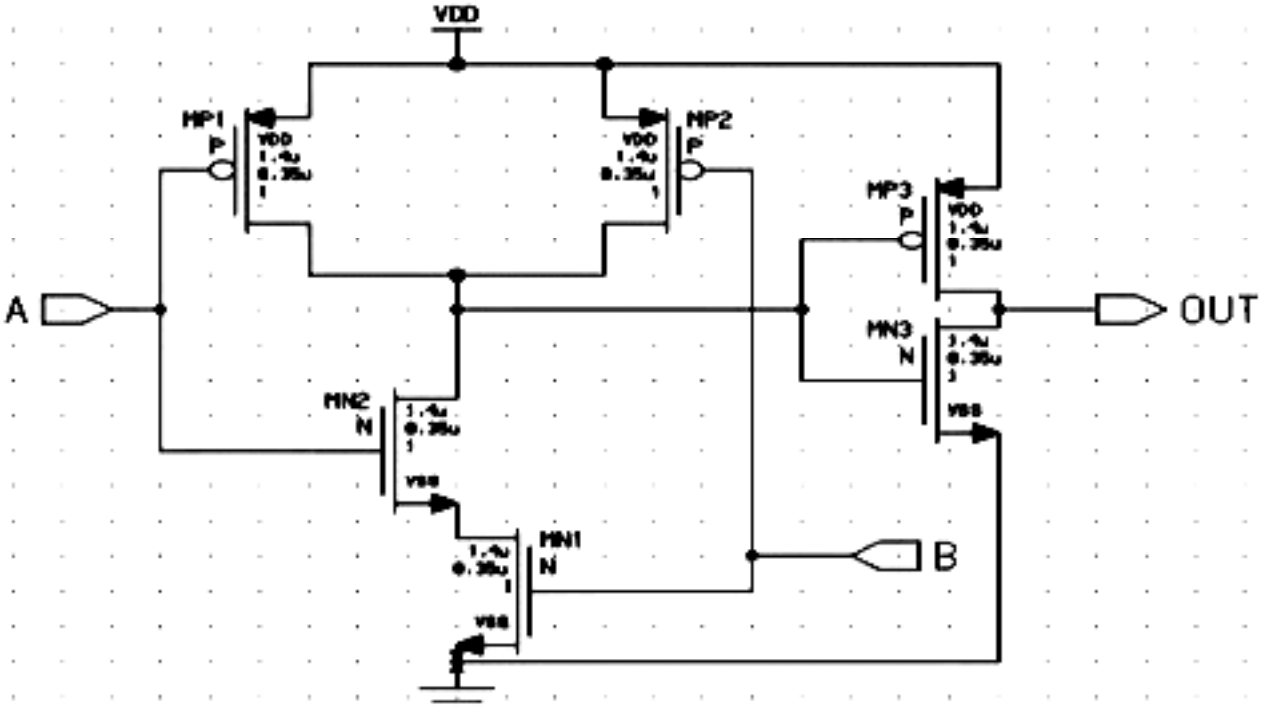

Figure 8: CMOS AND Gate

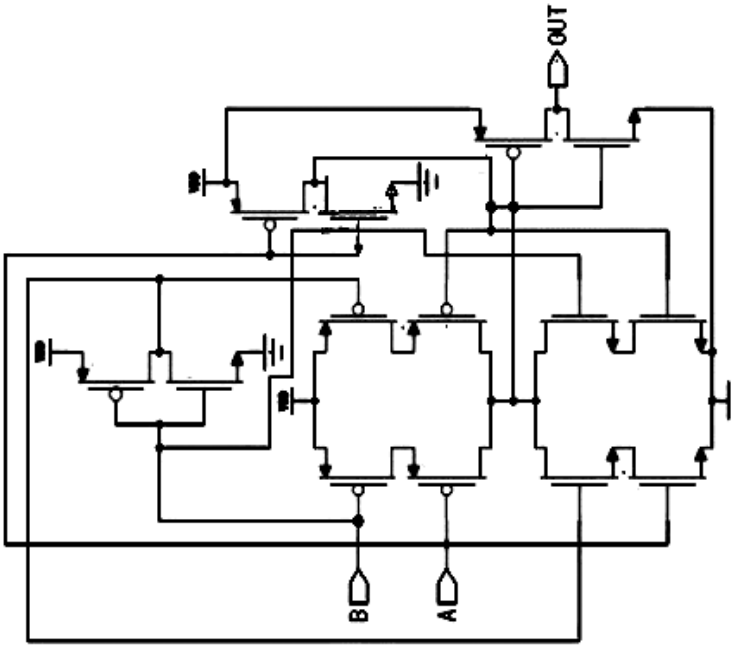

Figure 9: CMOS XOR Gate

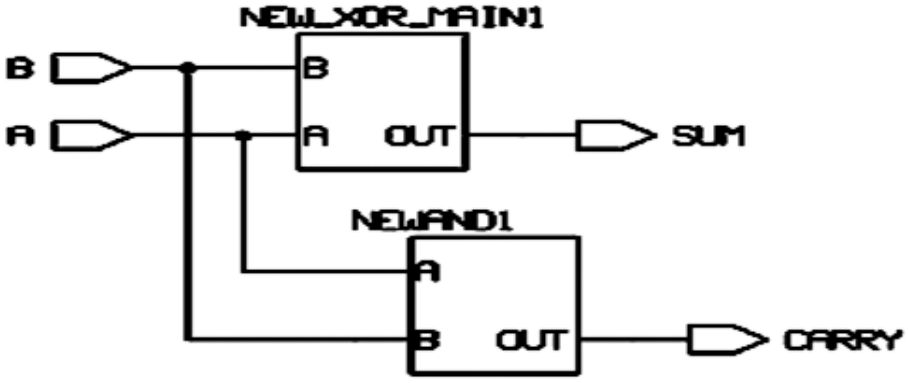

Figure 10: CMOS Half Adder Circuit

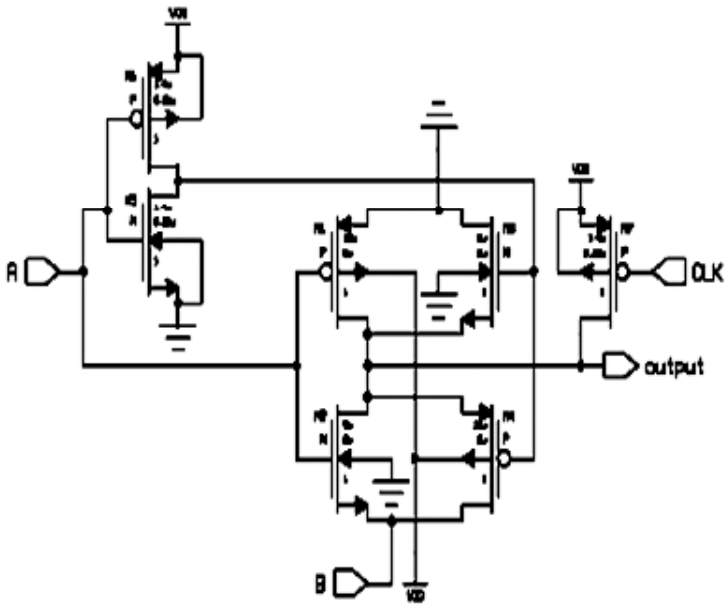

Figure 11: DMTGDI AND Gate [18]

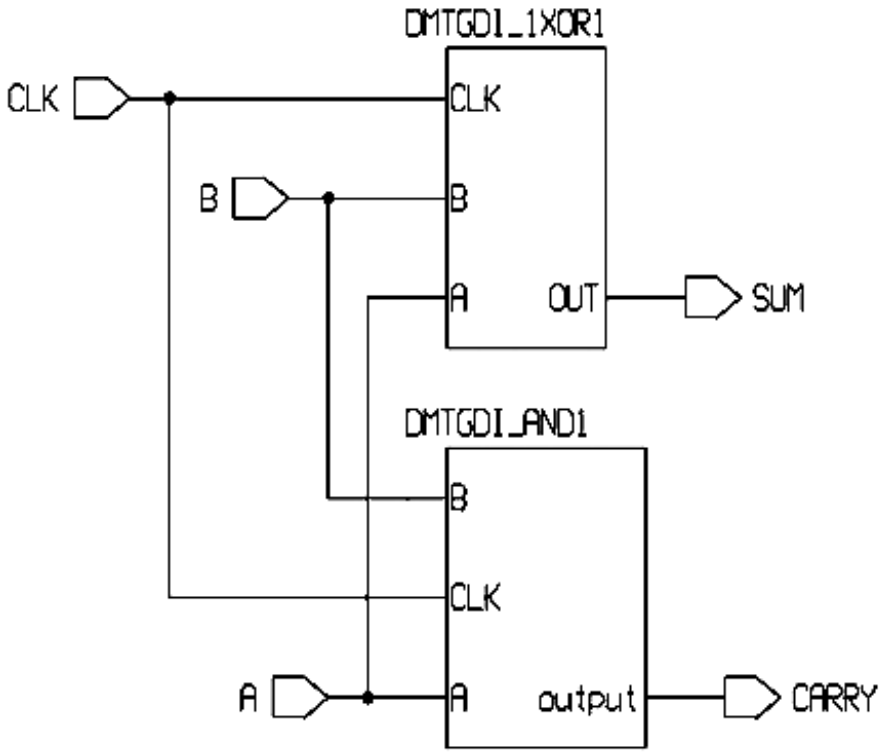

Figure 12: DMTGDI Half Adder Circuit

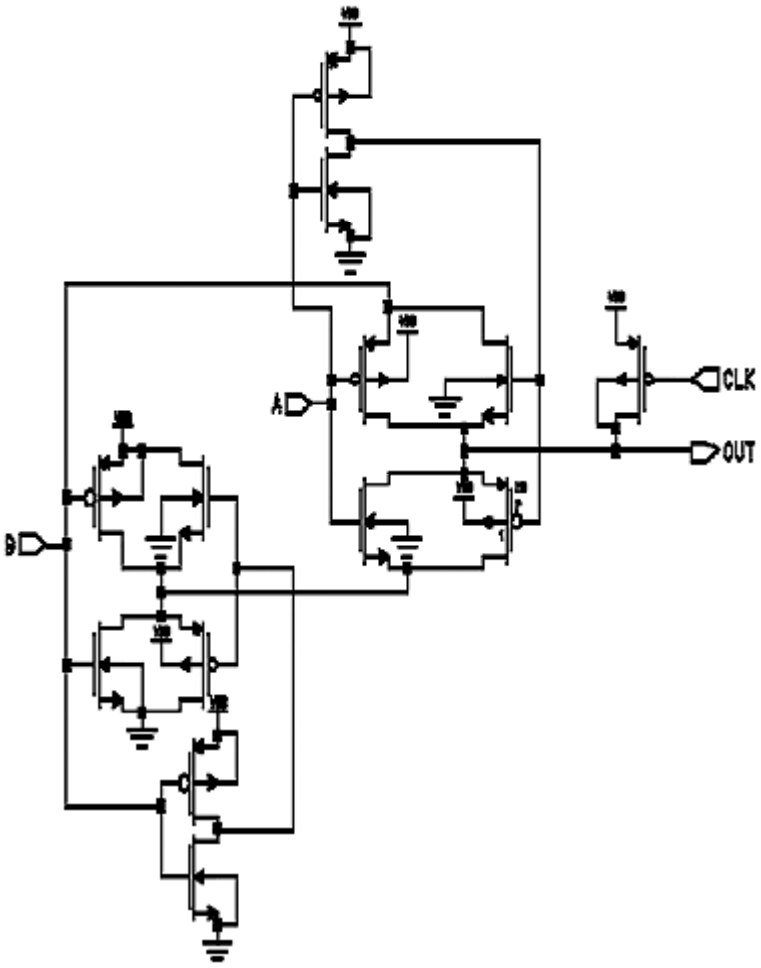

Figure 13: DMTGDI XOR Gate

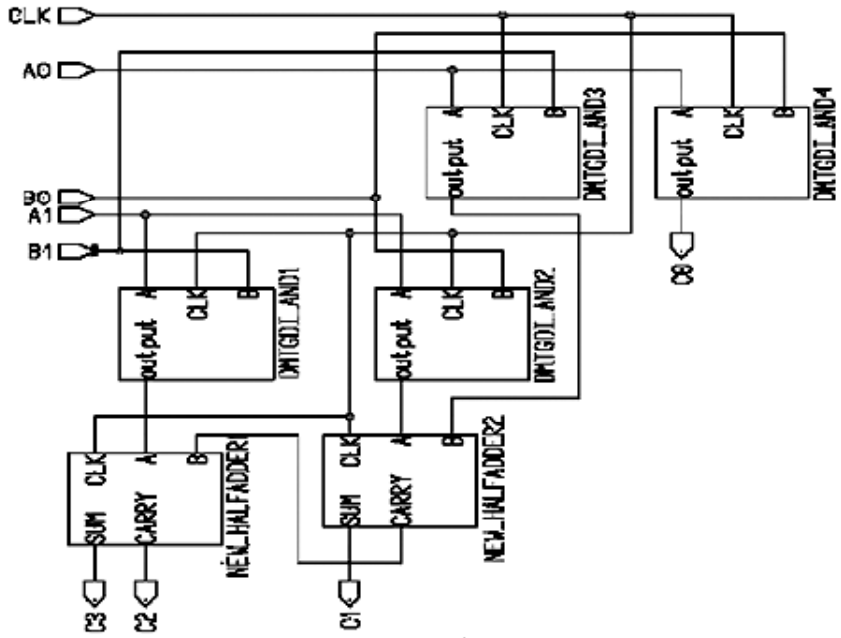

Figure 14: Block Diagram of 2-Bit Binary Multiplier using DMTGDI Logic

Fig. 13 shows an XOR gate using DMTGDI logic which has an extra transistor at the output node and a CLK input is given to this transistor. As. The VDD is replaced by an input terminal; the dynamic power of the circuit reduces to a large extent. The schematic of a two-bit binary multiplier using DMTGDI logic is shown in Fig. 14.

5. SIMULATION AND RESULT

A two bit binary multiplier is demonstrated and is implemented in conventional CMOS logic and DMTGDI logic. These circuits are used for simulation and comparison of performance, power consumption and delay in these logic families. Schematic of implemented 2-bit binary multiplier in CMOS logic is shown in Fig. 7. According to [7], by connecting cascaded gates alternatively, we can enhance the optimal design in DML and this methodology can also be enforced on DMTGDI logic. Table 1 shows the comparison between CMOS multiplier and DMTGDI multiplier on the grounds of power, delay, power delay product and number of transistors that has been used to construct the circuit. The implementations are compared at VDD¼ 300 mV. As expected, DMTGDI logic shows far better performance when compared to standard CMOS logic.

Table 1
Comparison of parameters of DMTGDI with CMOS

Parameters	*CMOS multiplier*	*DMTGD Imultiplier*
Delay	2.1nS	0.2pS
Average Power	6.4nW	0.624pW
Power Delay Product (PDP)	13.44	0.1248
Transistor Count	60	36

From Table 1, it is clear that DMTGDI logic has the lower PDP in all and this performance characteristic is inherited from both GDI and TGDI. It should be noticed that DMTGDI follows the same trend of DML, which infers if we reduce the size of the transistor in parallel path of the clock, power consumption gets reduced whereas the performance of DMTGDI is slightly degraded. DMTGDI consumes less power compared to CMOS under similar performance characteristics. Also DMTGDI logic has less effective area when compared to CMOS, because most of transistors in DMTGDI logic are minimum size devices. Design

consists of two main elements: four AND, and two half adder circuits. One half adder circuit is made of and an AND gate and an XOR gate. All cells are being designed as standard cells with same heights and regulated routing junctions. Fig. 14 shows time evolutions of multiplier input and relevant inputs signal. Fig. 14 shows the partial product outputs of 2-bit multiplier using DMTGDI logic.

6. CONCLUSION

In this paper, a two-bit binary multiplier has been designed using a new logic family called DMTGDI and the results have been compared with the conventional CMOS logic. This logic has been introduced basing on two consecutive steps. In the first step, we replace the pass transistor in the GDI logic by transmission gates so as to form TGDI and then we modify DML logic based on TGDI unit cell. Simulation results depicts that this logic family has remarkable performance and reduced energy consumption both in sub-threshold as well as above sub-threshold regions when compared to conventional DML and GDI logics, while inherits ûexibility of DML and low energy consumption of GDI.

Performance of implemented 2-bit multiplier in DMTGDI logic might be improved by methods of [14]. Also total power consumption can be shrinked by setting gates on the critical path in dynamic mode and setting the rest of the circuit in static mode [15]. To further improve the performance - power characteristics of this logic family, new techniques similar to dynamic voltage scaling [16,17] might be developed for dynamic selection of operating mode based on operating conditions.

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