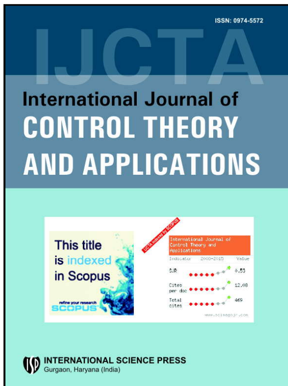

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Analysis of Subthreshold Drain Current for Pocket Implanted MOSFETs

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Abstract: MOSFET with overwhelmingly doped regions toward one side or both completions of the immediate show subjective differences in electrical direct appeared differently in relation to devices with on a level plane uniform channel. In this paper, we have investigated diverse paper on the subthreshold exhaust model of the Pocket installed MOSFETs. All the paper inspected has various model showed in them and these models have particular approach associated with evaluate the current.

Keywords: MOSFET modeling, halo implant, channel width, threshold voltage.

1. INTRODUCTION

Take embed is extensively used as a piece of significant sub-micron CMOS advances to diminish V_T get off and punch-through. This methodology, in any case, conveys colossal channel prompted V_T move and low R_{out} in long channel devices, essentially affecting straightforward circuit blueprint and execution. Physical negligible model for these effects, regardless, is not available.

As we reduce the channel length of the device to profound sub-100 nm regime, we observe the phenomenon of charge sharing [8] between the source or drain region and the channel. It leads to the reduction of threshold potential as the channel length gets reduced. Additionally, the source/drain channel barrier is sensitive to the drain voltage variation which leads to the increment of the off state leakage current. This impact is called the short-channel impact (SCE). Two-dimensional potential dissemination and the presence of high magnitude electric fields in the channel area lead to this impact. Locally increase the channel doping close to source and drain intersections can diminish and ultimately reverse the impact. The reverse impact was initially seen in devices because of oxidation upgraded dispersion or insert harm improved dissemination which are exceptionally hard to control.

Parallel channel outlining utilizing pocket embed incorporating channel and source territories is practical in covering short channel impacts[9]. The embedded pockets can be either uniform or non-uniform with respect

to source or drain region. With these improvement, the circuit having applications as a 256 M-bit DRAM and processors for mixed signal. Fortunately, this pocket embed development very effectively reduces the short-channel displays of sub-100 nm devices. Although, such reductions lead to cautious trade-offs between the shrink channel length and electrical parameters of the device. Authoritatively some papers have been disseminated related to the subthreshold lead of pocket inserted MOSFET.

Subthreshold drain current is defined as the current which flows when the gate potential is lower than the threshold voltage level and the Si-channel is operating in frail inversion region[4]. Study of the subthreshold region becomes significant in the area of low-voltage, low-power implementations. When the MOSFETs are used in digital memory and logic design, they are operated as switches and the turn on and off depend on subthreshold region. Different scientific subthreshold current model for pocket-embedded n-MOSFETs has been exhibited.

2. POCKET IMPLANTED N-MOSFET STRUCTURE

The structure of a n-MOSFET having the pocket implant for subthreshold drain current analysis is demonstrated in figure 1[14]. A pocket is defined as the area which has heavily doped p+ type Si region situated close to source and drain areas, whereas the center region of the device is softly doped p-type Si. N_P is the doping density of the pocket area and N_C denotes the doping concentration of middle locales. The distance of the pocket and the center sections are represented by L_P and L_C. t_{ox} is the oxide thickness and r_j is the intersection profundity.[1]

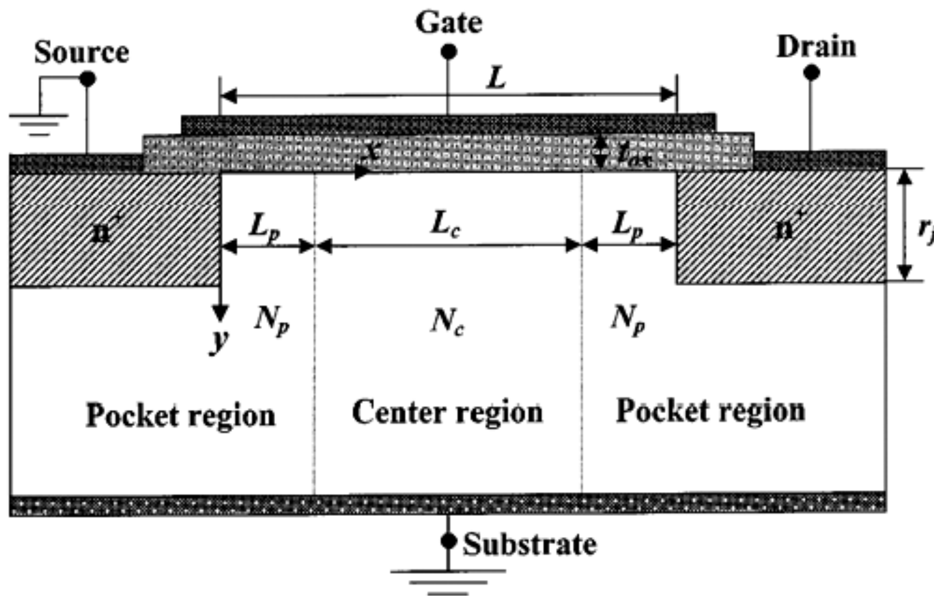

Figure 1: Pocket implanted n-MOSFET structure.

The n+–type polycrystalline silicon is used to make the contacts of the gate, source and drain whereas the substrate contact is made of p+-sort polycrystalline silicon. Any oxide charges, including the settled interface charge at the Si–SiO_2 interface, are thought to be zero. Bearer era and recombination rates are insignificant. Electrical conduction because of the minority transporters, i.e., gaps in the channel locale is overlooked.

3. BASIC THEORY

As we already know that when the N-MOSFET is in the sub threshold region and hence the Si channel surface is in weak inversion, the electrons need to cross a potential obstacle in the channel regime [2]. However, the conventionally

derived results for the I_D in the uniformly doped MOSFET devices do not apply here. It had been communicated that the surface-potential assortment in the station of pocket-inserted devices is important, which fairly elucidates the physics behind the subthreshold current. The study of subthreshold drain current using the pocket implant has been done on various structures which are different from each other either on the implant structure or the analysis method.

4. MODELS FOR THE SUBTHRESHOLD CURRENT

In the subthreshold model, it is expected that the pinnacle stash doping concentration (N_{pm}) bit by bit diminishes linearly towards the substrate level fixation (N_{sub}) with a pocket length (L_p) from both the source and deplete edges. The premise of the model of the pockets is to expect two lateral linearly doped profile from both the source and deplete edges over the channel as demonstrated in figure 2. The parameters of the pocket, N_{pm} and L_p, play critical part in deciding the RSCE.[1]

The pocket profile at the source end is given as,

$$N_s(x) = -\frac{N_{pm} - N_{sub}}{L_p} x + N_{pm}$$

$$N_s(x) = N_{sub}\frac{x}{L_p} + N_{pm}\left(1 - \frac{1}{L_p}x\right) \tag{1}$$

The pocket profile at the drain side is given as,

$$N_d(x) = \frac{N_{pm} - N_{sub}}{L_p}\left[x - \left(L - L_p\right)\right] + N_{sub}$$

$$N_d(x) = N_{sub}\left(\frac{L}{L_p} - \frac{1}{L_p}\right) + N_{pm}\left(1 - \frac{L}{L_p} + \frac{1}{L_p}x\right) \tag{2}$$

where *x* represents the distance across the channel.

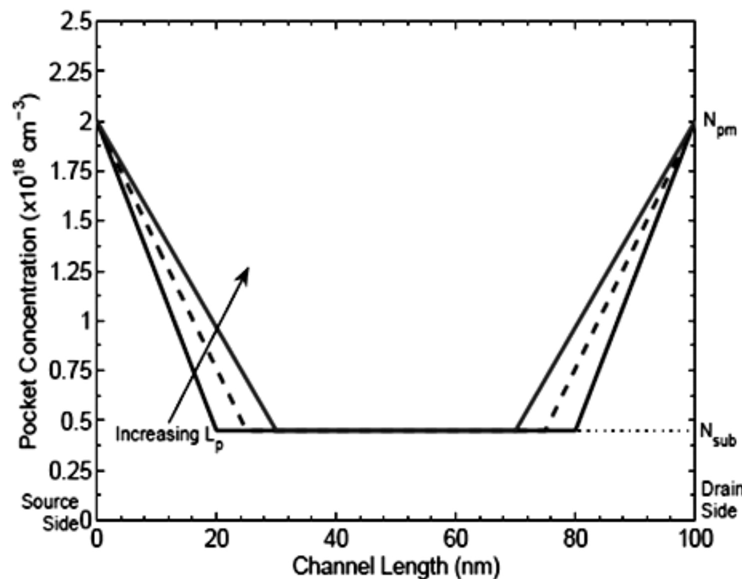

Figure 2: Simulated pocket profiles at the surface for different pocket lengths, L_p = 20, 25 and 30 nm; peak pocket concentration, N_{pm} = 2.0×1018 cm”3.

This model used the drift- diffusion equation to obtain the subthreshold drain current.

According to this model, in an n-MOSFET, the electron current density, J_n can be stated as in the equation (3),

$$Jn = q\left(-n\mu n,\ eff\frac{d\psi s}{dx} + Dn\frac{dn}{dx}\right)$$

$$= qDn\left(-\frac{n}{\phi th}\frac{d\psi s}{dx} + \frac{dn}{dx}\right) \tag{3}$$

In the model exhibited, the examination approach is diverse when contrasted with others. Consider a MOSFET sectioned into three districts, as appeared in figure 3. Nearby the source is a locale of length L_L and limit voltage V_{TL}, in the centre is an area of length L_C and edge voltage V_{TC}, and adjoining the deplete is a district of length L_R and edge voltage $V_{TR,}$ the source and mass are thought to be at zero volts and voltages V_G and V_D are connected to the door and deplete.[11]

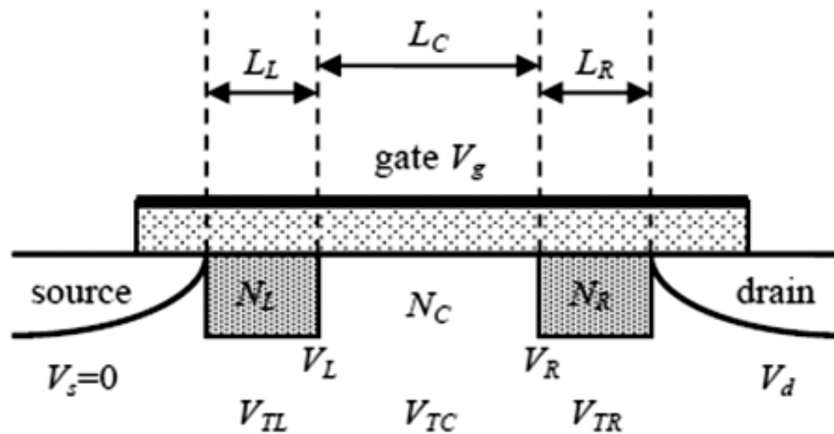

Figure 3: Three separately doped regions in the MOSFET

For operation in strong inversion non- saturation, at small V_d, the currents in each of the 3 sections, which must be equal, are approximately,

$$i_L = \frac{V_g - V_{TL} - 0.5V_L}{L_L}V_L$$

$$i_C = \frac{V_g - V_L - (V_{TC} + B_C V_L) - 0.5(V_R - V_L)}{L_C}(V_R - V_L)$$

$$i_R = \frac{V_g - V_R - (V_{TR} + B_R V_R) - 0.5(V_d - V_R)}{L_R}(V_d - V_R) \tag{4}$$

where V_L and V_R are the voltages between the left (source) and focus districts, and between the middle and the right (deplete) segments individually, and B_C and B_R are the body impact variables for the focal and right area, separately. After the examination, for the long gadget, we have,

$$\frac{g_m}{v_d} \to \frac{1}{L_C + 2L_H} \tag{5}$$

and for a short device,

$$\frac{V_L}{V_d} \rightarrow 0.5, \frac{V_R}{V_d} \rightarrow 0.5, \frac{g_m}{V_d} \rightarrow \frac{1}{2L_H + L_C \dfrac{V_g - V_{TH}}{V_g - V_{TC}}} \tag{6}$$

From this model, the unilateral halo model is also derived. The expression is given as follows,

$$\frac{g_m}{V_d} = \frac{V_g - V_{TL} + (V_L / V_d)(V_{TL} / V_{TC})}{L_L (V_g - V_{TC}) + L_C (V_g - V_{TL})} \tag{7}$$

In the following structure, the model is unique in relation to the above models since it considers step variety in the pocket implant doping profile [5]. The MOS structure and the doping profile are appeared in Fig 4.

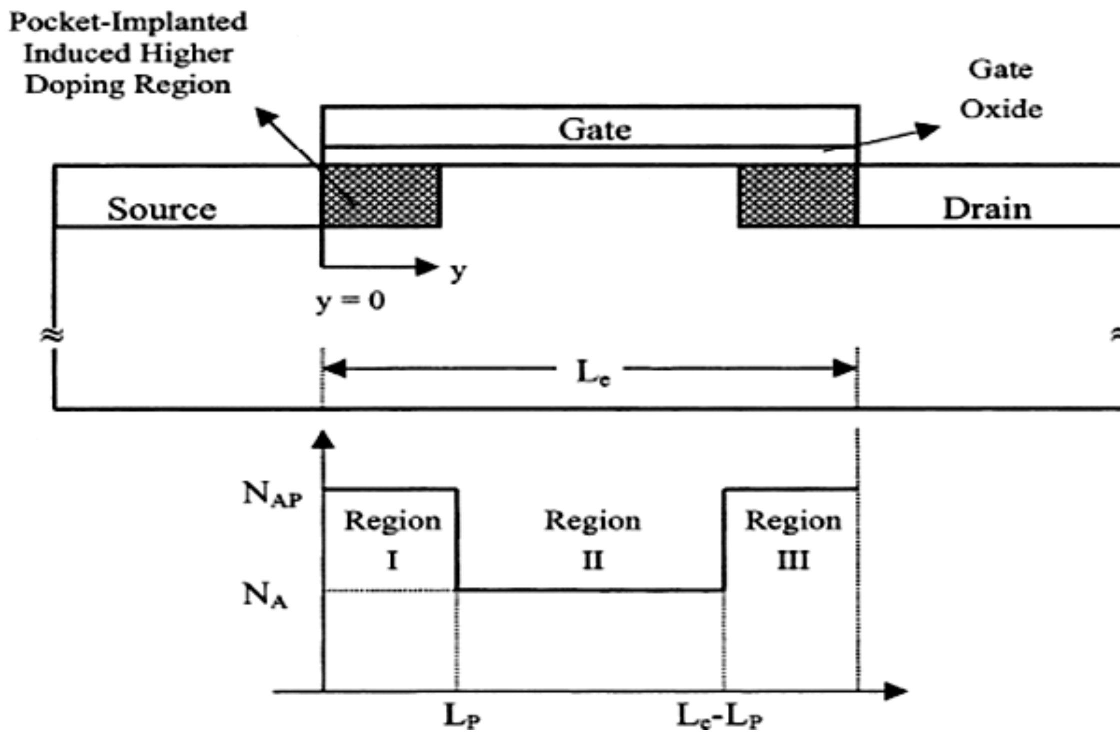

Figure 4: MOSFET structure with pocket implant and doping profile in the channel.

The drain current in the channel is obtained by integrating the current density over the cross section of the conducting channel, yielding

$$I_{DS} = J_N . \text{W. S}_{\text{eff}} \tag{8}$$

where W is the gadget channel, S_{eff} is the compelling channel thickness. Keeping in mind the end goal to figure the subthreshold deplete current, channel potential and compelling doping thickness should be known first. Taking after a pseudo-2-D technique and applying the Gauss' law to a rectangular box in the channel consumption district, the accompanying condition can be acquired:

$$\varepsilon_s, \frac{X_D}{\eta}, \frac{dE(y)}{dy} + \varepsilon_{ox} \frac{(V_{GS} - V_{BS} - V_{FB} - V_S(y))}{T_{Ox}} = q.N_{CH}(y).X_D \tag{9}$$

This equation can be used to evaluate using the boundary conditions.

In the model shown, we have considered the same doping profile yet the investigation is done utilizing the electric fields over the channel [6]. The model appeared in figure 5 and 6 was proposed in view of the surface-potential variety. In this model, the subthreshold current relies on upon the doping centralization of the pocket embeds just, yet it incorporates the essential of the type of the surface potential along the cannel locale.

For the induction of the subthreshold current model, we have the accompanying suppositions.

1) Boltzmann's guess is relevant.
2) There is no present course through the entryway dielectric and no recombination in the channel area, which yields a consistent channel current.

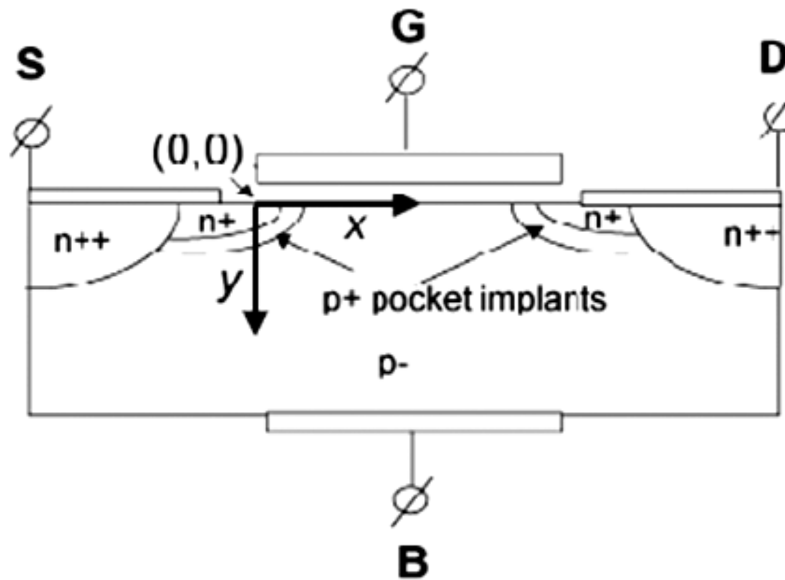

Figure 5: n-MOSFET cross section with p+ pocket implanted channel region.

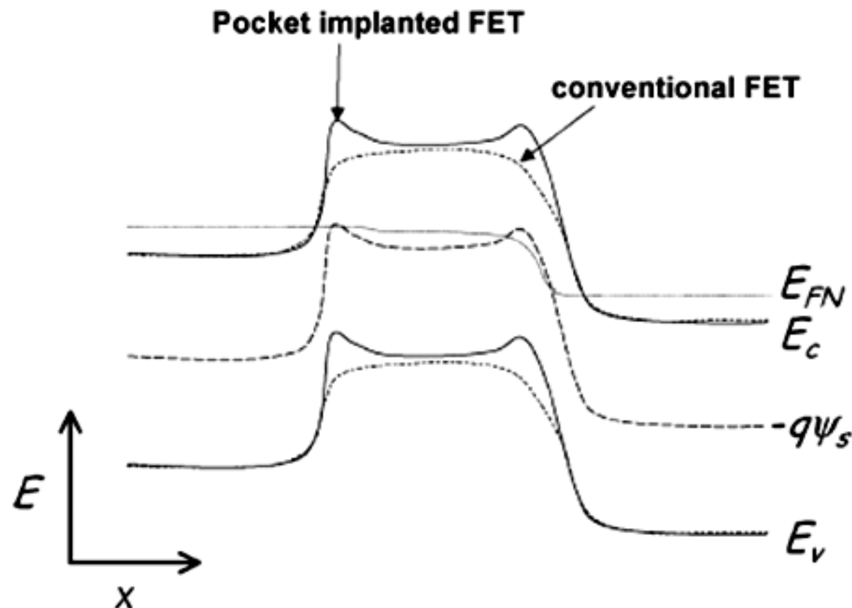

Figure 6: Channel region schematic diagram (bottom).

3) The gap Fermi potential y_{FP} is consistent in the channel area.

4) There is no interface charge.

5) There is no quantum restriction.

Using no vertical current flow, electron current density is given by,

$$J_n(x,y) = -q.n(x,y)\mu_n(x,y)\frac{d\varphi_{FN}(x)}{dx} \tag{10}$$

Current is given by,

$$I(x) = \int_0^{tsi} J_n(x,y)\,dy$$

$$= -q\frac{d_{\varphi FN}(x)}{dx}\int_0^{t_{si}} n(x,y)\mu_n(x,y)\,dy \tag{11}$$

Various analyses are done on the basis of these models and variation or the dependence of one variable on the other is simulated using the tools.

5. RESULTS

To affirm the analytical model for the subthreshold current for the n-MOSFET with pocket insertions, various sorts of simulations were done. Initially, model for the surface potential is simulated for varying pocket profile parameters. It is watched that the surface potential augmentations with the decreasing apex stash doping centers and take lengths separately. Since when the apex stash doping center or pocket length lessens the intense doping obsession in like manner reduces. In this way channel current is impacted.

It has been watched that as the pocket estimation or the pocket length is extended, the RSCE increases and in this way puts off the edge voltage get off [3]. Since the flexibility is affected by the point of confinement voltage, in this way, assortment of pocket estimations or pocket length will achieve the assortment of the intense convey ability. On increasing the pocket concentration and length of pocket implant, effective mobility gets spoiled even at low magnitude electric fields as the coulomb scattering rate gets increases as the ion concentration increases in the channel by the pocket dopants. This holds the all-inclusiveness of the powerful versatility bends. It is watched that, subthreshold drain current does not change obviously for longer channel length gadget as the deplete predisposition increments, but subthreshold current changes considerably shorter channel length gadget as the deplete inclination increments. This happens because of the impact caused by the DIBL. On increasing the bias of the substrate in the negative direction keeping the gate and the drain potential at the same level, we note the decrement of the subthreshold drain current. It is consistent with the literature result obtained. However, slope of the subthreshold current declines more rapidly with the increase of the gate potential is less in the short channel length devices. In an another simulation, we observe that there is increase in the subthreshold drain current for the same applied potential on the gate and drain as the oxide thickness is increased. Due to the increase of the pocket implant concentration, the subthreshold drain current decreases. It leads us to the conclusion that the reduction of the current in the off-state improves the subthreshold behavior.

6. CONCLUSION

This paper gives a survey on the expository subthreshold deplete current model for the ultra-thin oxide and nano scale take embedded n-MOSFET in view of routine float dissemination condition and utilizing the surface

potential, edge voltage and in addition reversal layer compelling versatility models of the pocket embedded n-MOSFET from prior works [15]. The impact of changing the gadget and pocket profiles parameters and in addition inclination possibilities on subthreshold deplete current have been contemplated utilizing the created demonstrate.

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