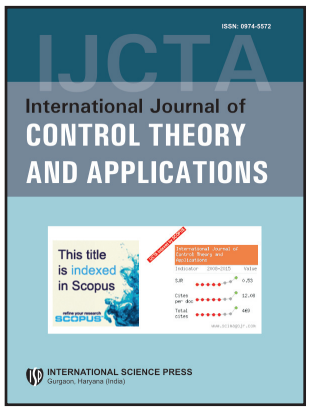


International Journal of Control Theory and Applications

ISSN : 0974-5572

© International Science Press

Volume 10 • Number 16 • 2017

A Real Time Application of IDVR for Improvement of Power Quality

Ramchandra Nittala[a], Alivelu M. Parimi[b] and K. Uma Rao[c]

[a]*EEE Department, BITS Pilani Hyderabad Campus, Hyderabad. Telangana, India. Email: nittala1988@gmail.com*
[b]*EEE Department, BITS Pilani Hyderabad Campus, Hyderabad. Telangana, India*
[c]*EEE Department, RV College of Engineering, Bangalore, Karnataka, India*

Abstract: Voltage fluctuations which occur frequently in the form of voltage sag/swell cause severe disturbances and damage the sensitive loads present on the distribution side of power system. One of the feasible solutions to mitigate these voltage sags/swells is Interline Dynamic Voltage Restorer (IDVR) which contains two or more Dynamic Voltage Restorers (DVR) sharing a common DC link. The IDVR has a major advantage in its simultaneous mitigation of voltage sag/ swells in multiple feeders at the same instance which is referred to as bidirectional compensation. In this paper, IDVR is designed for a specific application to mitigate power quality problems in an existing real time load. The load network data of BITS Pilani Hyderabad Campus located in Telangana, India which is spread over 200 acres is considered as the real time load. A multiple voltage sag/swell scenario is analysed in the real time load. The results have proven that the IDVR can effectively mitigate multiple voltage sags/swells in the considered real time load.

Keywords: Interline Dynamic Voltage Restorer; Power Quality; Voltage Sag/swell.

1. INTRODUCTION

Power Quality problems are the most significant problems on the distribution side of power systems. One of the major and frequently occurring power quality problems is voltage sag/swell. Voltage sag is referred to as the drop in voltage magnitude from 0.1 to 0.9 per unit of the nominal value, for a duration of half cycle to one minute. Similarly a voltage swell is referred to an increase in the voltage magnitude from 1.1 to 1.8 per unit of the nominal value for a duration of half cycle to one minute[1]. In the recent years sensitive loads have become more in number at the distribution side of the power system. These sensitive loads have low resistance towards the voltage sag/swell and get easily damaged when there is a voltage deviation. There are some devices like shunt capacitor banks, phase advancers, synchronous condensers etc. which are used to eliminate the voltage sag/swell. But there are certain limitations to these devices like less life span, restricted range of operation. Therefore these traditional devices are slowly getting replaced with Flexible AC Transmission Systems (FACTS) devices[2,3,4].

The FACTS device utilized on the distribution side for mitigation of voltage sag/swell is Dynamic Voltage Restorer (DVR)[5]. When there is a voltage sag or voltage dip in a system, the DVR mitigates the voltage sag by adding the necessary voltage to the system. The major limitation of DVR is, it needs huge amount of DC link

energy to mitigate deeper voltage sags and also the elimination of voltage sag/swell with DVR is restricted to only one feeder[6].

The limitation of DVR can be overcome with an extended version of DVR known as Interline Dynamic Voltage Restorer (IDVR). IDVR comprises two or more DVRs connected to a common DC link[7]. The ability of IDVR is, it can simultaneously eliminate voltage sag/swells in different feeders at same instance of time with one common DC link and also when one of the DVR is mitigating deeper voltage sag, the required power can be supplied by another DVR. This will reduce the size of DC link, which will also be beneficial economically.

In this paper, the functionality of IDVR is studied with real time data. The power network and the existing load in BITS is studied and considered for the real time load. The various changes in the load at different timings during day and its effect on voltage change has been recorded. Thus the occurrence of voltage sag/swell on the various possible load conditions in the real time is studied. In order to compensate this voltage sag/swell, suitable ratings for IDVR are designed for this network. Finally the performance of IDVR in eliminating the multiple voltage sags/swells at the same instance of time (bidirectional compensation) has been enumerated. The total network of BITS Pilani Hyderabad Campus has been simulated in MATLAB Simulink software.

2. INTERLINE DYNAMIC VOLTAGE RESTORER

A typical network incorporated with the IDVR shown in Figure 1. It consists of two DVRs having a common DC link. The two DVRs of IDVR are connected to two different feeders with the aid of series injection transformers. The IDVR consists of a PI controller which is the control system of the IDVR, a voltage source inverter and the filter. The network shown in Figure 1 contains two feeders. V_{b1} and V_{b2} are the bus voltages of feeder 1 and feeder 2 respectively. The two loads, Load 1 and Load 2 are considered as the sensitive loads connected to feeder 1 and feeder 2 respectively. V_{l1} and V_{l2} are the load voltages of load 1 and load 2. These voltages are initially at the nominal bus voltages, V_{b1} and V_{b2}. When a sag occurs at say load 1, then the DVR 1 injects the voltages V_{inj1} to maintain the V_{l1} equal to V_{b1}. Hence, in a voltage sag condition the bus voltages V_{b1} and V_{b2} can be represented as

$$V_{b1} = V_{inj1} + V_{L1} \tag{1}$$

$$V_{b2} = V_{inj2} + V_{L2} \tag{2}$$

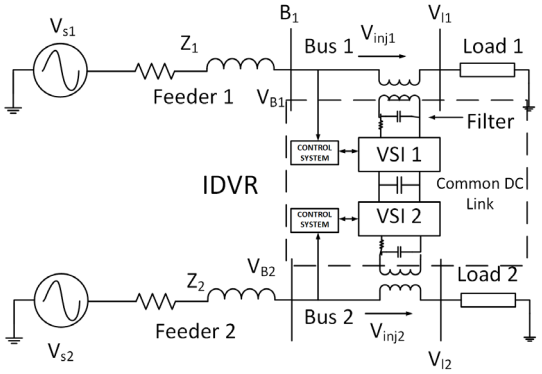


Figure 1: Schematic layout of two line IDVR

2.1. Design of Interline Dynamic Voltage Restorer

The design part of IDVR consists of two parts; rating of DVR and rating of DC link which are explained below:

2.1.1. Rating of the Inverter

The rating of inverter of IDVR depends on the control strategy for the voltage sag/swell compensation. In this paper, in phase compensation[8] is considered. In this method of compensation, the injected voltage of DVR is in phase with load (sagged) voltage. Figure 2 represents the phasor diagram of in phase compensation. The injected voltage V_{inj} is in phase with load voltage. As shown in Figure 2 the load current I_L is having a phase difference with injected voltage, hence the DVR should inject active power along with reactive power to the load nearly at all times

Hence, the steady state injected active power of the inverter of IDVR is given by:

$$P_{DVR} = \sqrt{3} \times (V_L - V_{inj}) \times I_L \times \cos\phi \tag{3}$$

where, V_L, V_{inj} are the load voltage line to line and injected voltage line to line of DVR, I_L is the load current line to line and is the load power factor.

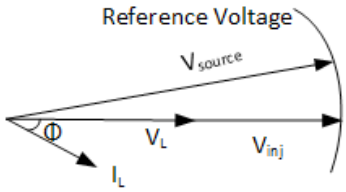


Figure 2: Phasor diagram of in phase compensation

2.1.2. Design of DC link of IDVR

One of the key factors of IDVR is the DC link. The required power for the voltage sag compensation by the DVR is given by the DC link[9]. For a voltage source inverter a capacitor is considered as the DC link. For a capacitor as a DC link, the size of capacitor and the voltage to which capacitor should be charged is to be determined. The DC link voltage of the capacitor is given by the equation:

$$V_{dc} = (V_{Pre\text{-}Sag} - V_{sag}) \times \sqrt{2} \tag{4}$$

where,

$V_{pre\ sag}$: Peak Voltage before the occurrence of sag

V_{sag}: Peak Voltage during occurrence of sag

The size of the capacitor can be determined from the following equation

$$\frac{1}{2} C_{dc} (V_{dc}^2 - V_{dc1}^2)^2 = \sqrt{3} \times V_L \times I_L \times \cos\phi \times \Delta t \tag{5}$$

where, V_{dc}: Dc link voltage

V_{dc1}: Permissible DC link voltage (The maximum limit below which the DC link voltage should not decrease)

V_L: Load Voltage line to line

I_L: Load Current line to line

cos φ : Power Factor of Load

Δt: Discharge time of capacitor

From the (4) and (5), the complete rating of DC link of IDVR can be determined.

The next section explains the control system of IDVR.

3. CONTROL SYSTEM OF IDVR

The functionality of IDVR is to compensate voltage sag/swell in a system. Whenever there is a voltage sag/swell, the IDVR detects the deviation in the voltage and injects the necessary voltage into the system thereby maintaining the system voltage constant at all conditions. The control system of IDVR plays an important role in controlling the injected voltage from IDVR. The schematic layout of the control system of IDVR is given Figure 3.

According to the schematic layout represented in Figure 3, the reference voltage $V_{ref(abc)}$ is converted to $V_{ref(dq)}$ axis using parks transformation given by:

$$\begin{bmatrix} V_{refd} \\ V_{refq} \\ V_{refO} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\Pi}{3}\right) & \cos\left(\theta + \frac{2\Pi}{3}\right) \\ -\sin\theta & -\sin\left(\theta - \frac{2\Pi}{3}\right) & -\sin\left(\theta + \frac{2\Pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} V_{refa} \\ V_{refb} \\ V_{refc} \end{bmatrix} \tag{6}$$

Similarly $V_{L(abc)}$ is also converted to $V_{L(dq)}$. The error between the reference voltage and load or actual voltage is given is given as input to the PI controller. The PI controller regulates the error and the output of the PI controller is given by equations (7) and (8).

$$V_{errd} = \left(K_p + \frac{K_i}{S}\right)(V_{refd} - V_{Ld}) \tag{7}$$

$$V_{errq} = (V_{refq} - V_{Lq})\left(K_p + \frac{K_i}{S}\right) \tag{8}$$

where,

K_p and K_i are proportional integral gains of PI controller.

The $V_{err(dq)}$ is converted to $V_{err(abc)}$ by the *dqo* to *abc* transformation and $V_{err(abc)}$ is fed as input to the PWM generator. The PWM generator generates the required gate pulses to the inverter for the injection of voltage into the considered system. The values of K_p and K_i are determined by zigler-Nicholas method[10].

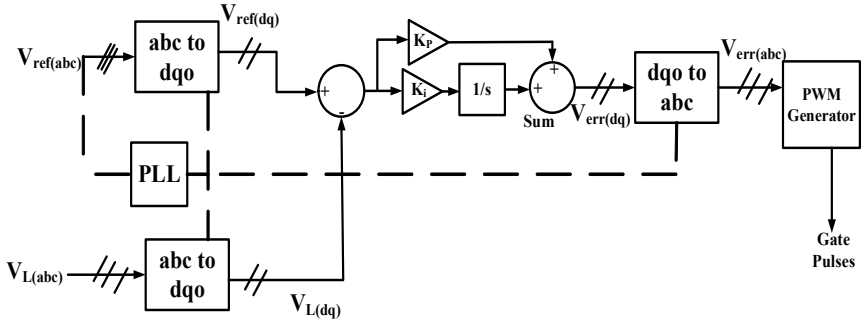


Figure 3: Schematic layout of the control system of IDVR

4. SIMULATION RESULTS AND DISCUSSION

The real time load of BITS Pilani Hyderabad Campus, located in Hyderabad, Ranga reddy district spread over 200 acres, is considered and simulated in MATLAB Simulink software. The power to the campus is given by the feeder from the 33/11kV MALKARAM substation. At the input side of the campus a 5MVA, 33kV/11kV step down three phase transformer is present, which steps down the voltage to 11kV. This 11kV voltage is given to three different substations present inside the campus.

Substation 1: The major load of the campus in on substation 1. The input voltage to substation 1 is 11kV which is stepped down to 415V by 2MVA, 11kV/415V three phase step down transformer within the substation. The load consists of totally 9 different blocks from 'A' block to 'G' block and two workshop units. These blocks consist of administration wing, class rooms and the various departments of the institute. A 10hp induction motor is connected along with the blocks to substation 1. This induction motor is used to pump water to various places of BITS campus. This induction is not a continuous load and is ON only when the pumping of water is required. The ratings of all the loads connected to substation 1 is given in Table 1. The maximum demand on substation 1 is 1000kVA. The other

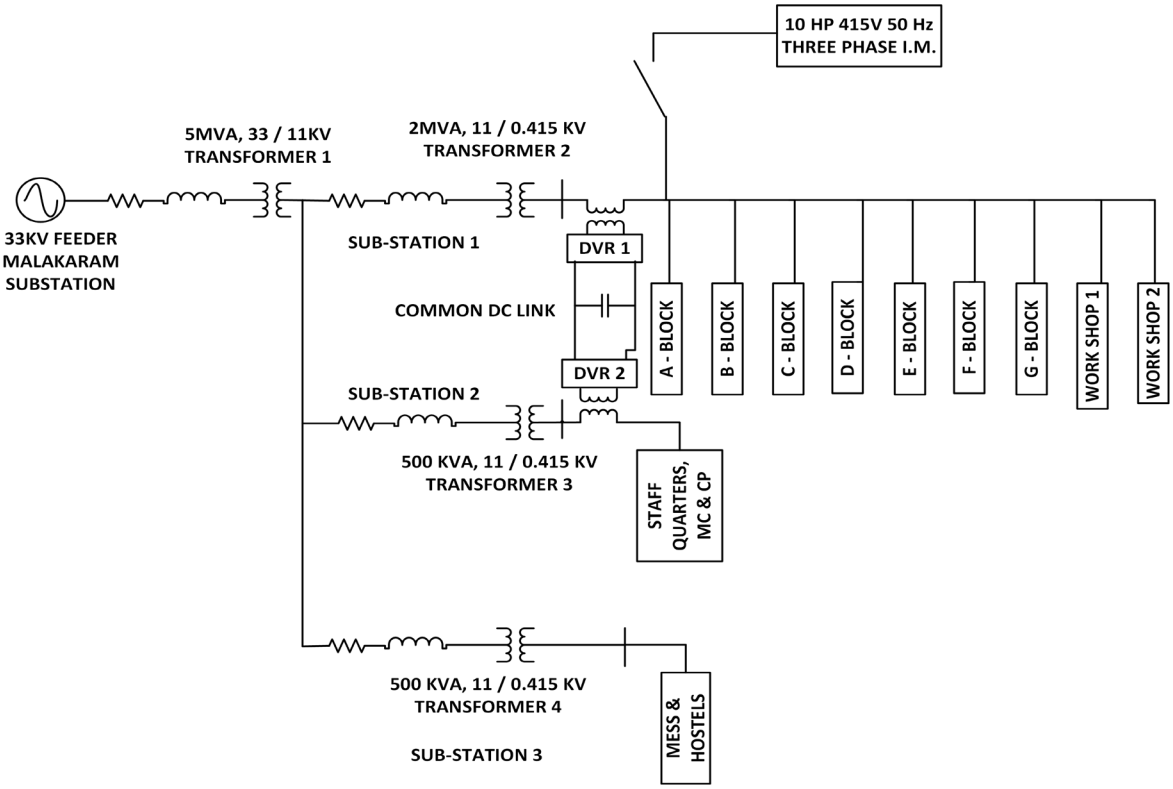


Figure 4: Schematic layout of the real time load with IDVR loads of BITS campus are connected to substation 2 and substation 3.

Substation 2: The 11kV voltage is given as input to the substation 2 which steps down to 415V using a 500 kVA, 11kV/415V three phase step down transformer. Staff Quarters, Medical center and CP, security office and remaining street lights are the various loads connected to substation 2. The maximum demand at substation 2 is 200kVA.

Substation 3: The 11kV voltage is given as input to the substation 3 which is stepped down to 415V by a 500KVA, 11kV/415V three phase step down transformer. The load at substation 3 consists of 6 boy's hostels, 2

girl's hostels and two dinning messes and some street lights. The load data substation 3 is given in table 1. The maximum demand at substation 3 is 300kVA.

The sensitive loads of the BITS campus are present in B-block connected to substation 1 and in medical centers connected to substation 2. These are loads which should be protected from voltage sag/swell. Hence, various possible conditions for the occurrence of voltage sag/swell at substation 1 and substation 2 is to be considered initially. The total system shown in Figure 4 is simulated using MATLAB/ SIMULINK software tool.

The possible chance for the occurrence of voltage sag/swell at Point of Common Coupling (PCC) of any substation is due to a fault occurring at one of its connected load. To observe a voltage sag/swell, a line to ground (LG) fault is simulated at one of the loads connected to substation 2. To test the ability of bidirectional compensation of IDVR, a voltage sag/swell is created in substation 1 and 2 as same instance of time which explained in the next section.

4.1. Substation 1 and Substation 2 Affected with Voltage Sag/Swell at Same Instance

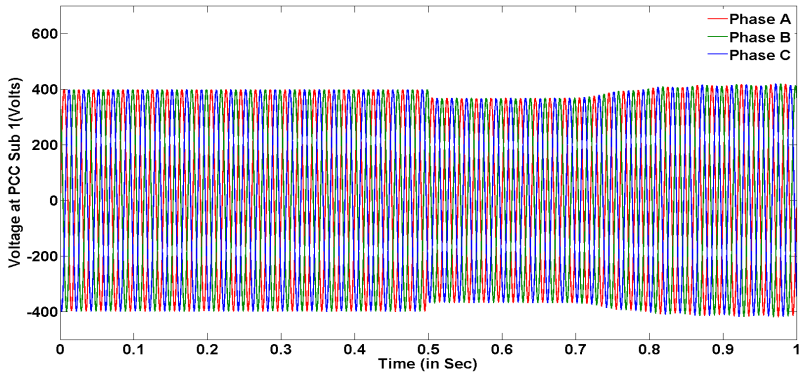
In this case, the induction motor connected at substation 1 is switched ON and fault at substation 2 occurs at the same time.

Figure 5 indicates that substation 1 and substation 2 are affected with voltage sag/swell at 0.5sec. In Figure 5(a), the voltage sag is observed at 0.5sec with switching ON of the induction motor and in Figure 5(b) voltage swell is observed at 0.5sec due to the occurrence of LG fault. The sensitive loads connected to both substations may get affected by voltage sag and voltage swell. To eliminate the voltage sag and voltage swell in both substations at the same instant, IDVR is connected to both substations as shown in Figure 4.

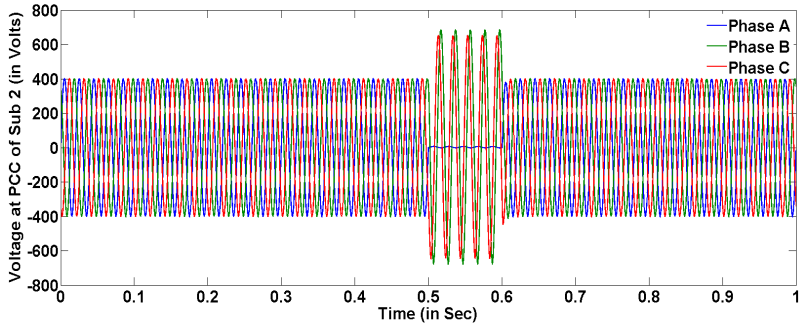
With the IDVR connected, the voltage at PCC of substation 1 and substation 2 is shown in Figure 6. It can be observed from Figure 6(a) and Figure 6(b), that the voltage sag/swell is completely eliminated by the two DVRs of the IDVR. The energy required to mitigate the voltage sag/swell in both feeders is given by the DC link of IDVR.

The DC link voltage during the time of compensation of voltage sag/swell by IDVR is shown in Figure 7. The DC link voltage is initially charged to 600V. The nominal voltage at the PCC, is itself 400 V, a slight drop from 415V, due to the existing loading conditions. We can see from Figures 6(a) and 6(b), that the voltages are maintained at 415V by IDVR. Therefore, in addition to mitigation of voltage sag/swell, IDVR also maintains the voltage at 415V under nominal loading conditions. Hence, the DC link voltage is continuously supplied to IDVR to sustain the voltages at PCC of substation 1 and substation 2 to the rated value. The DC link voltage is dropped from the initial 600V and maintained at 100V once the voltage settles at 415V. During the time (at 0.5sec) of occurrence of voltage sag/swell, the DC link voltage has slightly decreased at 0.5 sec, which can be observed in the zoomed portion shown in Figure 7. Since the decrease of the DC link voltage during the time of voltage compensation in both feeders at same instant is very small, it is observed that the effect of voltage sag/swell on the DC link voltage is considered to be negligible. Hence, DC link is charged sufficiently to supply the required energy to IDVR to maintain the rated voltage at all conditions in both substations.

Thus IDVR has effectively eliminated voltage sag/swell in both feeders at same time there by protecting the sensitive loads in both substations. Hence IDVR can be implemented in mitigating multiple voltage sags/swells simultaneously on the distribution side of power system. Finally it can be concluded that implementation of IDVR in the real time load will have a great impact in eliminating the voltage fluctuations and in protecting the sensitive loads.

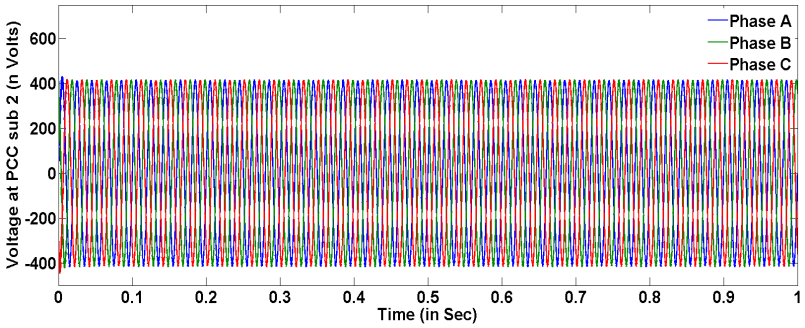


(a)

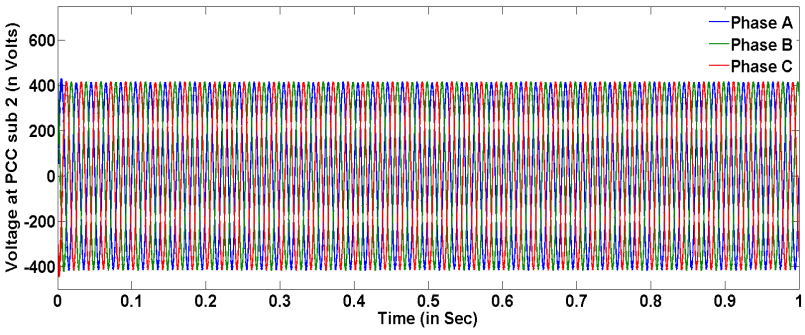


(b)

Figure 5: Simultaneous voltage sag/swell at (a) substation 1 with switching on induction motor and (b) substation 2 with LG fault



(a)



(b)

Figure 6: Simultaneous voltage sag/swell at (a) substation 1 with switching on induction motor and (b) substation 2 with LG fault with presence of IDVR

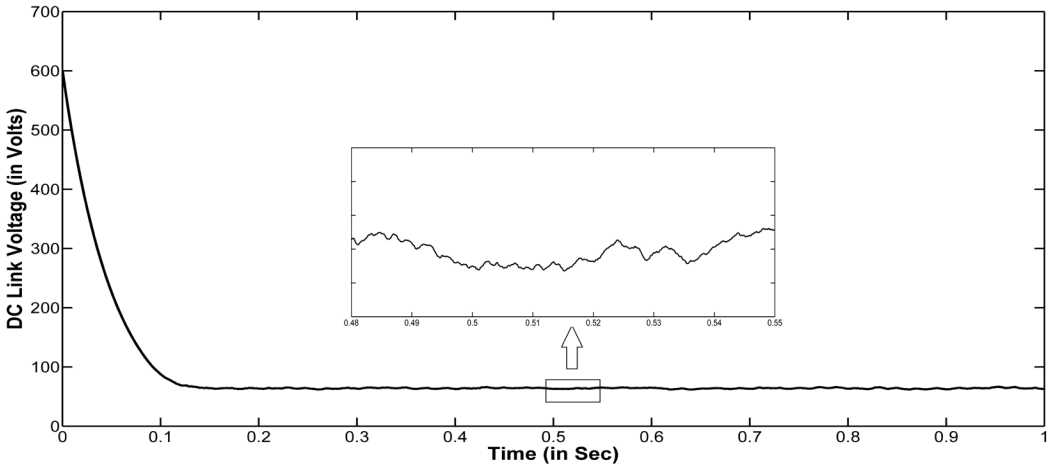


Figure 7: DC Link Voltage of IDVR

5. CONCLUSIONS

This paper deals with mitigation of voltage sag/swell with an IDVR. The electrical load of BITS Pilani Hyderabad Campus is considered as real time load, where the sensitive loads which get affected with the voltage sag/swell are identified. IDVR is connected to the PCC of those substations to which the sensitive loads are connected. Based on the intensity of voltage sag/swell that occurred at the substations, the appropriate ratings for the IDVR and DC link of IDVR are designed. The bidirectional compensation of voltage sag/swell in both substations with IDVR is observed. The IDVR effectively maintains the voltage at the substations at the rated value. Therefore the IDVR is helpful in solving the problems of voltage sag/swell in the considered real time load and with IDVR, multiple voltage sags/swells can be mitigated at same time, thereby protecting the sensitive loads from the voltage disturbances.

REFERENCES

[1] M. H. Bollen, Understanding Power Quality Problems: Voltage Sags and Interruptions. Wiley, 2000.

[2] R. Sedaghati, K. Isapour, M. B. Haddadi, and N. M. Afroozi, "Enhancement of power system dynamic performance using coordinated control of FACTS devices," Indian Journal of Science & Technology., Vol. 7, No. 10, pp. 1513–1524, 2014.

[3] R. Suguna, S. Jalaja, M. Pradeep, R. S. Kumar, S. SrikrishnaKumar, and K. R. Sugavanam, "Transient Stability Improvement using Shunt and Series Compensators," Indian Journal of. Science & Technology., Vol. 9, No. 11, pp. 1–11, 2016.

[4] P. B. C. and S. A. S. Muqthiar Ali*, "Enhanced Performance of a DVR using Mixed Cascaded Multilevel Inverter," Indian Journal of. Science & Technology, Vol. 8, No. January, pp. 171–178, 2015.

[5] V. R. K. Reddy and M. P. Lalitha, "Identification of instability and its enhancement through the optimal placement of facts using L-index method," Indian Journal of. Science & Technology, vol. 60, No. 3, pp. 616–622, 2014.

[6] R. Sudha, P. Usharani, and S. Rama Reddy, "Digital simulation of an interline dynamic voltage restorer for voltage compensation," 2011 Int. Conf. Comput. Commun. Electr. Technol. ICCCET 2011, No. March, pp. 388–393, 2011.

[7] M. Shahabadini and H. Iman-Eini, "Improving the Performance of Cascaded H-Bridge Based Interline Dynamic Voltage Restorer," IEEE Trans. Power Deliv., Vol. 8977, No. c, pp. 1–1, 2015.

[8] J. G. Nielsen, F. Blaabjerg, and N. Mohan, "Control strategies for dynamic voltage restorer compensating voltage sags with phase jump," in APEC 2001. Sixteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No. 01CH37181), 2001, Vol. 2, pp. 1267–1273.

[9] A. M. Rauf, V. Khadkikar, A. O. Al-mathnani, M. A. Hannan, M. Al-dabbagh, M. Alauddin, M. Ali, A. Mohamed, H. P. Tiwari, C. L. Bhattar, R. A. Metri, and S. K. I. Srikant, "Development of New Control Strategy for Voltage sag Mitigation," IEEE Trans. Power Delivery, Vol. 62, No. 3, pp. 318–323, 2013.

[10] S. K. Singh, Computer-Aided Process Control. PHI Learning Pvt. Ltd., 2004.