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Comparitvie Analysis and Proposed Schmitt Trigger Design using Different CMOS Foundries

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Abstract: This paper enumerates reduction of power consumption, which is in major demand in the field of VLSI. The CMOS device are used to achieve better power consumption, speed, hysteresis. Schmitt triggers are the regenerative comparators which are widely used in circuits This paper emphasize a low power, high speed construction of Schmitt trigger which contain less number of CMOS circuits. The circuit is modified on basis on various conventional Schmitt triggers. Its simulation result is compared with modified CMOS Schmitt trigger at 120nm and 90nm technology. The designed trigger and simulations are carried out by MICROWIND tools.

Keywords: CMOS DESIGN, LOW POWER, Schmitt Trigger, VLSI.

1. INTRODUCTION

In recent years, low power consumption has become highly important design concern in the era of VLSI design. The circuit designs are fulfilled on the basis of NMOS, PMOS and CMOS devices. There is trade-off between the power and the performance of a VLSI circuit [15] The digital circuits are not exactly relevant for digital signal, for some reasons it may have slow rise time or fall time and small noise, to overcome from these condition specific device is required which will "clean" or maintain a signal known as Schmitt trigger [3]. It was invented by the American scientist named Otto H. Schmitt in the year of 1934 while pursuing graduation [1].The Schmitt triggers are bistable multivibrator circuits. The term trigger is used because of its output, which remains in its state until input level changes, by triggering a change. These are one of the major components and widely used in analog and digital circuits as it convert irregular signal into square wave and to remove noise problem [4]. These are used to improve the 0 or 1 control state [7] and decrease the sensitivity to noise such as sensor [5].

Schmitt trigger are design by using operational amplifier (op-amp) by connecting two limiting resistors in closed loop i.e. positive feedback but such kind of preparations are not appropriate for integration circuit in CMOS (complementary metal oxide semiconductor) technology (a) High gain of operational amplifier. (b) Area utilization of the resistor is poor. (c) Current limiting of resistor values [2]. The Schmitt trigger is a comparator having hysteresis which is implementing by applying a positive feedback to non inverting input of differential amplifier or comparator. The dual threshold action is termed as hysteresis. In general words comparator is a

electronic component which compare two voltages or current and give digital output. The major difference between comparator and Schmitt trigger is DC transfer characters tics [8]. The comparator shows only single switching threshold point of transfer characteristics whereas Schmitt trigger show two different switching threshold points, positive and negative input going signal as shown in figure.1. The causes for Schmitt trigger to be trendy because it has the property of hysteresis, due to the presence of two threshold levels. The important application for Schmitt trigger circuit is broadly used in input buffer to get better noise immunity, SRAM work as decision making circuit. [11], pulse with modulation circuit [9].

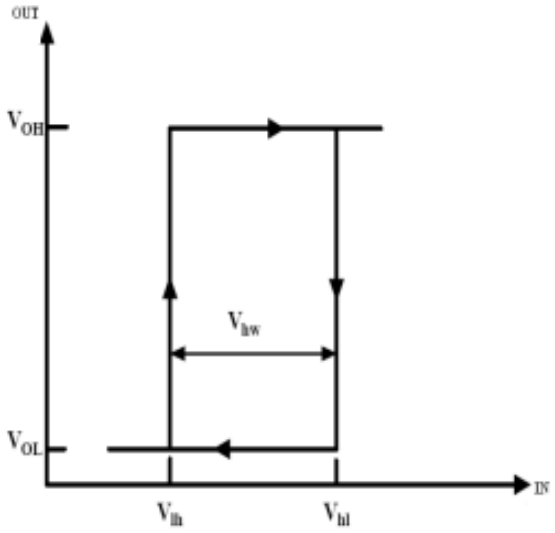

Figure 1: DC transfer characteristic curve

The CMOS circuits contain high speed due to which some power dissipation may occur: the leakage current, which is related to the logical states of the circuit and independent to switching activity. The short circuit power dissipation which is used when both NMOS and PMOS transistors in the circuit turned ON, at the same time for short duration of time during switching which results in direct current path between VCC and ground. The capacitance current which flows for charging and discharging capacitive load during logic changes.

1.1. Power Minimization Techniques

There are many techniques to reduce the power minimization in CMOS circuit. Some of them are given below:

- Reducing chip and package capacitance: It can be achieved through process development such as SOI with partially or fully depleted wells, CMOS scaling to submicron device sizes, and advanced interconnect substrates such as Multi-Chip Modules (MCM). This approach can be very effective but is also very expensive and has its own pace of development.
- Scaling the supply voltage: This approach can be very effective in reducing the power dissipation, but often requires new IC fabrication processing. Supply voltage scaling also requires support circuitry for low-voltage operation including level-converters and DC/DC converters as well as detailed consideration of issues such as Signal-To-Noise margins.
- Employing better design techniques: The approach promises to be very successful because the investment to reduce power by the design is relatively small in comparison to the other three approaches and because it is relatively untapped in potential.

2. RELATED WORKS

Numerous designs have been proposed for Schmitt Trigger for different application by various researchers with several techniques. Some of them are:

1. Priyanka Sharma and Rajesh Mehra [15]. In this paper author design a low power TSPC edge triggered D flip-flop with five transistors and analysis the result with eleven TSPC D-FF at 70nm and 90nm technology.
2. C.Zhang et. al., [3]. In this paper author design two Schmitt trigger which uses dynamic body bias technique and operate each of them at different voltages. By this method threshold voltage goes lower.
3. Chung-Yu Wu et. al., [9]. In this paper new structure of low photo current CMOS retinal focal plane sensor with pseudo BJT and adaptive Schmitt trigger is proposed on small chip area.
4. S.L. Chen et. al., [7]. In this paper the authors design a low voltage device which receive high input signal with gate oxide. The circuit works on 3.3V without any problem of gate oxide. The Schmitt trigger is suitable for mixed voltage input and output interference to receive input signal.
5. C. Kho Pham[8]. In this paper the author proposed the voltage control threshold circuit which able to control threshold voltage of gate.
6. Ghulam Ahmad Raza et. al., [16]. In this paper author design a Schmitt trigger and its various layouts by using PMOS and NMOS transistors at 90nm technology. Compare the various power consumption and surface area of the transistors.
7. Pushpa Saini et. al., [12]. In this paper author proposed a technique which reduce the leakage power and glitch at 90nm and 250nm technology which result in ultra low power consumption.
8. Ricardo Guazelli et. al., [18]. In this paper author tell how Schmitt trigger on output inverter can help mitigating problem occur in null convention logic gates (NCL).
9. Kobchai Dejhan [6]. In this paper author design a inverting and non inverting bootstrapped Schmitt trigger for higher voltages.
10. Swati kundra et. al., [13]. In this paper author proposed a Schmitt trigger using four transistors at 130nm technology with comparison to six transistor Schmitt trigger.
11. Priyanka Sharma and Rajesh Mehra [14]. In this paper author uses MTCMOS technique for reduction of leakage power.

3. CONVENTIONAL LOW POWER SCHMITT TRIGGER

3.1. Circuit Description

Many designs have been proposed for the Schmitt triggers. Several techniques, as have been implemented to reduce the power consumption. In this section, we survey the various design of Schmitt trigger. The simple structure of the trigger was design by using three NMOS and three PMOS transistors [11] consist of six transistors shown in Figure 3(a). This model was design in Microwind software tools. The working is similar to inverter but it have hysteresis curve which makes it different from the NOT gate. The both transistor connected back to back NMOS and PMOS allows filtering both 1 to 0 and 0 to 1 glitches. When we gave supply through VDD. The transistor P1, P2 and N3 act as a closed switch we get output at across out1. Similarly when the

switch IN1 is press goes 0 to 1. It will turn transistors P1, P2 and N3 open and N1, N2 and P3 goes closed there will be no output across out1. All the current flow through ground from N2 when it acts as a closed switch. The transistor P3 is closed when in1 is high and transistor N3 is closed when IN1 is low. So it work as a Not gate.

The timing simulation of six transistor Schmitt trigger is shown in Figure 3 (b) It is evident from the timing diagram when the input is low the output is high which means when input is 0 its output is 1 i.e. ON. It work as a inverter

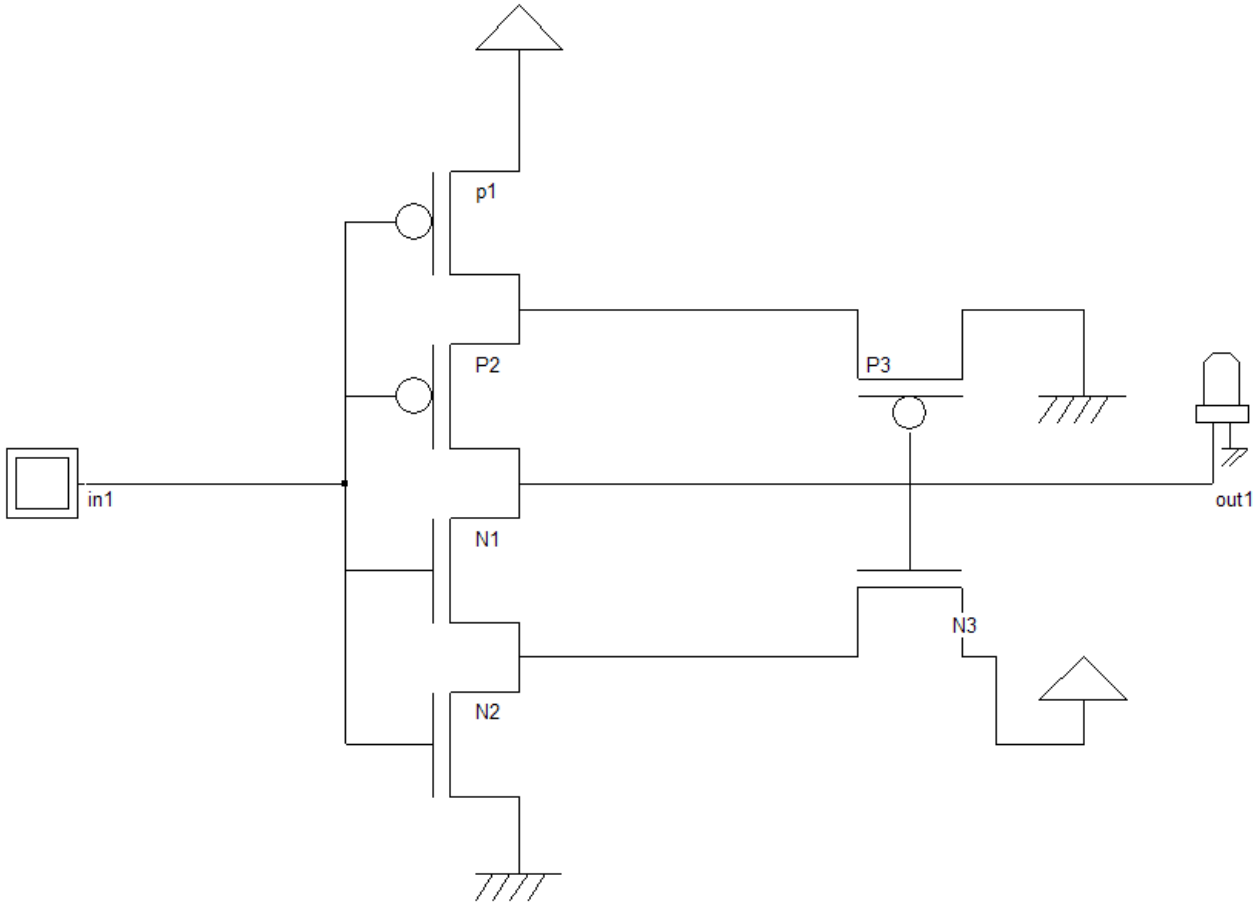

Figure 3: (a) Conventional 6T- Schmitt trigger CMOS

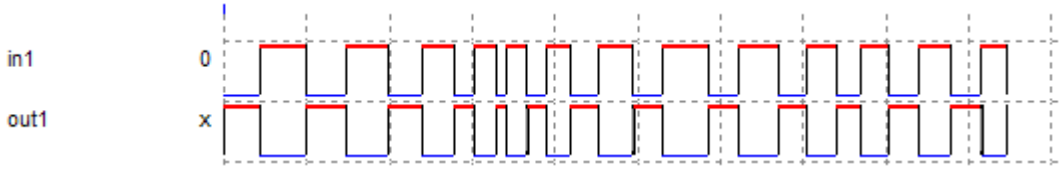

Figure 3: (b). Conventional 6T- Schmitt trigger CMOS timing simulation

The second, traditional Schmitt trigger CMOS was built by using three PMOS and two NMOS [13] shown in Figure 3 (c). The purpose of designing triggers to increase the circuit robustness due to their ability to reject noise, using hysteresis properties. In this 5 transistors are used three PMOS and two NMOS. When the input is given to switch S1 N1, N2 and P3 act as a closed switch and P1 and P2 act as an open switch all the current flow from ground there will be no output across out1. When S1 is made low mean 0 than P1, P2 act as a closed

switch and we get the output across out1. In other words, when the input is low the output is high. The PMOS is connected to the ground, and it work as a filter.

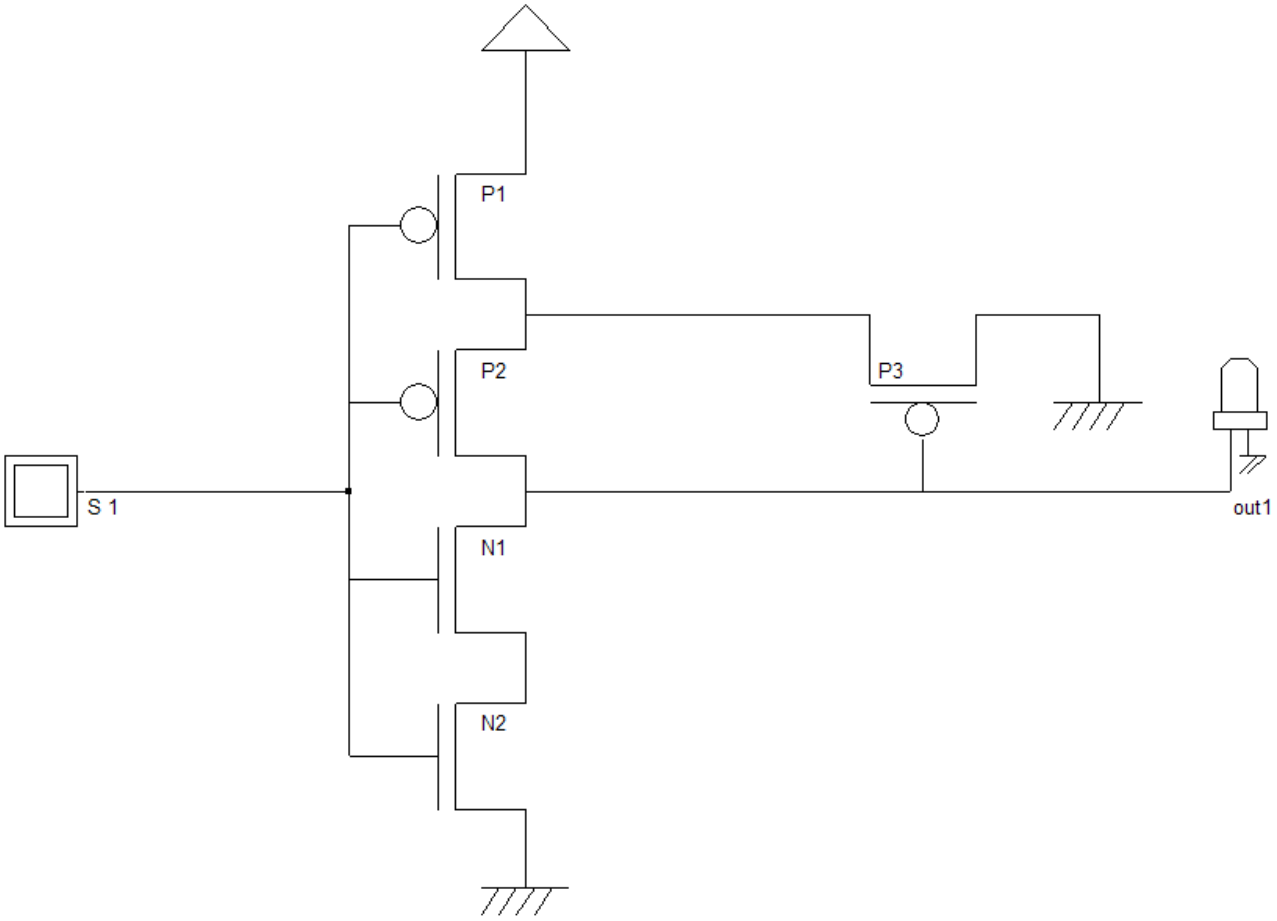

Figure 3: (c) 3PMOS and 2 NMOS Schmitt trigger

The timing simulation of three PMOS and two NMOS Schmitt trigger is shown in Figure 3 (d) when there is no input S1 = 0, the output is high, out1 = 1. When the input is high, S1 = 1, the output is low, out1 = 0.

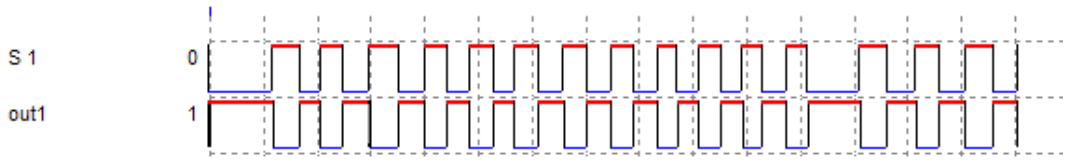

Figure 3: (d) Conventional 3PMOS and 2 NMOS Schmitt trigger CMOS timing simulation

Similarly by using 2 PMOS and 3 NMOS trigger is implemented [13] shown in Figure 3 (e). In this two PMOS and three NMOS are used for fabrication of Schmitt trigger its working is also same as previous conventional triggers. When S1 = 0, the P1, P2 and N3 are in closed state where N1 and N2 are in open state due to which we get output across out1. When S1 = 1, N1 and N2 are closed and remaining transistors turn open and there will be no output. The N2 enables filtering when low to high glitches on in1.

It is clear from the timing simulation Figure 3(f) when S1 = 0, The out1 = 1. In other words we can say when S1 = OFF, the out1 = ON.

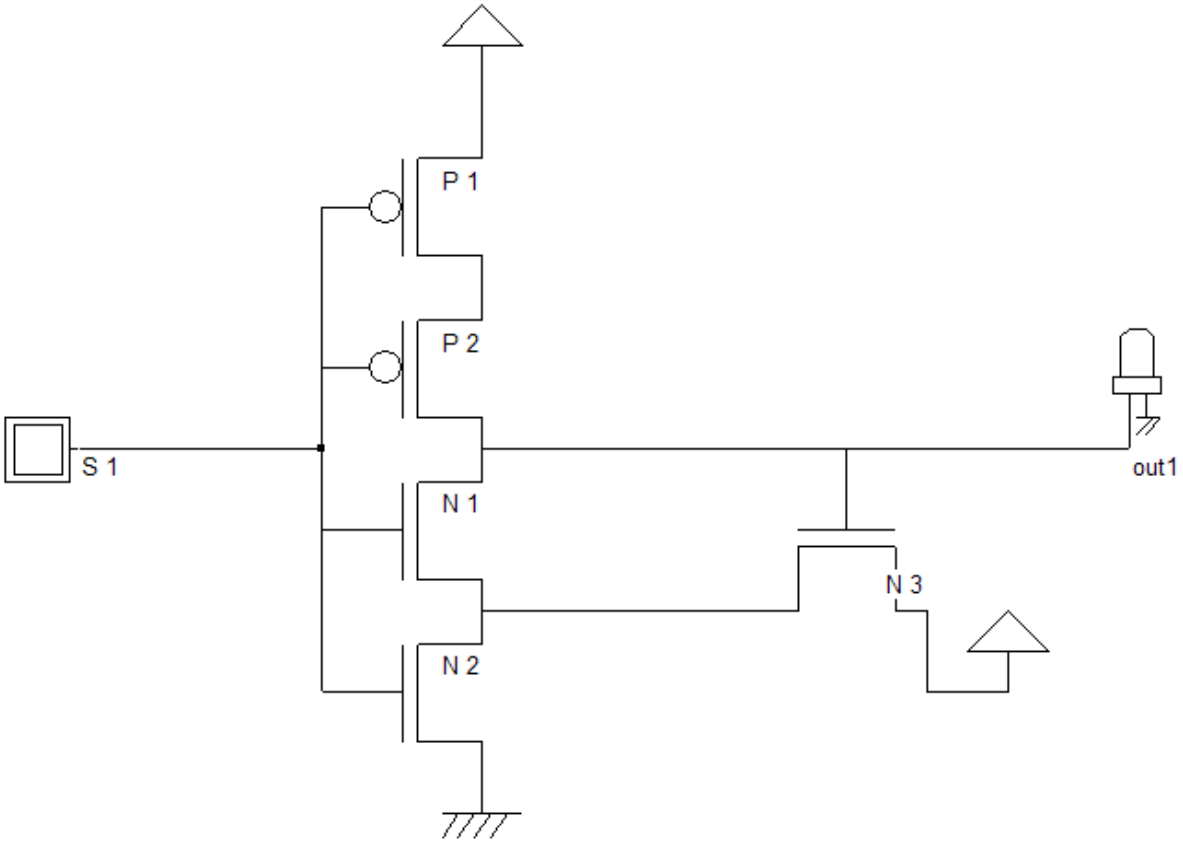

Figure 3: (e) 2PMOS and 3 NMOS Schmitt trigger

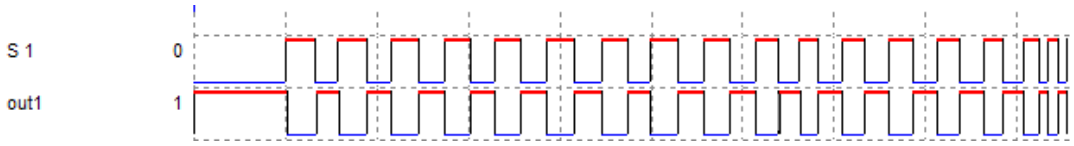

Figure 3: (f) Conventional 2PMOS and 3 NMOS Schmitt trigger CMOS timing simulation

4. PROPOSED TECHNIQUES FOR LOW POWER SCHMITT TRIGGER

Many techniques and ideas have been applied to the Schmitt trigger to enhance its characteristics such as speed [14] [15], low temperature coefficient functioning [16] and tunable hysteresis [17]. The reason for designing the trigger as it is the basic building block of electronic circuits. It is used in both analog and digital circuits. Power is being given equal importance in comparison to area and speed [18]. The purpose of this paper is to study the various conventional Schmitt triggers and design proposed Schmitt trigger in the terms of hysteresis curve, delay introduced, power dissipation and find the most suitable low power Schmitt trigger with less number of NMOS and PMOS. Due, to which the cost and size of circuit is reduced.

4.1. Circuit Description

Proposed 2PMOS and 3 NMOS Schmitt trigger

The design of proposed Schmitt triggers is displayed in Figure 4(a). Connecting of NMOS and CMOS with different methods minimize the power consumption. The proposed trigger is construct by using two PMOS

and three NMOS. The switch in1 is connected to P1, N1 and N2 transistors, the supply voltage VDD is given to the source of P1 and P2 transistor. When in1 is low, the P1and N3 work as a closed switch and output turns high. When the input signal is given to the switch in1 high than P2,N1 and N3 work as a closed switch and P1 and N3 act as a open switch due to which output show no current that is output is low. Its working is similar to NOT gate. When input is low out is high, when input is high output is low. The DSCH and Microwind tool is used for designing the proposed Schmitt trigger. Its power consumption is also minimum The PMOS channel width is 2.0µm and channel length is 1.2µm is used and NMOS channel width is 1.0µm and channel length is 0.12µm. The timing diagram of Proposed 2PMOS and 3 NMOS Schmitt trigger is display in Figure 4(b).

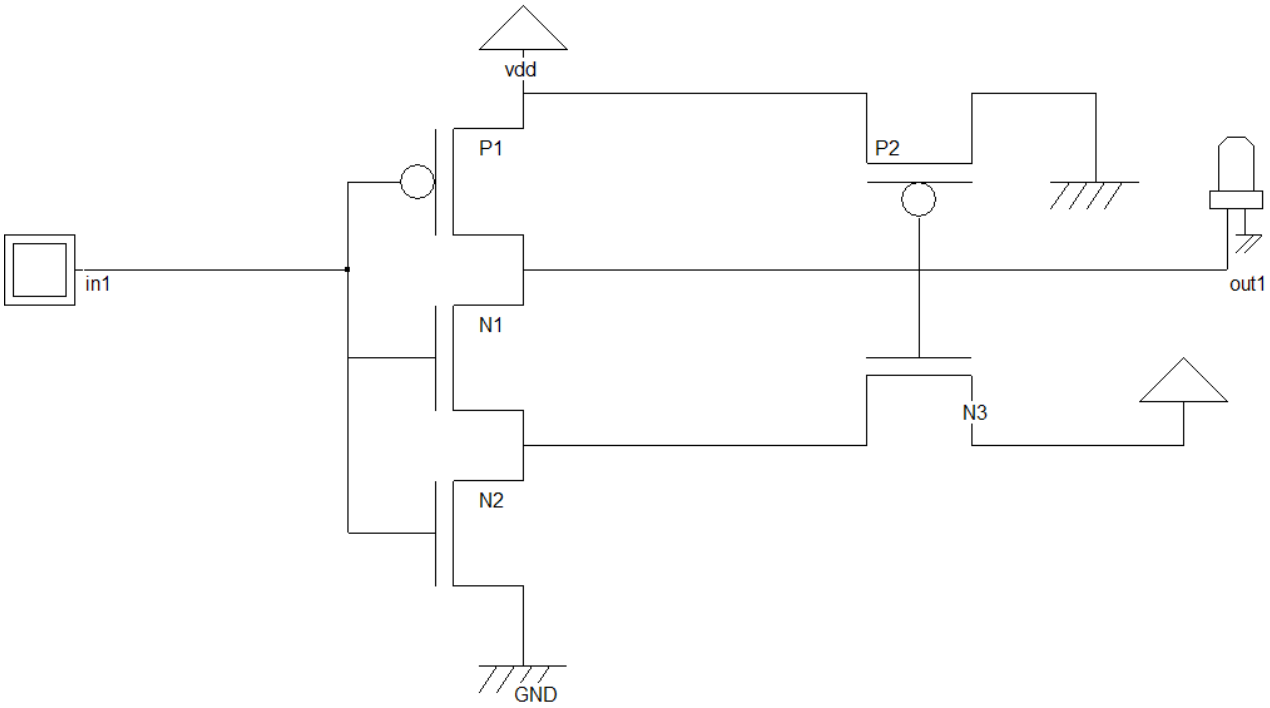

Figure 4: (a) Proposed 2PMOS and 3 NMOS Schmitt trigger

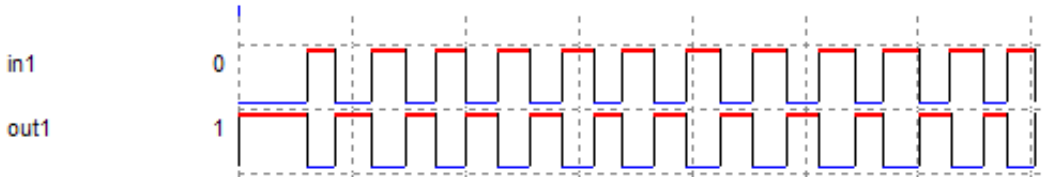

Figure 4: (b) Proposed 2PMOS and 3 NMOS Schmitt trigger CMOS timing simulation

Proposed 1PMOS and 3 NMOS Schmitt trigger

The other proposed design of trigger is shown in Figure 4(c). In this four transistors are used for designing, one PMOS and three NMOS. The switch S1 is connected to the gate of the NMOS and PMOS. Supply voltage VDD is given to the source of P1 and drain of N3. When input is provided the supply voltage VDD is made permanently high and Switch S1is high, N1 and N2 is made closed due to all the current goes ground due to which there is no output occur. When the switch S1 is low, than P1 and N3 is turn closed and N1, N2 goes open. Due to which output turns high. This also reduces the power dissipation and the area of transistors. The Timing

diagram is illustrated in Figure 4(d). It is evident from the timing diagram when S1=0 than out1=1 and when S1=1 than out1=0.

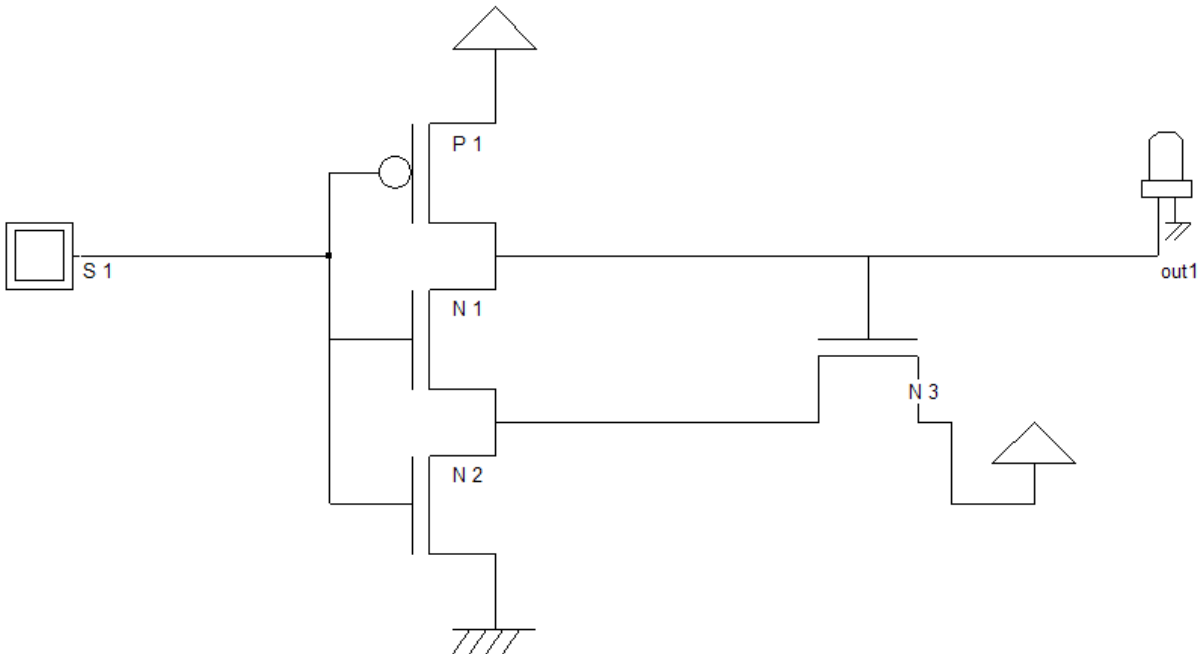

Figure 4: (c) Proposed 1PMOS and 3 NMOS Schmitt trigger

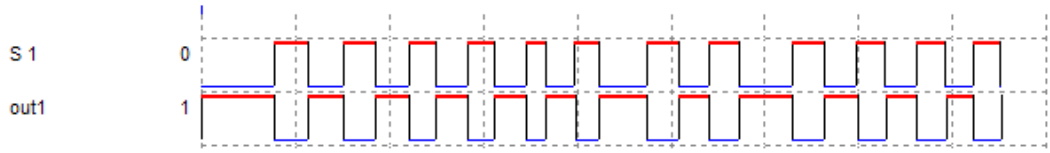

Figure 4: (d) Proposed 1PMOS and 3 NMOS Schmitt trigger CMOS timing simulation

Proposed 3PMOS and 1 NMOS Schmitt Trigger

The other method of implementing trigger is by using three PMOS and a single NMOS illustrate in Figure 4(e). In this three PMOS and a single NMOS is used. The switch S1 is connected to the P1, P2 and N1. The output of P2 is connected to the gate of P3. When the input is low switch S1=0, P1 and P2 act as a closed switch the supply voltage pass from P1 and P2 which make the output high which makes the LED glow. When switch S1 is turn ON than N1 goes closed and P1 and P2 turn open by which all current go towards ground from N1. There is no output across out1. By this we can achieve power reduction and reduction in size. The Figure 4(f) verifies the behavior of three PMOS and a single NMOS.

Proposed Sleep Transistor Schmitt Trigger

Similar circuit is purposed by using three PMOS and single NMOS. The P1 transistor is having high threshold voltage known as sleep transistor [18] [12]. Since PMOS P1 sleep transistor is connected to the body of PMOS P2 and P3 transistor. In this sleep transistor P1 is given input supply VDD over the source and gate is done ground. So, the P1 is permanently turning ON, it is not control by switch. The output of P1 is given to source of P2 and P3. When the S1 is turned ON, N1 is become close and P2 and P3 work as a open gate. So there is no output across out1. The current flows from power supply to ground nodes known as static biasing current [18].

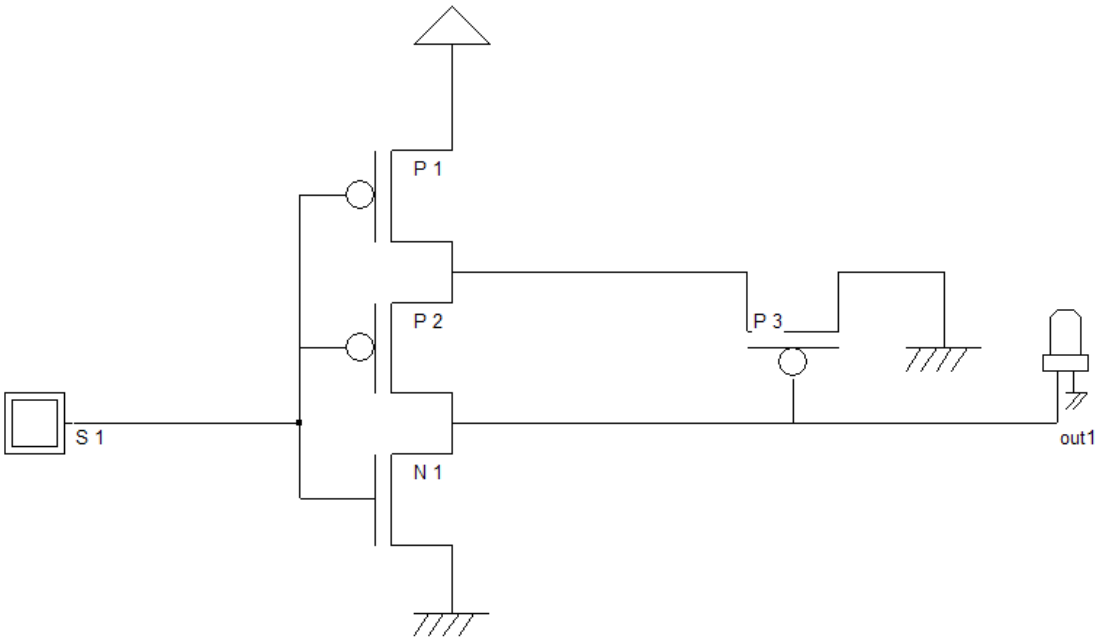

Figure 4: (e) Proposed 3PMOS and 1 NMOS Schmitt trigger

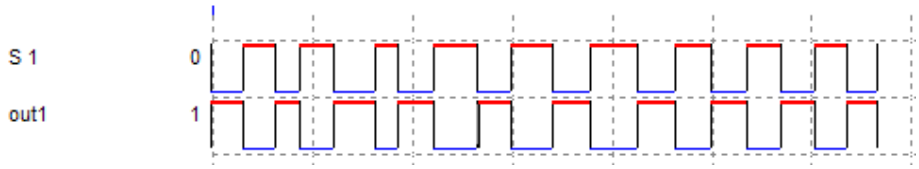

Figure 4: (f) Proposed 3PMOS and 1 NMOS Schmitt trigger CMOS timing simulation

When there is no input given to S1. The output turn high and output is seems across out1. The timing simulation of CMOS is shown in Figure 4(h).

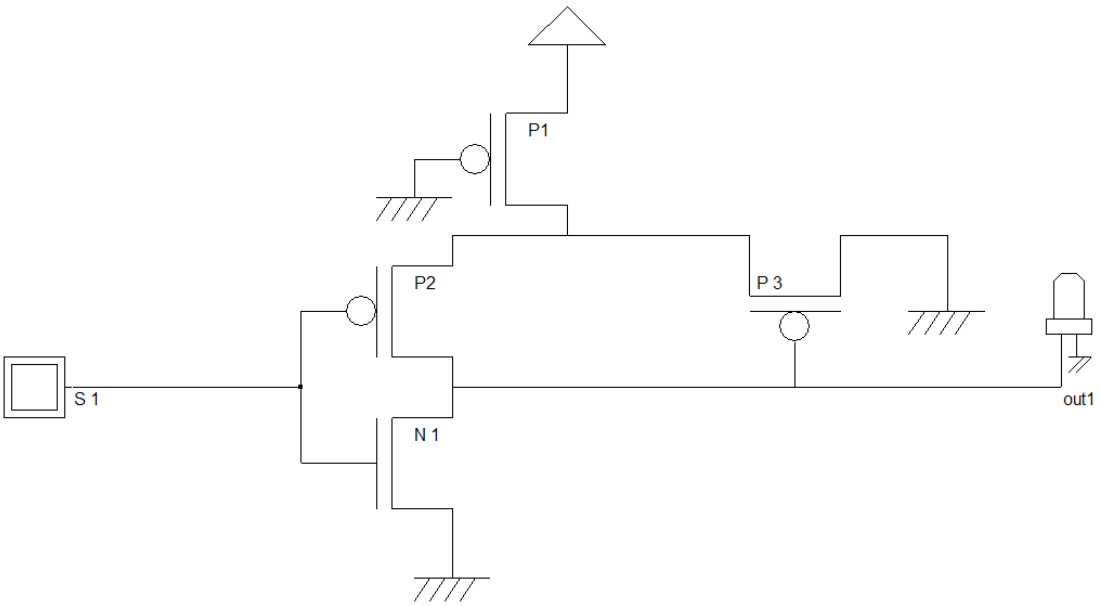

Figure 4: (g) Proposed sleep transistor Schmitt trigger

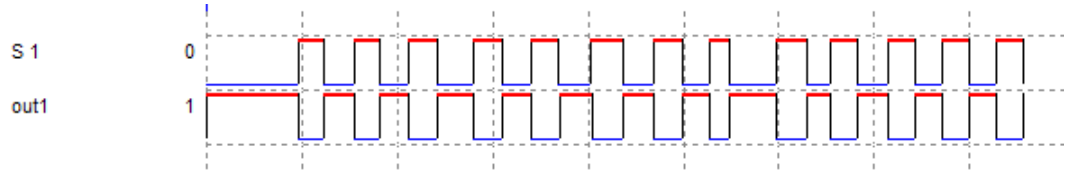

Figure 4: (h) Proposed sleep transistor Schmitt trigger CMOS timing simulation

4.2. Simulation Layout

Conventional Schmitt Triggers Layout

The layout design illustrates how small features can be and approximately packed in a particular manufacturing process. The designers generate the different chart by using different techniques. The purpose of making layout chart is to place and connect all the components and to design the chip. The layout designs tell us about the size, performance and manufacturability. The Verilog file is used to generate the layout for a given circuit. This layout can be designed at 0.12um and 90nm. The following layouts of conventional and proposed Schmitt triggers are as shown.

In Figure 4.2(a) the auto generated layout of Schmitt trigger design on rule called λ based rule which describes how small feature can be and how closely packed. Different logical layers are used for designing, to generate the layout of the circuit. There are specific layers for metals, contacts and diffusion area and poly silicon. The dark blue colour in the layout chart represent metal1 and metal2; red colour represent polysilicon, light green colour indicates p+ diffusion.

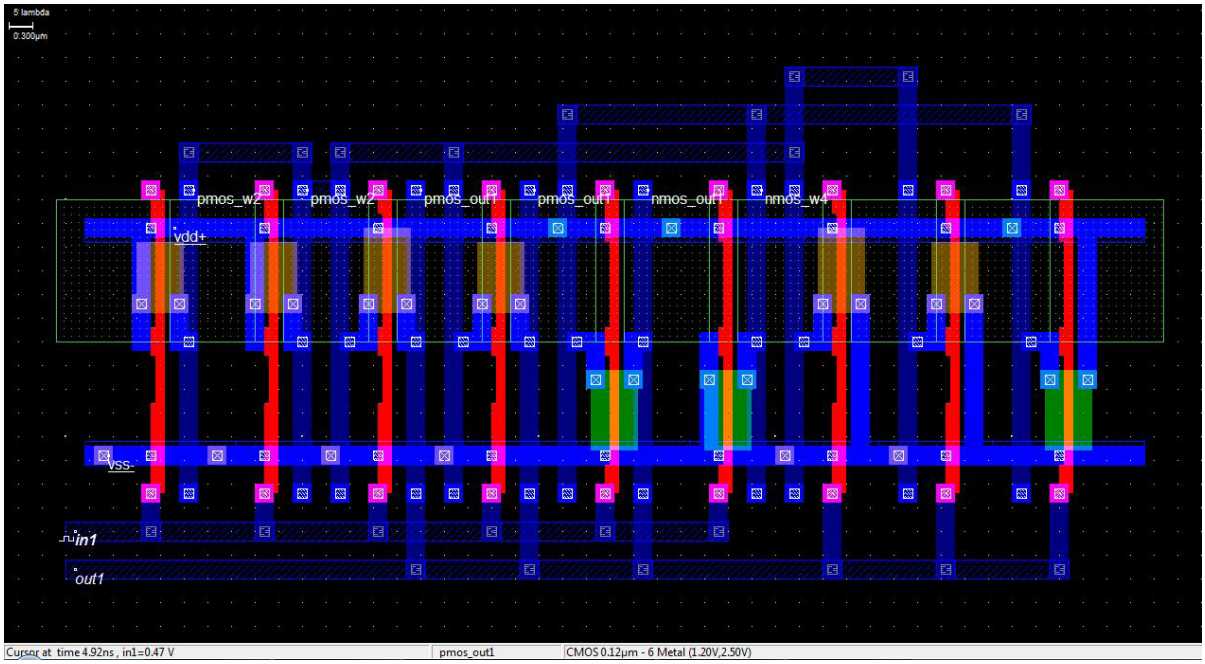

Figure 4.2: (a) Conventional 6T schmiit trigger layout at 0.12um

In Figure 4.2 (b) a result of simulation, power dissipation by using conventional six transistors Schmitt trigger is shown which is 14.929µW at 1.2V. The hysteresis property of Schmitt trigger, in which the input threshold change depending on input whether it is on rising edge or falling edge. In other words hysteresis is the difference between the input signal at which trigger is standby mode and active mode. A small amount of

hysteresis can also be useful in Schmitt trigger because it have ability to reduce the circuit sensitivity to noise as well as reduce multiple transition of output when state changes.

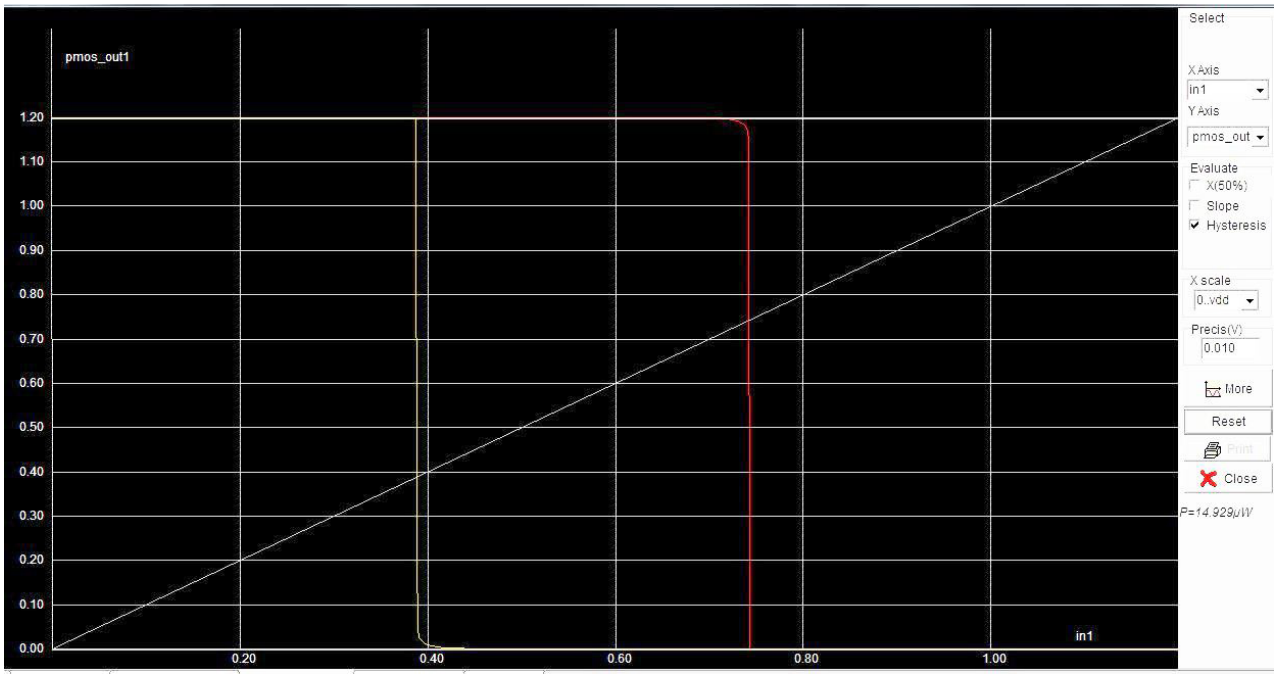

Figure 4.2: (b) hysteresis and power measurement of Schmitt trigger

The layout of conventional three PMOS and two NMOS is shown in Figure 4.2(c). Its layout is design at 0.12um technology. In Figure 4.2 (d) a result of simulation, power dissipation and hysteresis curve by using conventional three PMOS and two NMOS Schmitt which is 8.812µW at 1.2V is.

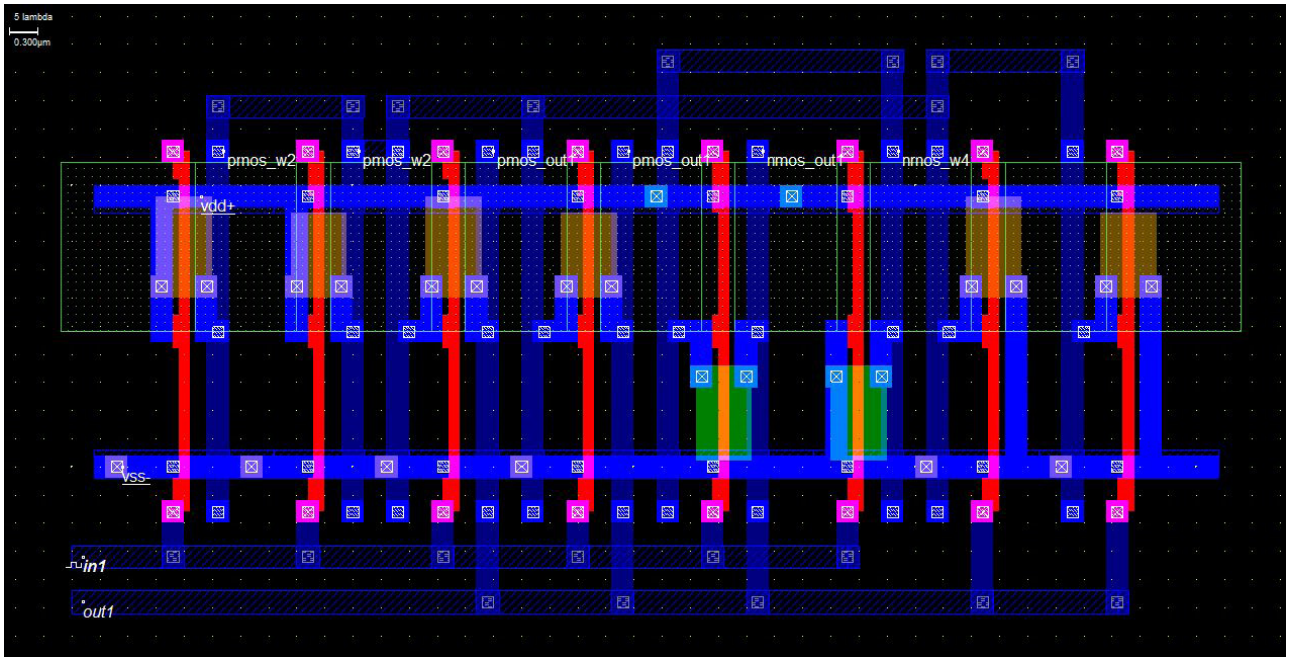

Figure 4.2: (c) Conventional 3PMOS and 2 NMOS schmiit trigger layout

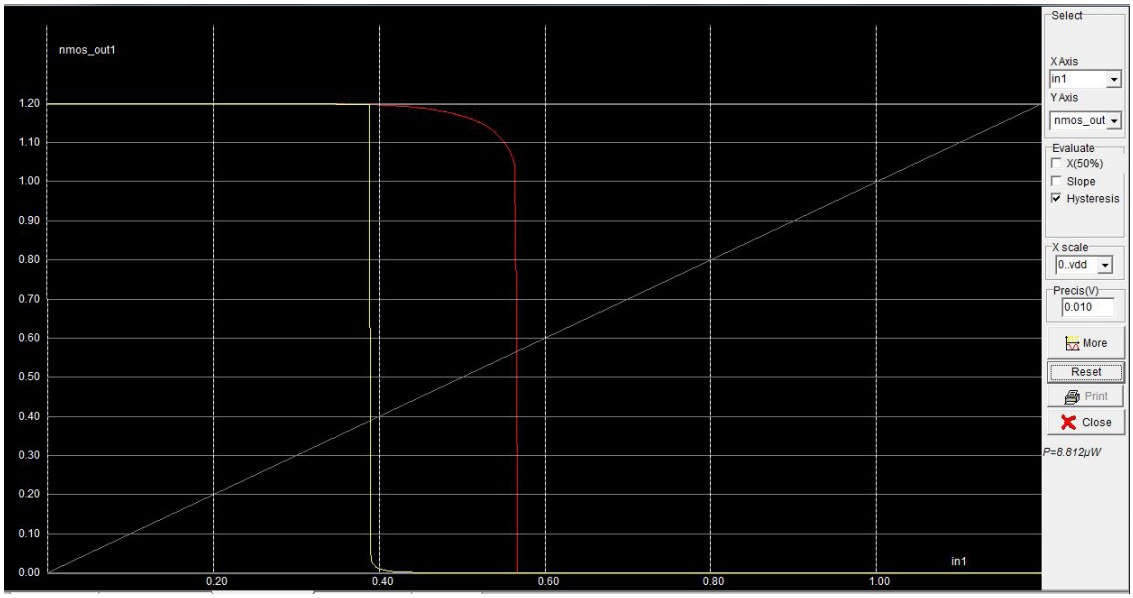

Figure 4.2: (d) hysteresis and power measurement of Schmitt trigger

In Figure 4.2(e) the layout of conventional two PMOS and 3NMOS is illustrate. In Figure 4.2(f) illustrate hysteresis curve and power dissipation of the circuit.

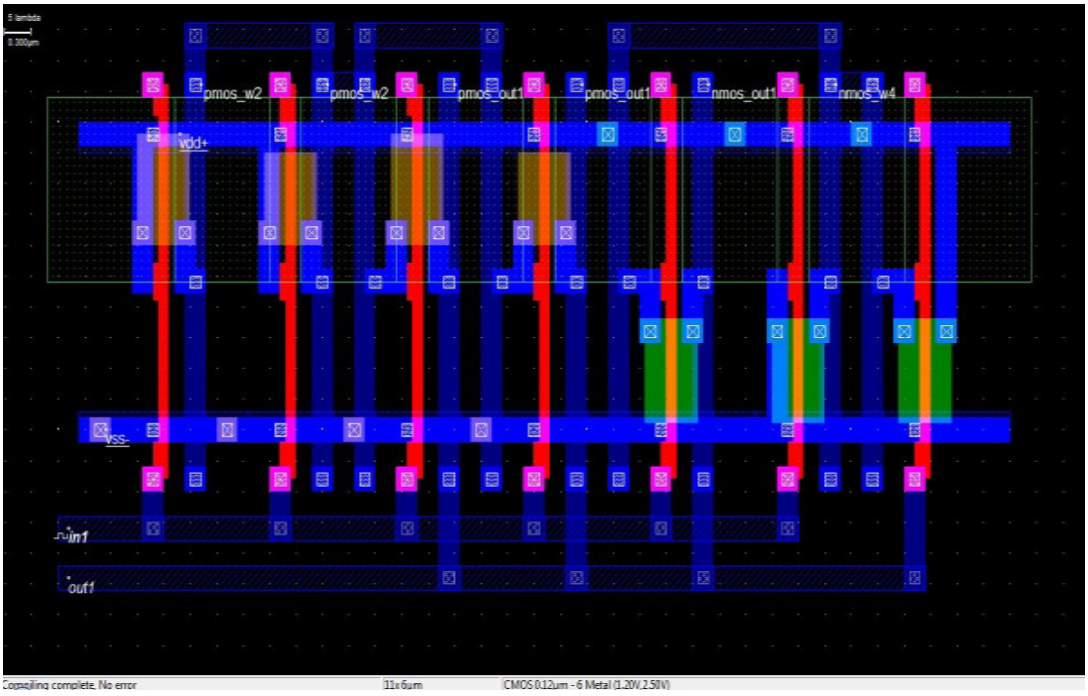

Figure 4.2: (e) Conventional 2PMOS and 3 NMOS schmiit trigger layout

Proposed Schmitt Triggers Layout

The proposed circuit has been performed by using Microwind DSCH simulator. Placing the CMOS with different topologies leads to reduction of power consumption of the circuit. The Figure 4.2 (g) to 4.2(n) shows the layout and its hysteresis curve results.

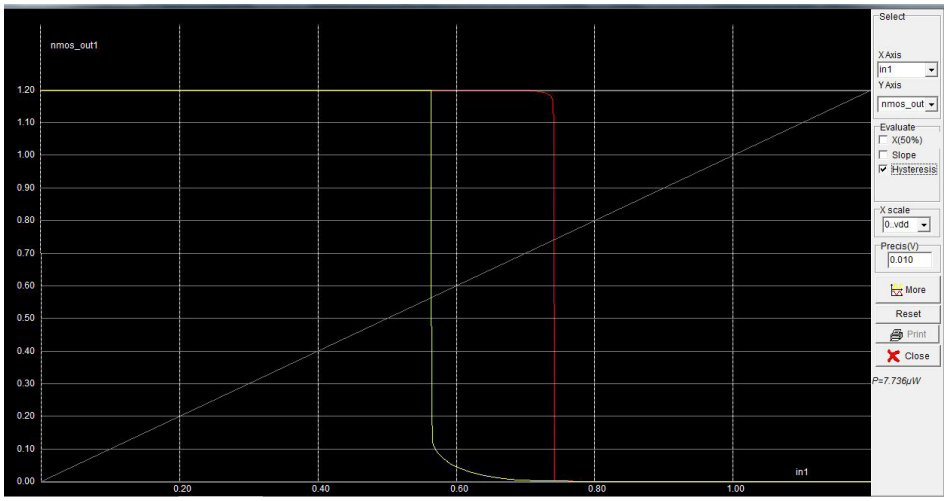

Figure 4.2: (f) hysteresis and power measurement of Schmitt trigger

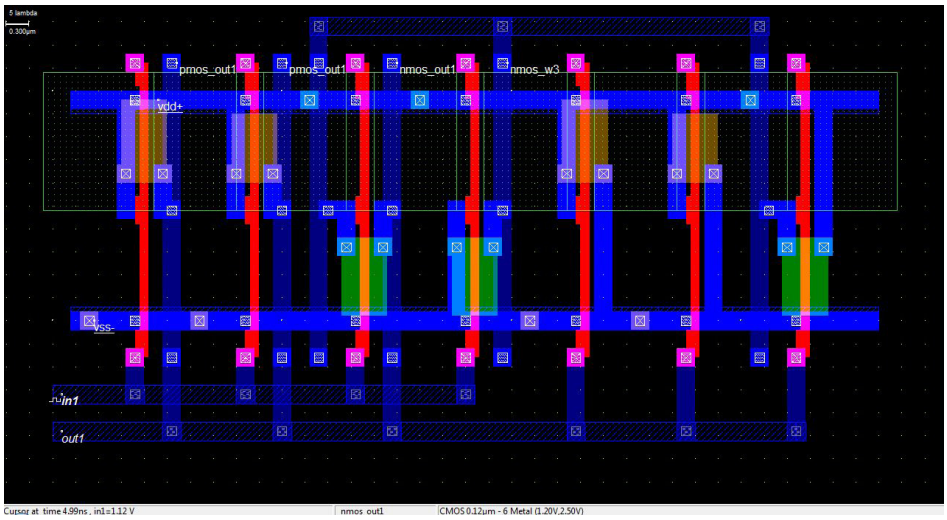

Figure 4.2: (g) Proposed 2PMOS and 3 NMOS schmiit trigger layout

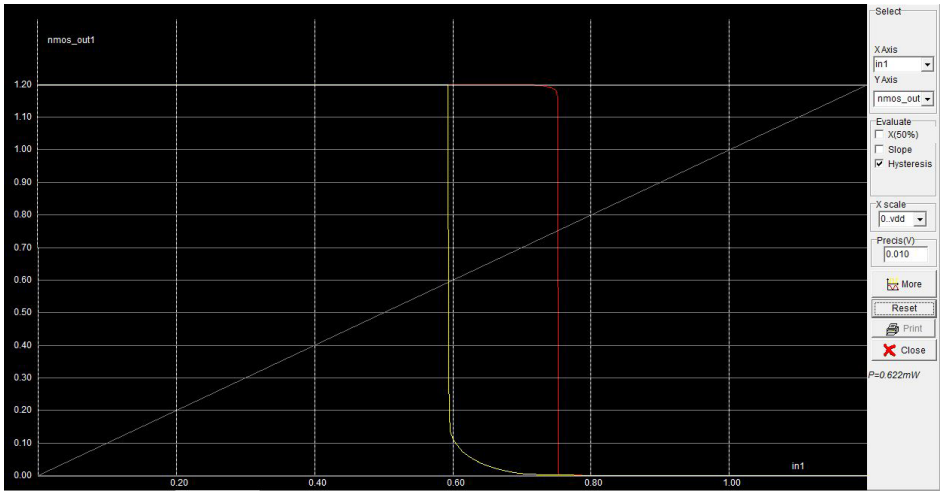

Figure 4.2: (h) Power Dissipation and hystersis curve when VDD=1.2V

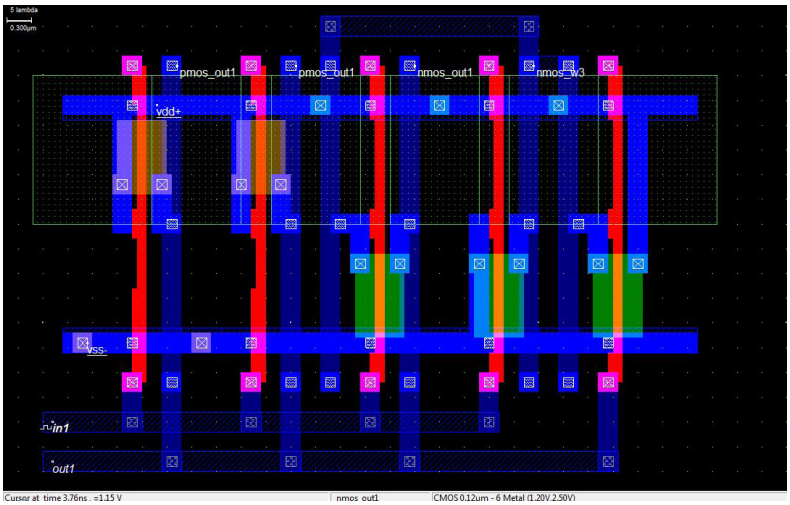

Figure 4.2: (i) Proposed 1PMOS and 3 NMOS schmiit trigger layout

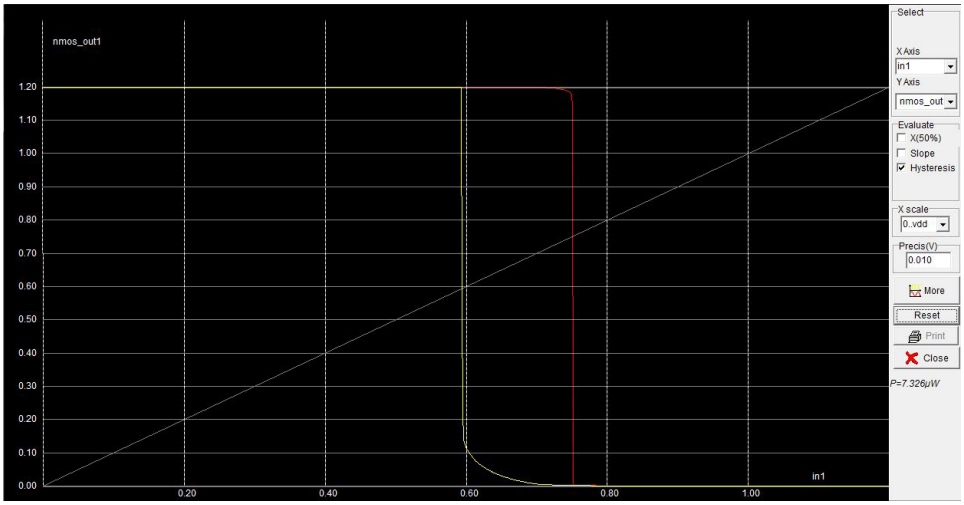

Figure 4.2: (j) hysteresis and power measurement at VDD=1.2V

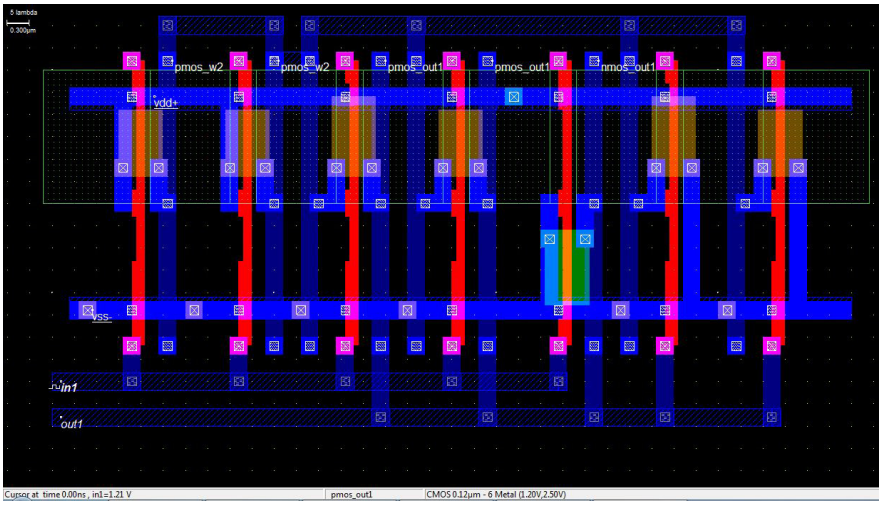

Figure 4.2: (k) Proposed 3PMOS and 1 NMOS schmiit trigger layout

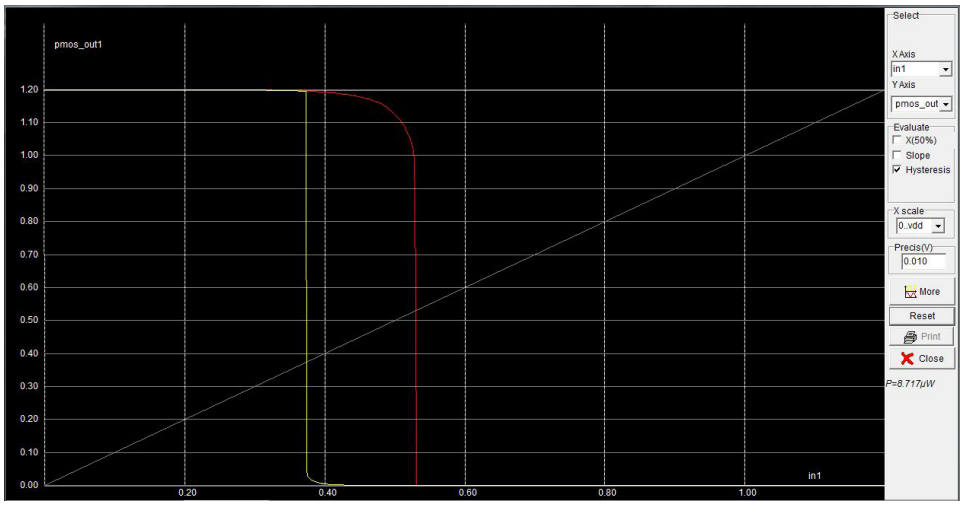

Figure 4.2: (l) Power Dissipation and hystersis curve

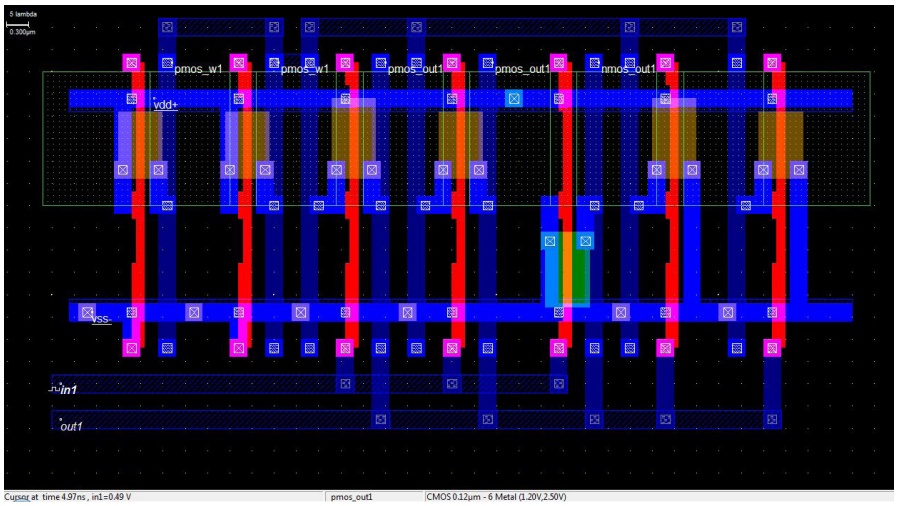

Figure 4.2: (m) Proposed Sleep transistor Schmitt trigger

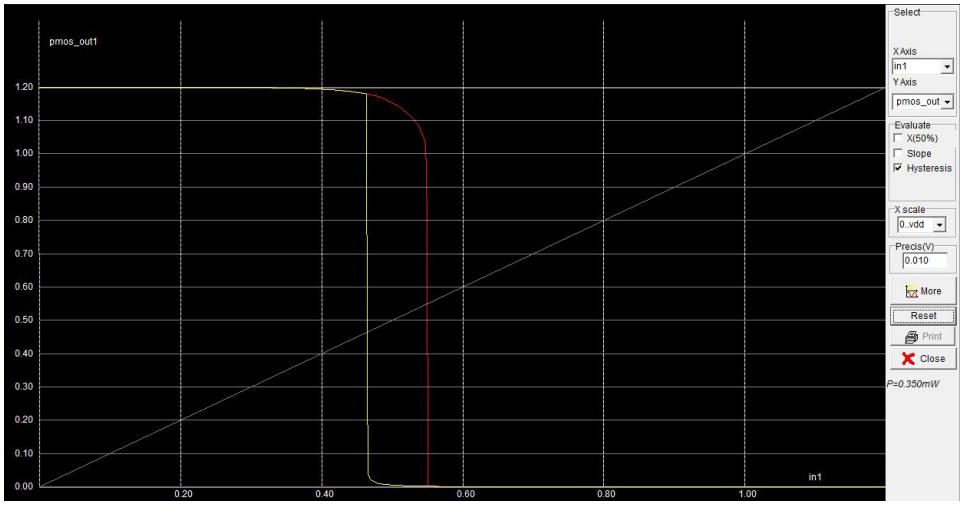

Figure 4.2: (n) Power Dissipation and hystersis curve

5. RESULTS ANALYSIS AND DISCUSSION

5.1. Various Conventional Schmitt Triggers Parameters

In this section, various performance analysis of different Schmitt triggers design. Various designed are planned by giving different voltages with default temperature of 27oC in order to reduce power dissipation. All the designs are made by using DSCH and micro wind tool at 120nm and 90nm technology.

Table 1
Comparison of various Conventional schmitt triggers at 120nm

Parameters	*Power Dissipation Conventional Schmitt trigger*		
Supply voltage	*6T Schmitt Trigger*	*3 PMOS-2 NMOS Schmitt Trigger*	*3 PMOS-2 NMOS Schmitt Trigger*
1V	9.012 µW	5.515 µW	4.541 µW
1.2 V	14.929 µW	8.812 µW	7.736 µW
1.5 V	26.618 µW	15.468 µW	14.130 µW
2 V	55.717 µW	33.913 µW	29.417 µW

From Table 1. Illustrates the different Schmitt triggers on 120nm scale at different voltages have different power dissipation. From Table 2. It seems when voltage 1.5v and 2v is given to the 3PMOS and 2NMOS Schmitt trigger the power dissipation goes reduce at 90nm with comparison to 120nm scale.

Table 2
Comparison of various Conventional schmitt triggers at 90nm

Parameters	*Power Dissipation Conventional Schmitt trigger*		
Supply Voltage	*6T Schmitt Trigger*	*3 PMOS-2 NMOS Schmitt Trigger*	*3 PMOS-2 NMOS Schmitt Trigger*
1V	11.031 µW	7.595 µW	45.285µW
1.2 V	16.663 µW	11.352 µW	8.033 µW
1.5 V	27.282 µW	18.363 µW	13.250 µW
2 V	54.255 µW	35.832 µW	26.572 µW

5.2. Various Proposed Schmitt Triggers Parameters

In this various results are made on proposed Schmitt triggers on 120nm and 90nm.scale.

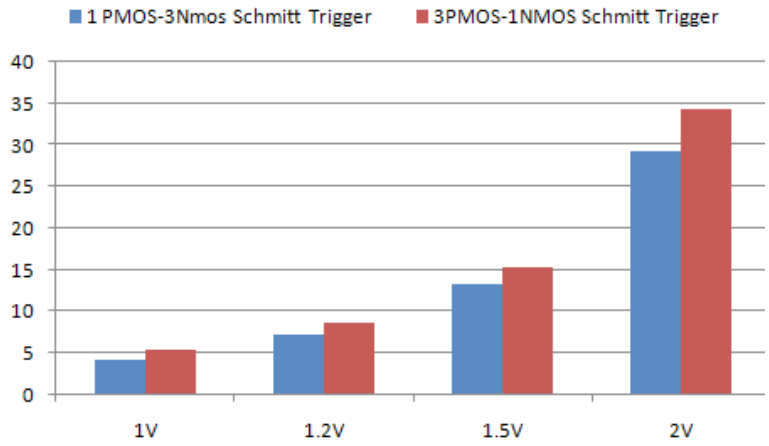

Figure 5.2: (a) Comparative Analysis of Proposed Schmitt Trigger at 120nm (Power in µW)

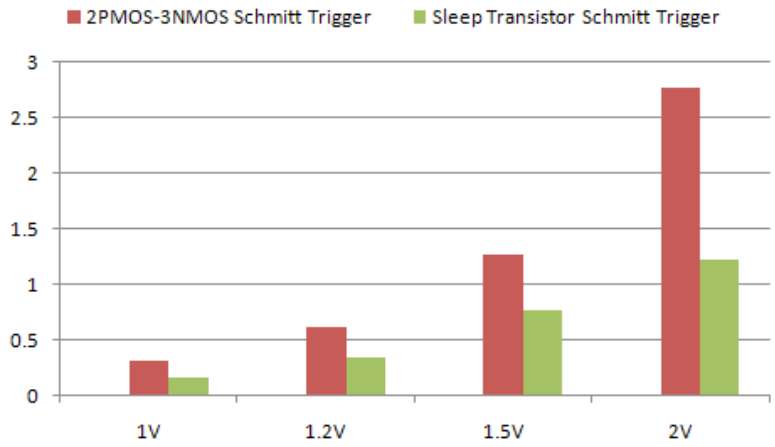

Figure 5.2: (b) Comparative Analysis of Proposed Schmitt Trigger at 120nm (Power in mW)

The bar graph Figure 5.2(a) and Figure 5.2(b) illustrates various power dissipation of Schmitt trigger at different voltages. 2PMOS and 3NMOS Schmitt trigger have more power dissipation as compare to sleep transistor Schmitt trigger. The minimum power consumed by single PMOS and 3NMOS Schmitt trigger among all the proposed Schmitt triggers.

The Table 3 reveals various power dissipation at 90nm technology. The sleep transistors have less power dissipation at 90nm technology as compare to two PMOS with three NMOS. While going to 120nm to 90nm scale for CMOS technology the power dissipation also increase. The minimum power dissipation consumed proposed Schmitt trigger is single PMOS with three NMOS at various voltages.

Table 3
Comparison of various Proposed schmitt triggers at 90nm

Parameters	*Power Dissipation Proposed Schmitt trigger at 120 nm*			
Supply voltage	*2PMOS-3NMOS Schmitt Trigger*	*1PMOS- 3NMOS Schmitt Trigger*	*3PMOS-1NMOS Schmitt Trigger*	*Sleep transistor Schmitt Trigger*
1V	0.438mW	4.406 µW	7.521µW	0.217 mW
1.2 V	0.694mW	6.769 µW	11.274µW	0.356 mW
1.5 V	1.180mW	11.444µW	18.419µW	0.625 mW
2 V	2.261mW	24.766µW	37.895µW	1.230 mW

6. CONCLUSION

From the various simulation and comparison results it is seems that proposed single PMOS with 3NMOS consume less power dissipation at both 120nm and 90nm scale. The proposed circuit decreases the size, power and area of the circuit. It has better performance than conventional Schmitt trigger. It can be used in various applications such as squaring circuit, sine to square comparator, amplitude comparator and many more and it increases the noise immunity as it is a primary element of electronic circuits.

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