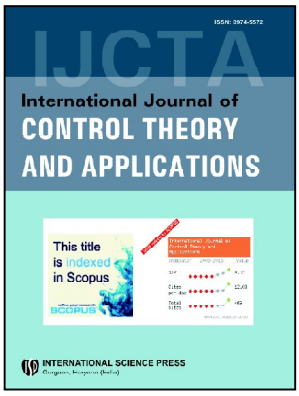

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Simulation and Performance Evaluation of Closed Loop Pi and Pid Controlled Sepic Converter Systems

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Abstract: The objective of this work is to improve the dynamic response of SEPIC system. This paper deals with modeling and simulation of soft switched Single Ended Primary Inductor Converter (SEPIC) system. SEPIC can step up DC with low ripple in current and voltage. Auxiliary switch with clamped capacitor is added to obtain the soft switching. The modes of operation of the SEPIC system are presented. State space method is used to solve the equations of the proposed circuit. The open loop and closed loop controlled systems with step changes, multiple changes in source voltage are simulated and the corresponding results are presented. A simple PID is applied to SEPIC system to achieve voltage regulation. The response of PI controlled system is compared with that of PID controlled system. The comparison is done in terms of time domain parameters detailed from PI and PID controlled systems. The simulation studies indicate that the response with PID is faster than that of PI controlled system.

Key words: Zero Voltage Switching (ZVS), Proportional-Integral (PI) Controller, Proportional-Integral-Derivative (PID) Controller, Matlab Simulink, Closed Loop Single Ended Primary Inductor Converter (CLSEPIC).

1. INTRODUCTION

Due to high output gain flexibility, SEPIC converters have been widely employed for applications involving power factor improvement/correction [1-6], photo voltaic system [7-9] and LED lighting [10-12]. The usage of SEPIC converter is restricted especially in high voltage applications due to its voltage stresses on power semiconductor devices and low efficiency owing to hard switching operation of the power switches. Voltage multiplier techniques can overcome these two main problems associated with the SEPIC converter, thereby an improvement in the efficiency can be obtained.

To satisfy the requirement of high voltage demands in power converter systems, a highly efficient, simple, single phase bridgeless converter with automatic power factor correction and reduction in voltage stresses is presented in [1]. By applying voltage multiplier techniques to the classical SEPIC converter, a high power factor rectifier suited for universal line application is presented in [2] with the advantages of high static gain, soft commutation and an increase in efficiency. A simplified bridgeless SEPIC converter operating in discontinuous conduction mode without current loop is investigated in [3] with simultaneous reduction in conduction losses

and components. Bridgeless rectifiers derived from the conventional SEPIC and CUK converter are presented in [4]. Proposed topologies on comparison with the classical SEPIC and CUK power factor circuit resulted in less conduction losses and an increase in the conversion efficiency. In [5] the modification is made in the classical power factor correction SEPIC converter by eliminating the input bridge diode has resulted in a slightly improvement of efficiency, because of ripple- free current. In [6] experimental investigation of a new SEPIC and CUK converter, three- phase power factor correction circuit employing a single switch with the capability of voltage boosting / bucking and also the converter operating at a power factor closer to unity is provided. SEPIC converter operating in discontinuous mode without current loop is designed and analyzed in [7] to act as perfect power factor pre-regulators. Ripples present in the input current are limited and hence high quality input current is achieved by appropriately choosing the values of input inductor and intermediate capacitor.

A novel technique using a SEPIC or CUK converter to track the maximum power point of a photo voltaic cell with less hardware requirements and mathematical calculation is presented in [8] under varying meteorological conditions. The efficacy of SEPIC converter based fuzzy logic controller is investigated experimentally in [9] to track the maximum power point of a photo voltaic system under varying load conditions. Real time implementation of the system ensures optimal usage of photo voltaic array.

Achievement of high efficiency and reduction in voltage stresses by using a single stage modified SEPIC converter operating in discontinuous conduction mode to drive the LED lamps for conserving energy is given in [10]. For LED applications a novel valley- fill SEPIC derived power supply with electrolytic capacitor is given in [11]. Results indicate the improvement in the performance of LED lighting system with the use of proposed topology. A new series SEPIC implementing voltage lift techniques is presented and applied to several DC-DC converters is introduced in [12]. Experimental results indicate that the voltage lift DC-DC converter derived from the SEPIC prototype ensures high output voltage transfer gain there by enabling them to be employed for potential applications. To obtain high step up static gain and reduction in maximum switch voltage, voltage multiplier technique applied to the classical non-isolated DC-DC converter is presented in [13]. By integrating the multiplier circuit with DC-DC converter the reverse recovery current of the diode is minimized. For renewable energy systems requiring high voltage transfer gains a series of voltage lift split inductor type boost converter is provided in [14].

Motivated by the encouraging results shown in [1], the performance evaluation of PI, PID controller SEPIC converter systems is investigated in this paper. To show the superior performance of the closed loop PID controlled SEPIC converter system, extensive simulation studies have been carried out with step changes in source voltage.

The organization of the paper is as follows: After a brief introduction in section 1, the three modes of operation of ZVS resonant converter is presented in section 2. Simulation results of open loop and closed loop PI, PID controlled SEPIC converter systems are presented in sections 3 and 4. The conclusion drawn from the simulated SEPIC converter system is given in section 5.

2. OPERATION OF ZVS RESONANT CONVERTER [1]

(Adapted from Hyun-Lark Do IEEE Trans. on Power Electronics, vol. 27, no. 6, June 2012)

Different versions of classical SEPIC converter are highlighted in the literature. Fig. 1.1 represents separate inductor version whereas Fig. 1.2 refers to ripple- free SEPIC converter with a loosely coupled inductor L_c. In Fig. 1.2 replacing separate inductor L_1 and L_2 by a single magnetic component i.e a loosely coupled inductor L_c with leakage inductances L_{lk1} and L_{lk2} respectively a ripple- free input current is achieved. Leakage inductances are inevitable and the ripple- free conduction is related to leakage inductance L_{lk2} and not on L_{lk1}. It is also dependent on magnetizing inductance and the turns ratio. As ripple free input current is related to L_{lk2}, an additional inductor L_a replaced it and the tightly coupled inductor version is shown in Fig. 1.3. Fig. 1.4 shows the circuit diagram of soft switching ripple free SEPIC converter proposed by Hyun- Lark Do. In the converter, L_r resonant

inductor, clamp circuit with auxiliary switch S_a and clamp capacitor are added to the classical SEPIC converter which is shown in Fig. 1.1. The equivalent circuit of the SEPIC converter is shown in Fig. 1.5 in which L_c is modeled as magnetic inductor L_m and an ideal transformer with turns ratio 1: n. The diodes D_a and D_m are used for free wheeling purpose that are coupled across the auxiliary switch S_a and the main switch S_m. C_a and C_m represents the internal capacitances and asymmetrically the switches S_a and S_m are operated. Voltage ripple can be ignored by assuming larger values of the capacitors C_1, C_o and C_c.

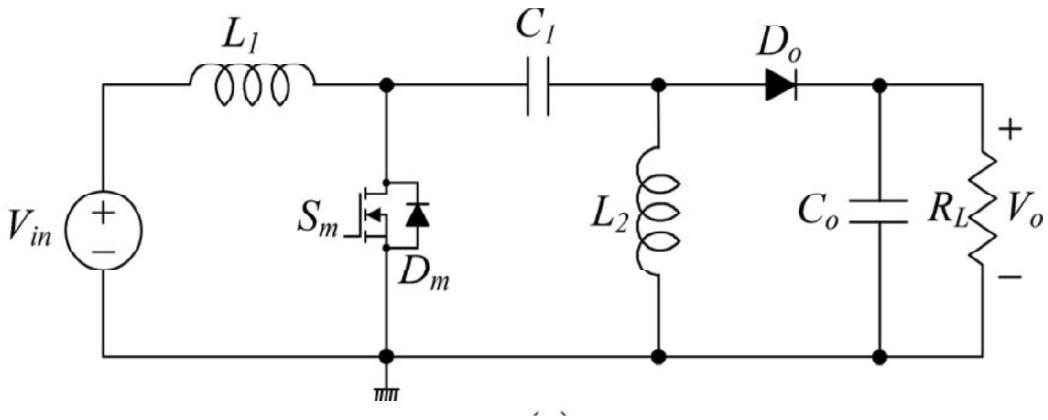

Figure 1.1: Conventional SEPIC converter

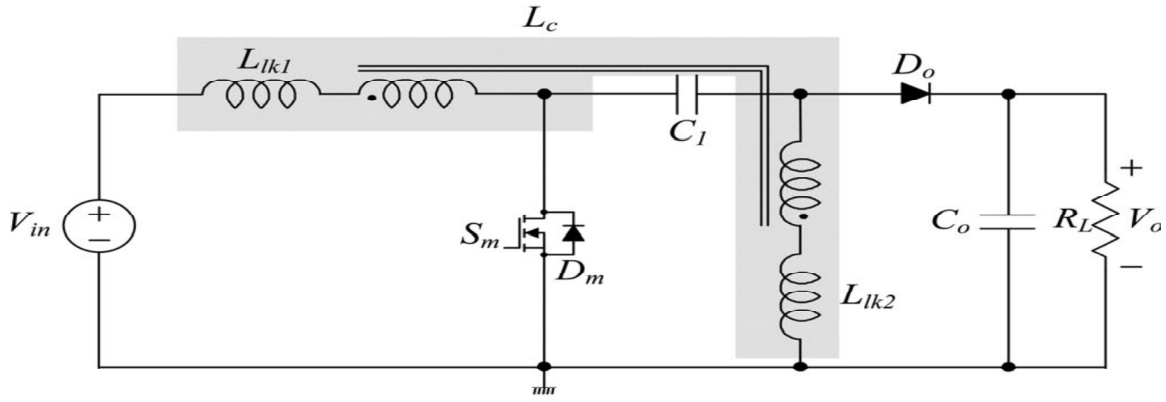

Figure 1.2: Ripple-free SEPIC converter with a loosely coupled inductor

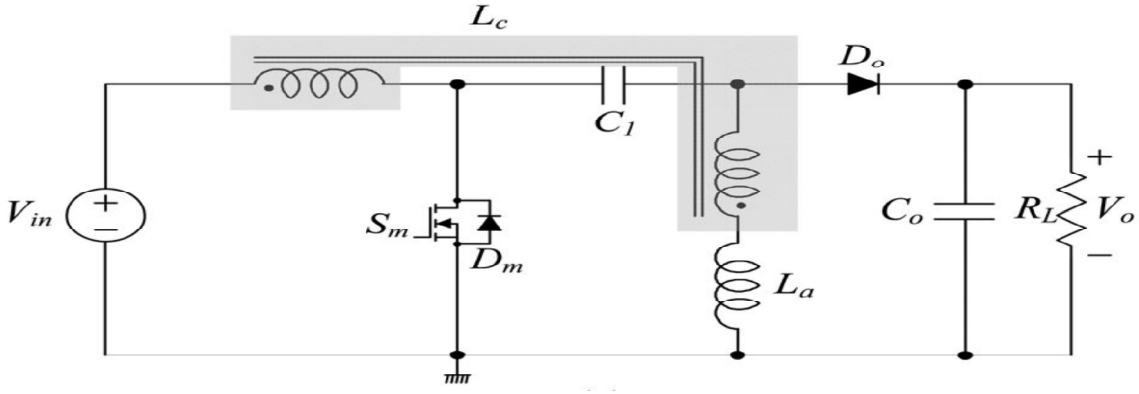

Figure 1.3: Ripple-free SEPIC converter with a tightly coupled inductor

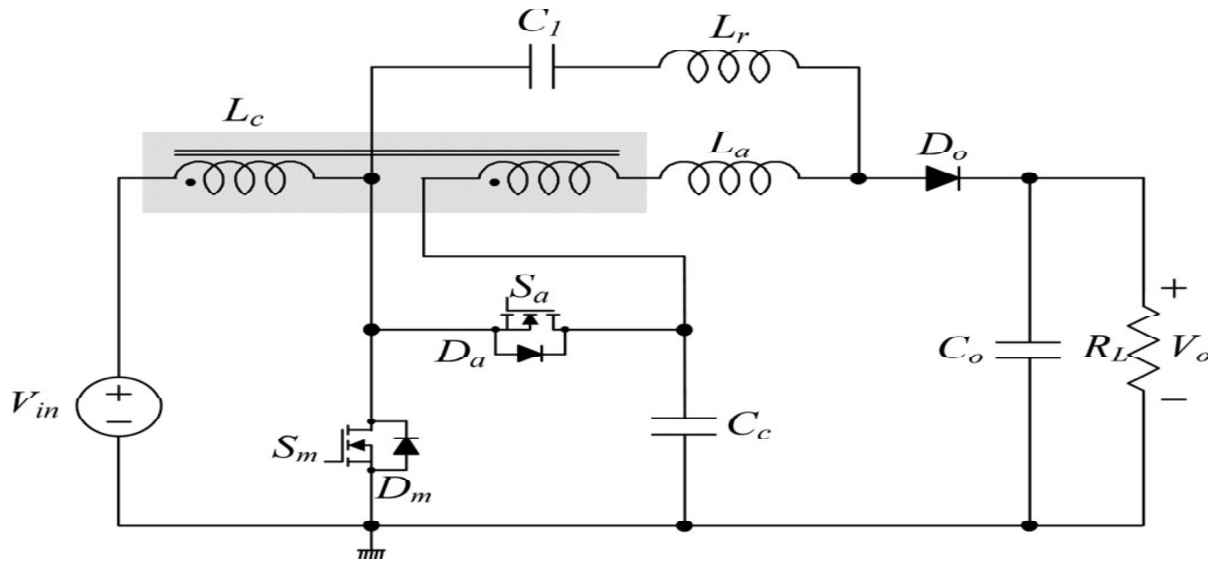

Figure 1.4: Soft-switching ripple-free SEPIC converter

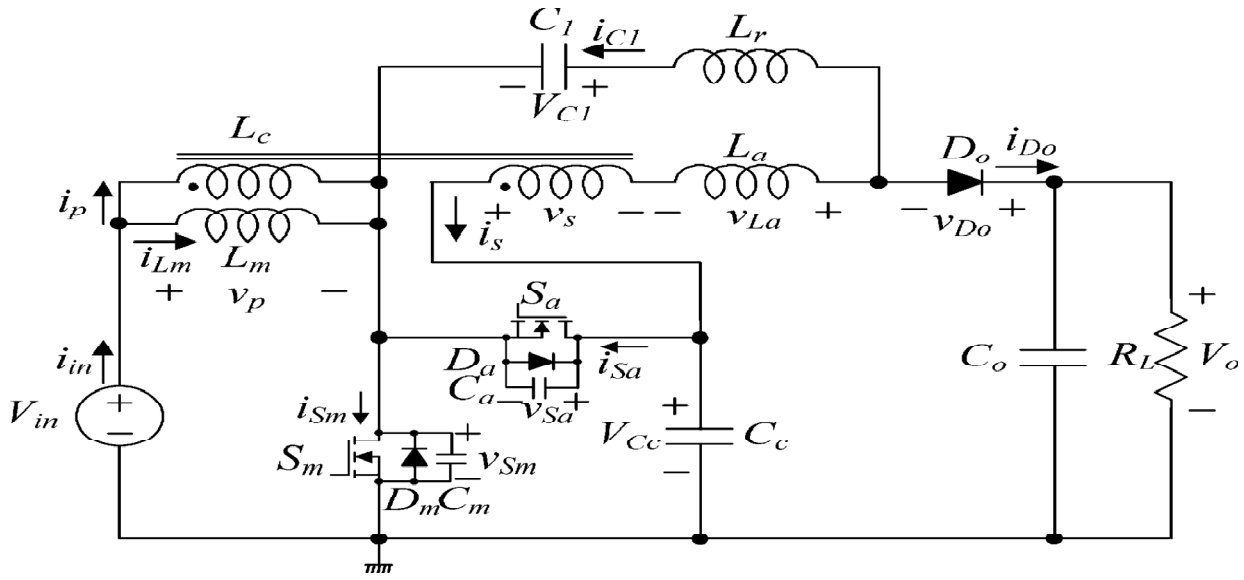

Figure 1.5: Equivalent circuit of the SEPIC converter

2.1 Modes of Operation

The circuit operation is divided into three modes and are as follows:

2.1.1. Mode I

In this mode, the switch S_m is turned on. The current through L_c and L_m increases linearly and the energy is stored in them. The current through C_1, L_r and C_o charges the capacitor C_o. When the current reaches zero, the diode D_o gets turned off.

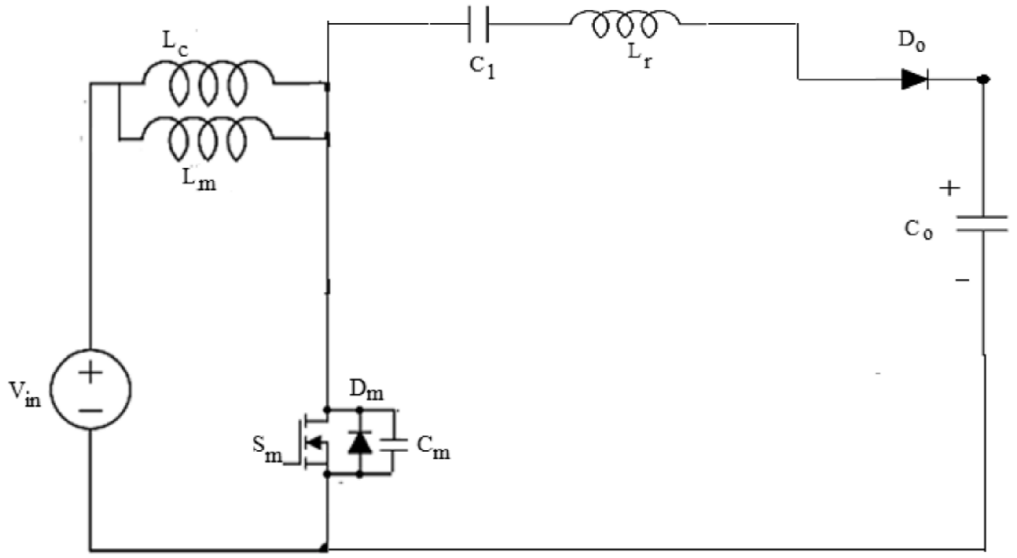

Figure 2.1: Mode I

2.1.2. Mode II

The switch S_m is turned off and the switch S_a is turned on. The energy in the inductor L_c is transferred to the capacitor C_c.

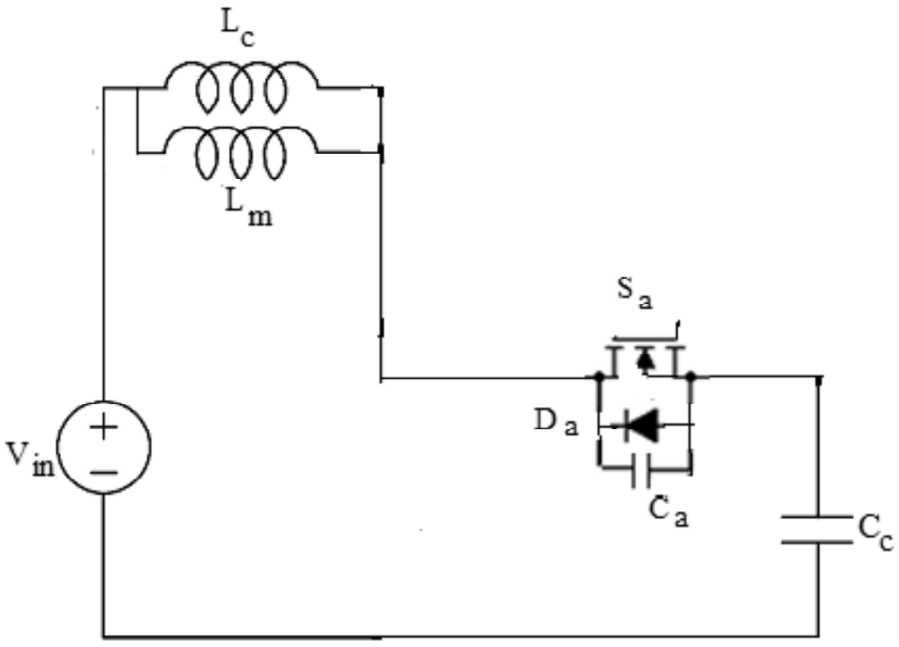

Figure 2.2: Mode II

2.1.3. Mode III

In this mode, both the switches are turned off. The energy stored in the capacitor C_o drives current through the load. The voltage across C_o decreases exponentially.

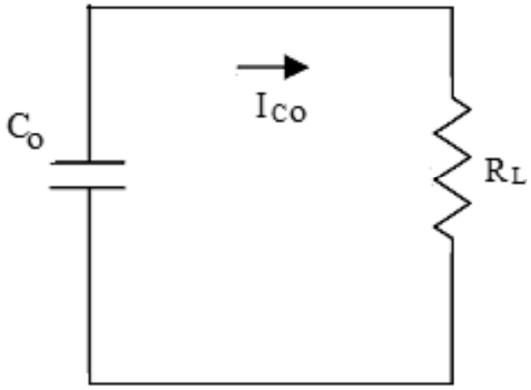

Figure 2.3: Mode III

3. SIMULATION RESULTS

3.1. Open Loop Controlled System

Open loop controlled SEPIC converter system is designed, modeled and simulated using the elements available in simulink. The open loop controlled SEPIC converter system is shown in Fig. 3.1. A step change in input voltage is applied as shown in Fig. 3.2.The input voltage increases from 48 to 54 volts. The output voltage of the SEPIC converter is shown in Fig. 3.3. The output voltage also increases from 200V to 220V. The output current and output power are shown in Fig. 3.4 and 3.5 respectively. The parameters used for simulation are listed in Table 1.

Table 1
Parameters used for simulation

Parameters	*Value*
L	1.3µH
L_1	35µH
C	10nF
C_1	6µF
C_2	50µF
R_L	500 ohms

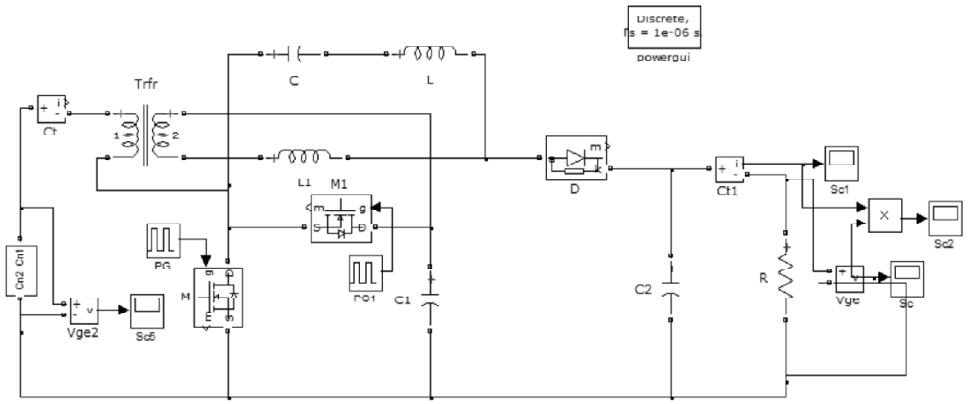

Figure 3.1: Simulink diagram of open loop system

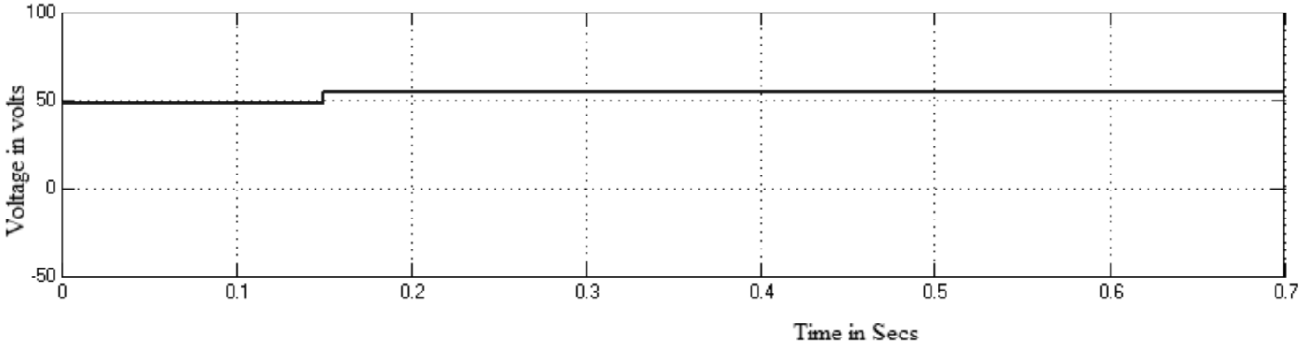

Figure 3.2: Input voltage

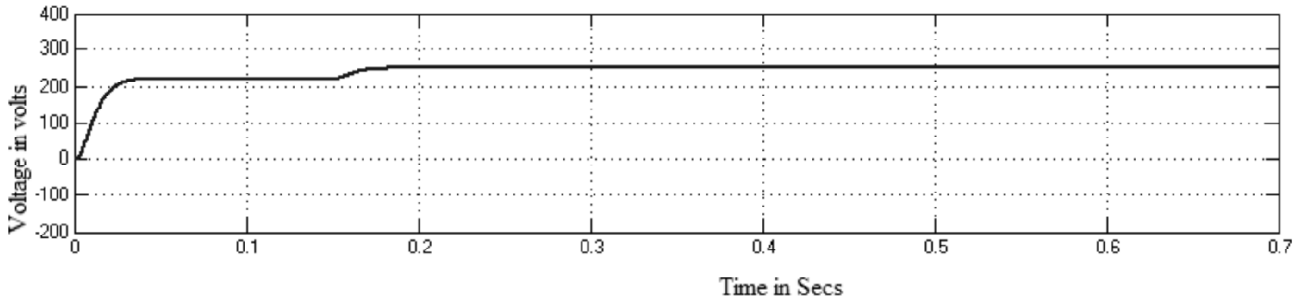

Figure 3.3: Output voltage

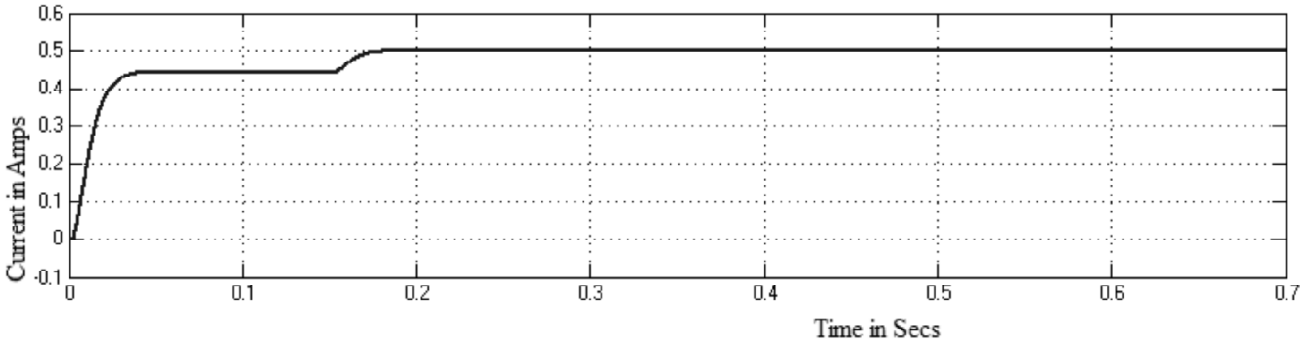

Figure 3.4: Output current

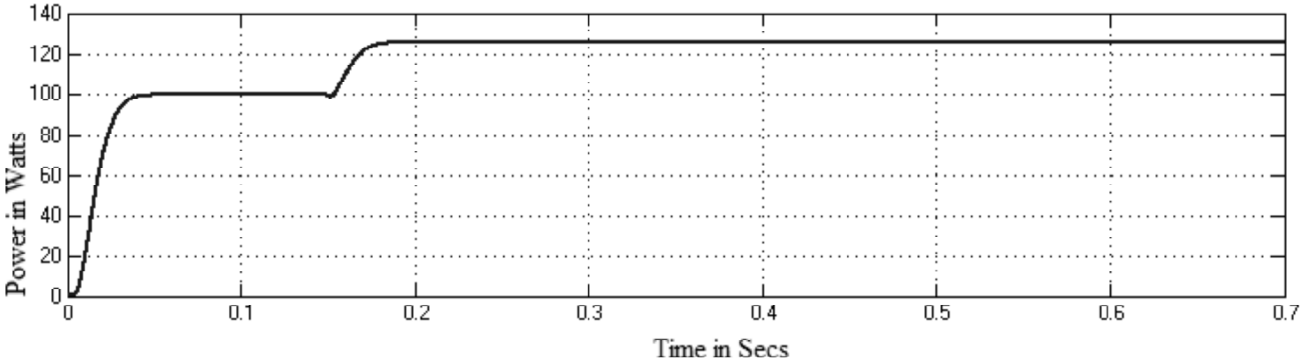

Figure 3.5: Output power

4. CLOSED LOOP PI AND PID CONTROLLED SYSTEMS

4.1. Step Change in Voltage

Closed loop PI controlled system is shown in Fig. 4.1.The load voltage is sensed and it is compared with the reference voltage of 200V. The error is applied to a PI controller. The output of PI controller is compared with the time base voltage to generate an updated pulse. When the load voltage increases, the error increases and pulse width of the control system gets reduced. Therefore, the output voltage gets corrected. The input voltage, output voltage, output current and output power are shown in Fig. 4.2, 4.3, 4.4 and 4.5 respectively. It can be seen that the output voltage, current and power reaches steady state value. The closed loop PID controlled system is shown in Fig. 4.6. The input voltage, output voltage, output current and output power with PID controller are shown in Fig. 4.7, 4.8, 4.9 and 4.10 respectively. The output voltage quickly reaches steady state value.

The summary of PI and PID controlled systems with voltage sag and swell in input voltage is given in Table 2. The rise time, settling time, peak voltage and steady state error are very much reduced by using the PID controller. The settling time is reduced to 0.33 seconds and steady state error is reduced to 0.9 by replacing PI with PID controller.

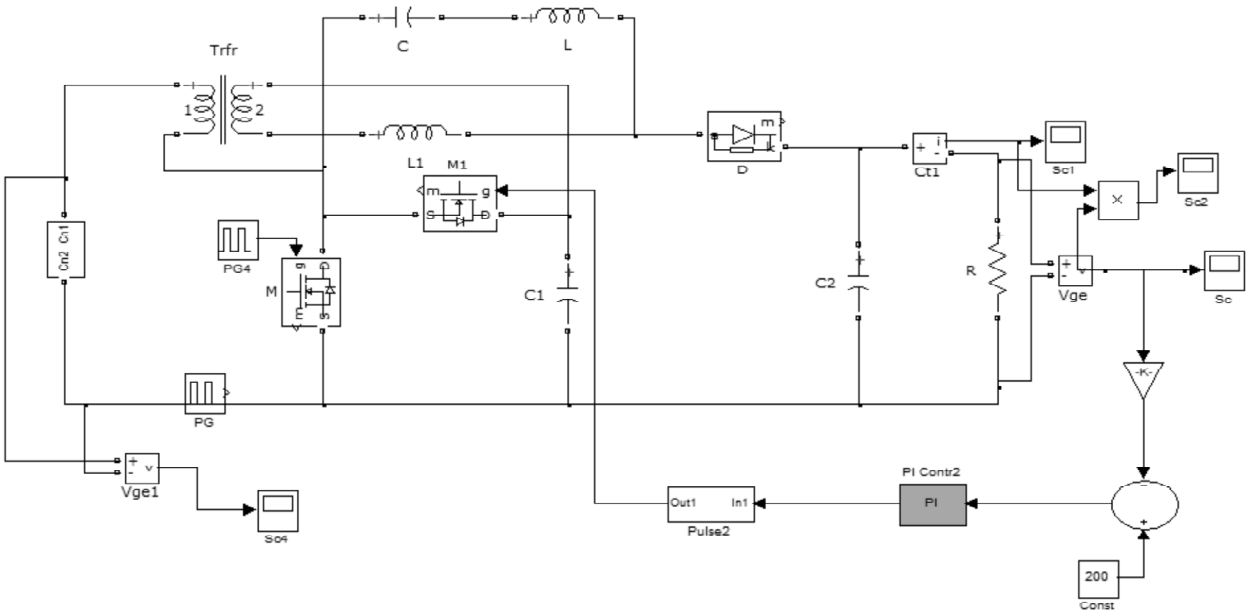

Figure 4.1: Closed loop PI controller

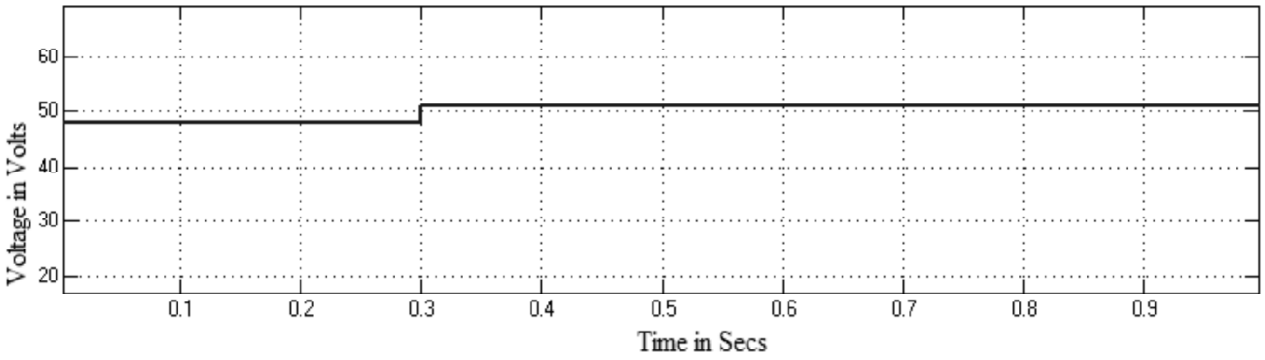

Figure 4.2: Input voltage with PI controller

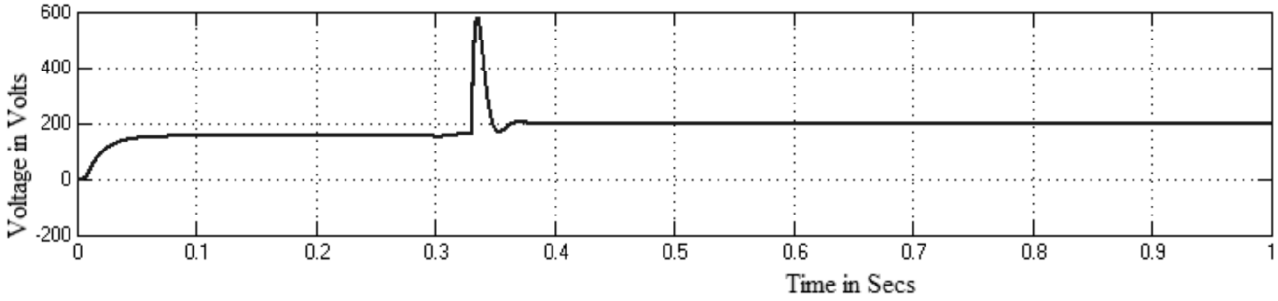

Figure 4.3: Output voltage with PI controller

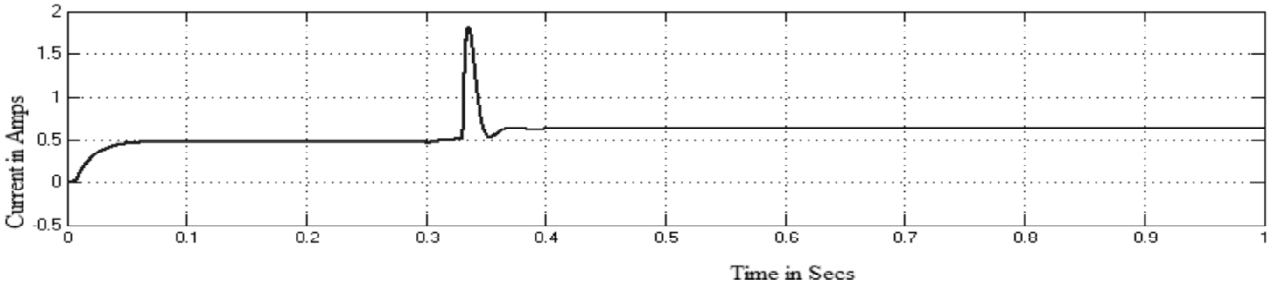

Figure 4.4: Output current with PI controller

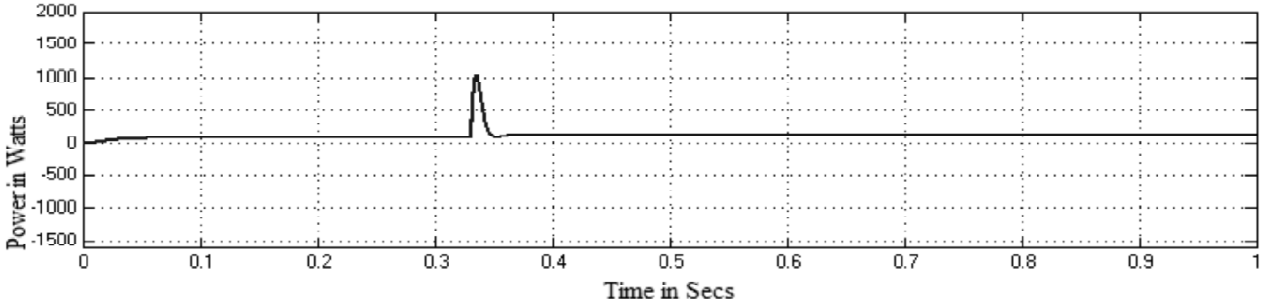

Figure 4.5: Output power with PI controller

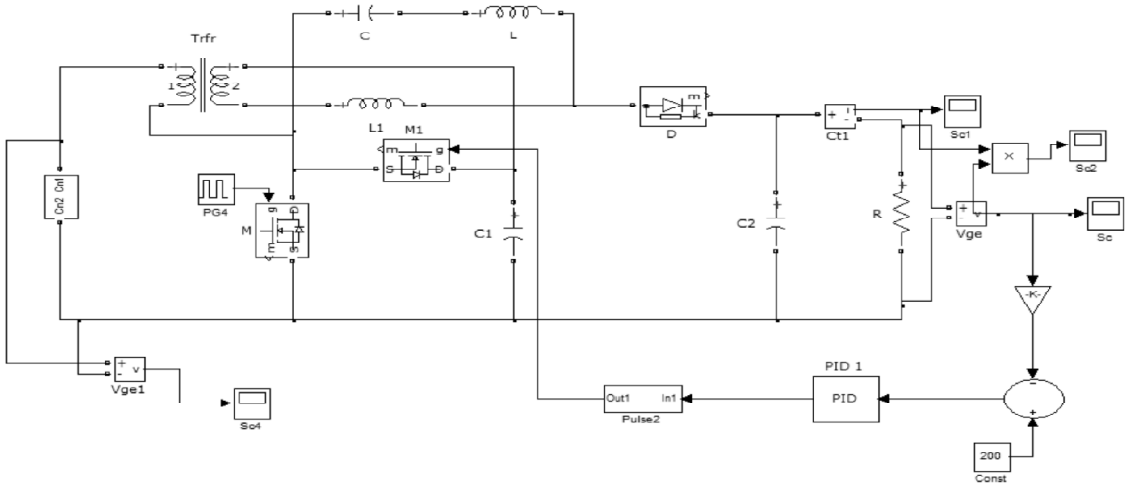

Figure 4.6: Closed loop with PID controller

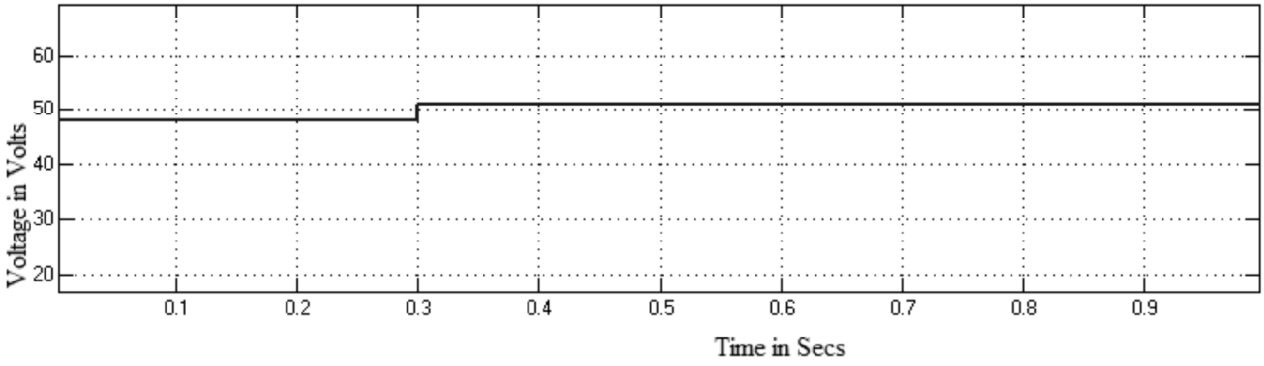

Figure 4.7: Input voltage with PID controller

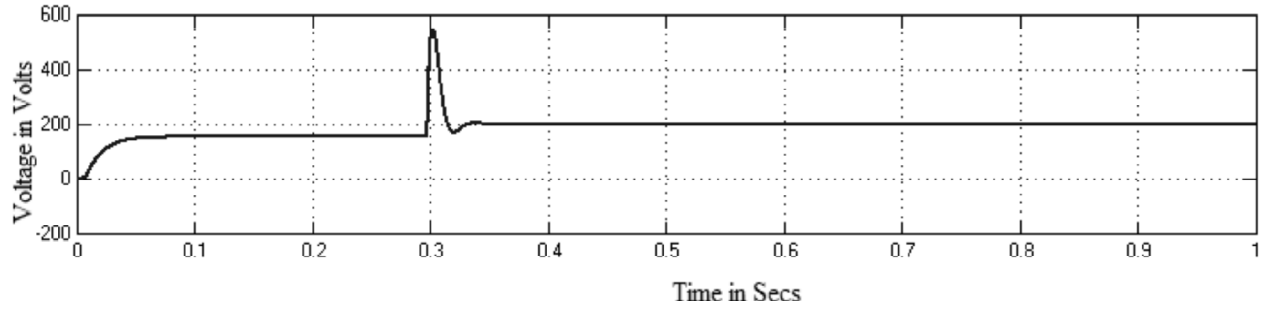

Figure 4.8: Output voltage with PID controller

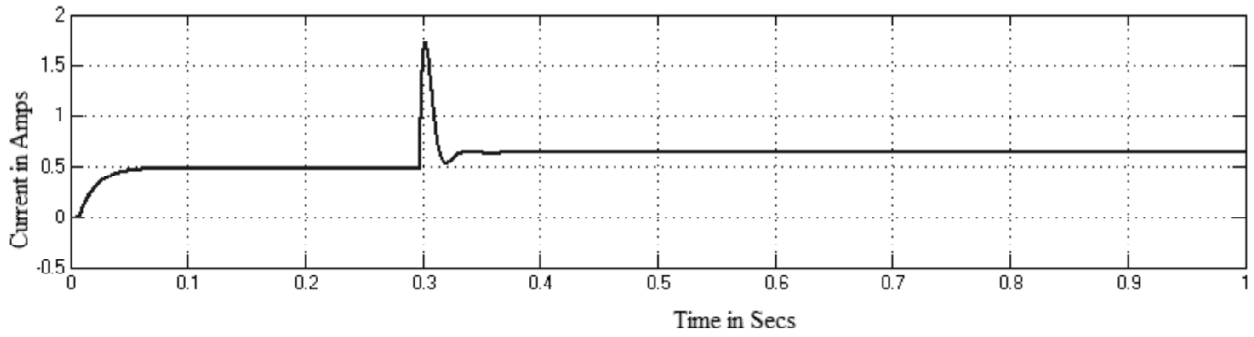

Figure 4.9: Output current with PID controller

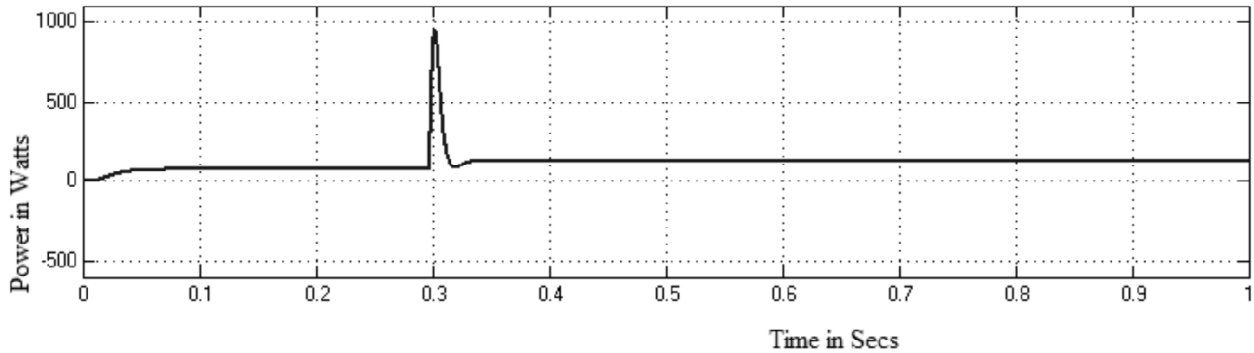

Figure 4.10: Output power with PID controller

Table 2
Time domain parameters with step rise voltage

Controller	T_r	T_s	T_p	E_{ss}
PI controller	0.31	0.38	0.32	1.3
PID controller	0.30	0.33	0.31	0.9

4.2. Step Fall and Rise in Input Voltage

The closed loop simulation study is done with fall and rise in input voltage as shown in Fig. 4.11.The corresponding response of output voltage is shown in Fig. 4.12. It can be seen that the output voltage reaches the set value. Simulation is done with multiple disturbances with PID controller as shown in Fig. 4.13. The corresponding output is shown in fig 4.14. The summary of time domain parameters with fall and rise in input voltage is given in Table 3. The response of PID controller is faster than PI controller which can be observed from Table 3. The settling time is reduced to 0.15 seconds and steady state error to 0.9.

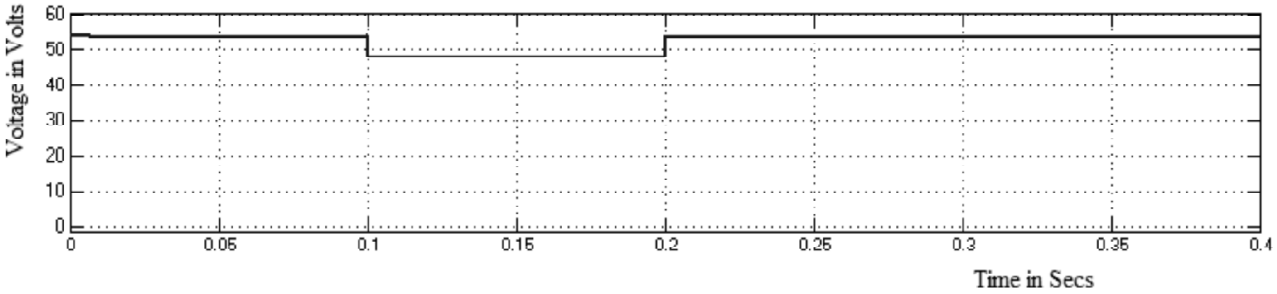

Figure 4.11: Input voltage with step fall and rise using PI controller

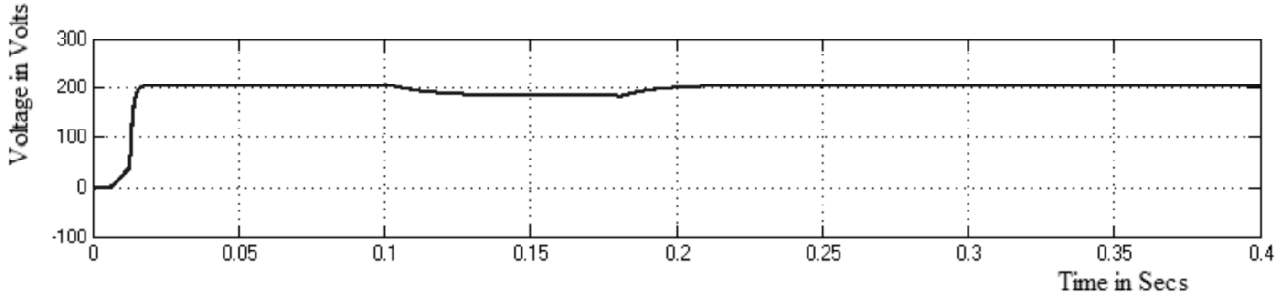

Figure 4.12: Output voltage with PI controller

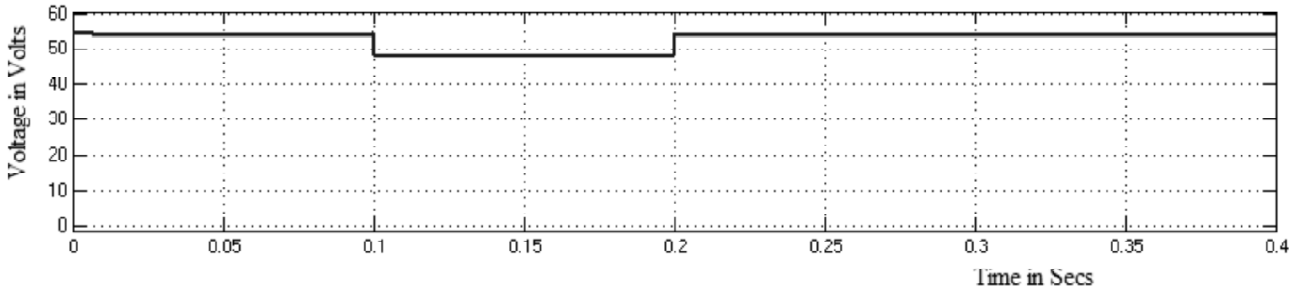

Figure 4.13: Input voltage with PID controller

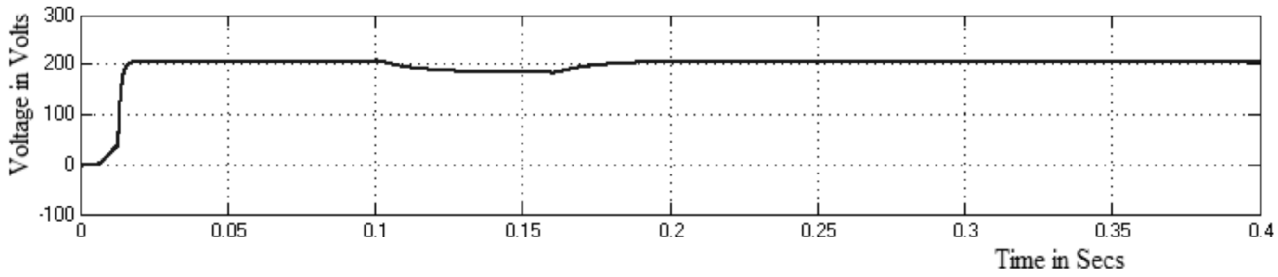

Figure 4.14: Output voltage with PID controller

Table 3
Summary of time domain parameters with fall and rise in input voltage

Controller	T_r	T_s	T_p	E_{ss}
PI controller	0.04	0.2	0.18	1.7
PID controller	0.03	0.15	0.16	0.9

4.3. Step Rise and Fall in Input Voltage

The simulation is also done with step rise and step fall in input voltage as shown in Fig. 4.15. The corresponding closed loop response for output voltage with PI controller is shown in Fig. 4.16. The above simulation is also done with PID controller. The input voltage with PID controlled system is shown in Fig. 4.17. The output voltage with PID is shown in Fig 4.18. Summary of time domain parameters with rise and fall in input voltage is given in Table 4. The settling time is 0.15 seconds and steady state error is 0.8.

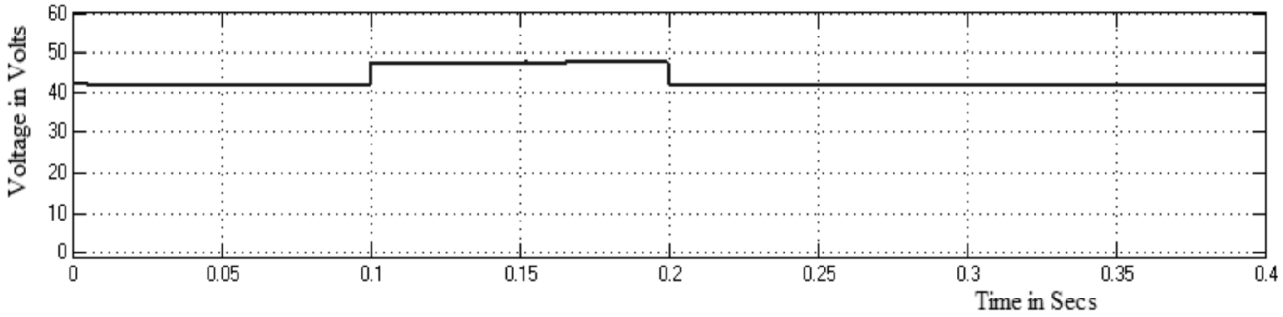

Figure 4.15: Input voltage with step rise and step fall

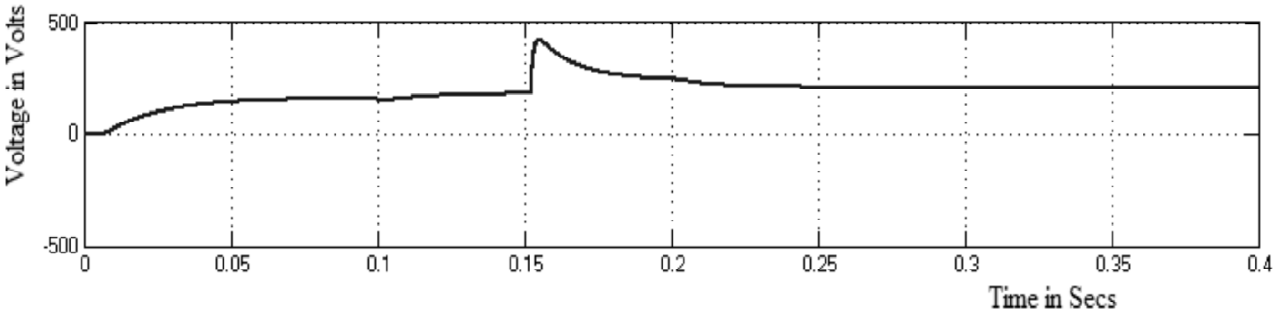

Figure 4.16: Output voltage with PI controller

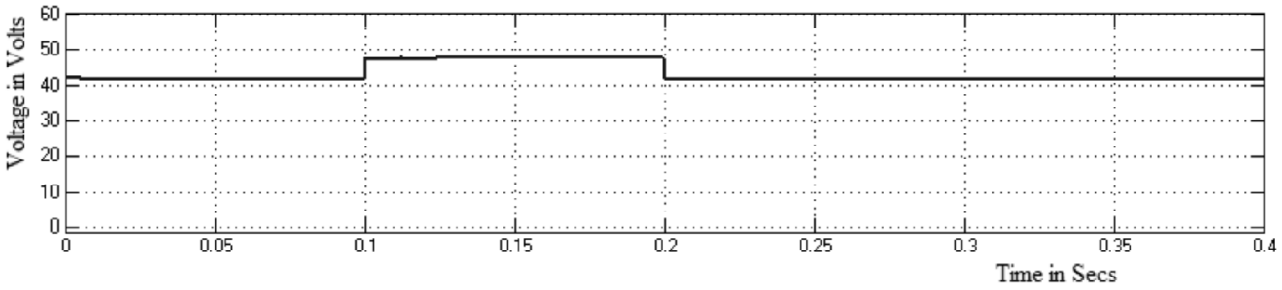

Figure 4.17: Input voltage with PID controller

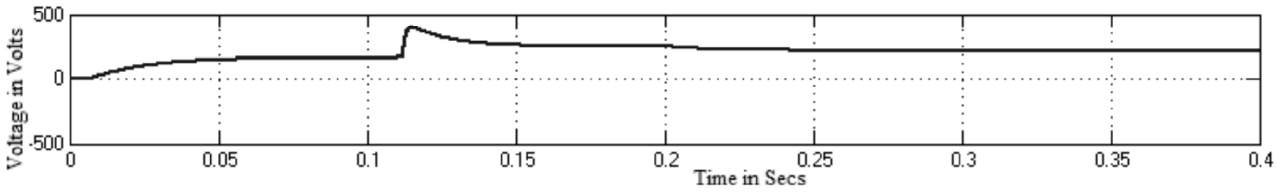

Figure 4.18: Output voltage with PID controller

Table 4
Summary of time domain parameters with rise and fall in input voltage

Controller	T_r	T_s	T_p	E_{ss}
PI controller	0.05	0.2	0.16	1.4
PID controller	0.04	0.15	0.13	0.8

5. CONCLUSION

The closed loop controlled SEPIC converter is designed, modeled and simulated successfully by using MATLAB. The results of closed loop system with PI and PID controllers with different types of disturbances are presented in this paper. This work has reviewed the performance of CLSEPIC system with step rise and step fall in input voltage. The results indicate that the response of the PID controlled system is superior to that of the PI controlled system. Simulation and numerical results have been presented with supporting comparisons. The results obtained in this paper are clear examples of improvement in dynamic response of CLSEPIC system. The advantages of the closed loop system are reduced setting time, and steady state error. The disadvantages of the converter is that it requires an additional switch, a coupled inductor and a capacitor. FLC or Hysteretic control can be used to increase the range of controllability.

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