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Improved SRAM Cell using Fin-FET in Terms of Power and Stability

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ABSTRACT

This paper includes a 6-T fully differential SRAM cell using Fin-FET to obtain stronger data stability and lower power consumption. The P-Type Transistors are used for data access and transmission gates are used to force new data into the cell during write operation. In Isodata stability the proposed design consumes 44% less power as compared to 6T SRAM cell designed by CMOS technology.

Keywords: Fin-FET; SRAM; Differential; transmission gates.

I. INTRODUCTION

Memory banks in modern high performance Microprocessors consists of a large number of transistors so the power consumption of the whole circuitry is very high . To reduce power consumption Dynamic Voltage scaling is used in modern microprocessors[2]-[4]. For this process performance of SRAM cell or memory bank is compromised. Smaller device or lesser gate length of CMOS device can further degrades the stability of the SRAM cell.

Technology circuit coding is widely used for mitigating the transistor sizing requirement in Fin-FET based memory circuits [2], [5]-[7]. A multioriented 6F (6 Fin-FET) SRAM cell is proposed in [8] however the complex layout makes the designing process challenging.

To achieve an independent controlled gate Fin-FET the top gate of the Fin-FET has to be selectively removed, which makes the fabrication process challenging. Asymmetrical gate work function Fin-FET is discussed in [2],[3] , but significant lower on current against symmetrical Fin-FET makes not negligible data access delay.

II. COMPARISON OF EXISTING FIN-FET SRAM CELL ARCHITECTURES

SRAM cells are described in this section, assuming a 90-nm Fin-FET technology. Cadence is used to characterize the SRAM cells. Quantum mechanical confinement, carrier– carrier scattering, surface scattering, carrier velocity saturation, field-dependent mobility, concentration-dependent mobility, and temperature-dependent mobility models are used in the simulation.

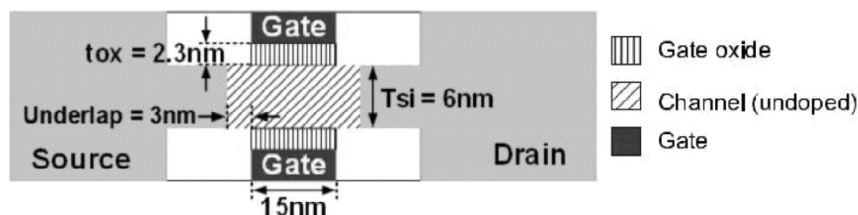

Figure: Cross-sectional view of the optimized Fin-FET-Tied

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SRAM cells are typically designed with tied-gate Fin-FETs (Fin-FETs-Tied) [1], [4]–[6], [16]. An Fin-FET-Tied that is used in memory design in this paper is shown in Fig. 1.

(A) Fin-FET structure

The continuous down in scaling of bulk CMOS creates major issues due to it base material and process technology limitations. The main drawback of CMOS based design is the leakage in small channel size; due to this the leakage stems increased from the lower oxide thickness, more substrate doping. The optimal performance of the device can be achieved by lowering the threshold voltage with low supply voltage worsen the leakage. The primary obstacles to the scaling of CMOS gate lengths to 22nm and beyond includes short channel effects, sub threshold leakage, gate-dielectric leakage and device to device variation reduction 3 which leads low yield. The International Technology Roadmap for Semiconductors (ITRS) predicts that double gate or multi-gate devices will be the perfect solution to obtain the device with reduced leakage problems and less channel length of the transistor. The FINFET based designs are known as double gate device which offers the better control over short channel effects, low leakage current and better yield in 22nm and beyond which helps to overcome the obstacles in scaling. When threshold voltage Vt is less than a potential voltage, gates of the double gate or FINFET device activates the currently flow between drain to source with modulating the channel from both the sides instead of one side. The potential which is applied to two gates together influence potential of the channel which fighting against the drain impact and leads to solve and give the better shut off to the channel current and reduces Drain Induced Barrier Lowering (DIBL) with improved swing of the design.

This FINFET based transistors offers good tradeoff for power as well offering interesting delay. The Figure 1 shows the 3D structure of multi-FIN based field effect transistors. The FINFET model structure consists of following regions:

1. Low doping silicon Fin
2. Highly doped Poly silicon region
3. Highly doped contact region between source and drain
4. Gate region- oxide (SiO2)

II. BASICS OF SRAM CELL

A typical SRAM cell is made up of six Fin-FETs. Each bit in an SRAM is stored on four transistors (P1, P2, N1, and M2) that form two cross-coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. Two additional access transistors serve to control the access to a storage cell during read and write operations. Since the cost of processing a silicon wafer is relatively fixed, using smaller cells and so packing more bits on one wafer reduces the cost per bit of memory.

Figure 2: Basic diagram for 6T SRAM cell

Access to the cell is enabled by the word line (WL in figure) which controls the 7 two access transistors N3 and N4 which, in turn, control whether the cell should be connected to the bit lines: BL-1 and BL-2. They are used to transfer data for both read and write operations. Although it is not strictly necessary to have two bit lines, both the signal and its inverse are typically provided in order to improve noise margin. The size of an SRAM with m address lines and n data lines is $2m$ words, or $2m \times n$ bits. The most common word size is 8 bits, meaning that a single byte can be read or written to each of $2m$ different words within the SRAM chip. Several common SRAM chips have 11 address lines (thus a capacity of $2m$ = 2,048 = 2k words) and an 8-bit word, so they are referred to as "2k × 8 SRAM".

(A) Operation of SRAM Cell

An SRAM cell has three different states. It can be in: standby (the circuit is idle), reading (the data has been requested) and writing (updating the contents). The SRAM to operate in read mode and write mode should have "readability" and "write stability" respectively. The three different states work as follows:

Standby: If the word line is not asserted, the access transistors N3 and N4 disconnect the cell from the bit lines. The two cross-coupled inverters formed by P1 – N2 will continue to reinforce each other as long as they are connected to the supply.

Read Operation**:** Basically, reading process requires only asserting the word line WL and reading the SRAM cell state by a single access transistor and bit line, e.g. BL. Nevertheless bit lines are relatively long with large parasitic capacitance. Therefore to speed-up reading, more complex process is used in practice: The read cycle is started by precharging by an external module both bit lines BL-1 and BL-2, i.e. driving the bit lines to a threshold voltage (midrange voltage between logical **1** and **0**). Then asserting the word line WL, enabling both the access transistors N3 and N4 which causes that the bit line BL-1 voltage either slightly drops (bottom N FinFET transistor N2 is ON and top PMOS transistor P2 is off) or rises. It should be noted that if BL-1 voltage rises, the BL-2 voltage drops, and vice versa. Then the BL-1 and BL-2 lines will have a small voltage difference between them while reaching a sense amplifier, which will sense which line has the higher voltage thus determining whether there was **1** stored or **0**. The higher the sensitivity of the sense amplifier, the faster the speed of the read operation. It is defined as the range of common mode input voltage up to which the transistors associated with the differential stage (first stage) are in saturation and gives a constant gain.

Write Operation: The start of a write cycle begins by applying the value to be written to the bit lines. If we wish to write a **0**, we would apply a **0** to the bit lines, i.e. setting BL-1 to **1** and BL-2 to **0**. This is similar to applying a reset pulse to an SRlatch, which causes the flip flop to change state. A **1** is written by inverting the values of the bit lines. WL is then asserted and the value that is to be stored is latched in. Note that the reason this works is that the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily override the previous state of the cross-coupled inverters. In practice, access NFinFET transistors N3 and N4 have to be stronger than either bottom N FinFET (N1, N2) or top PFinFET (P1, P2) transistors. This is easily obtained as PFinFET transistors are much weaker than NMOS when same sized. Consequently when one transistor pair is only slightly overridden by the write process, the opposite transistors pair gate voltage is also changed. This causes that M1 and M2 transistors can be easier overridden, and so on. Thus, cross-coupled inverters magnify the writing process.

III. THE CONVENTIONAL 6T SRAM CELL USING MOSFET

Here in this section we will discuss about conventional 6T SRAM cell. The conventional SRAM cell design is shown below:

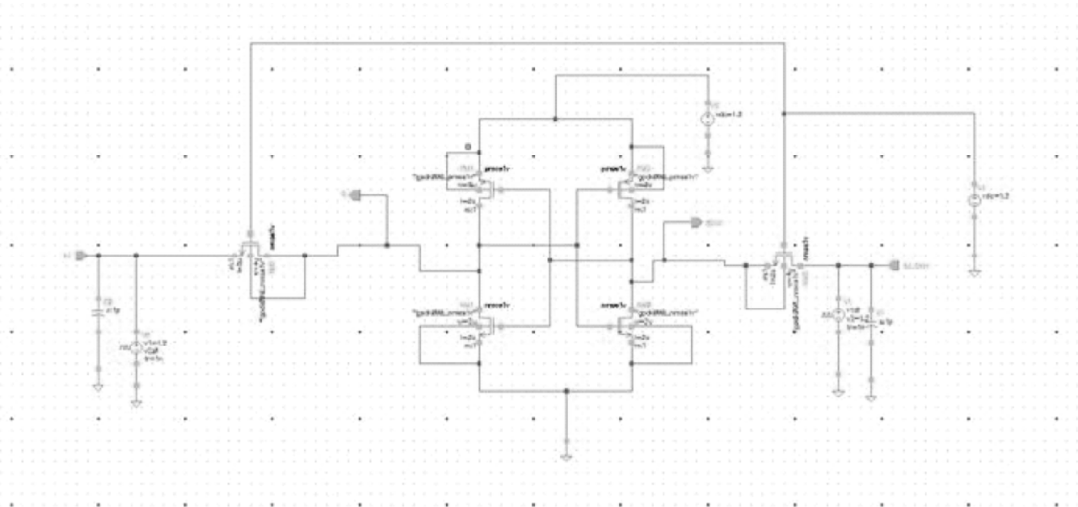

Figure 3.1: Diagram for 6T SRAM cell using static CMOS

Here in the above diagram both the P-type transistors are used as pull up transistor and two N-type transistors are discharge transistor. Two inverters are cross coupled to hold the data accessed by two access transistors. At the both end of the bit lines opposite Vpulse are used and Vdc is given to the cross coupled inverters. The driver transistors should be stronger than the access transistor to drive the node q. Here in the design driver transistors are thrice in width that of access transistor. The word line 10 high makes the NMOS conduct and connect the inverter inputs and outputs to two Vertical bit

lines. These inverters drive the current value stored inside the memory cell onto the bit line and inverted t0he value on the inverted bit line, this data generates the output value of the SRAM cell during a read operation. In writing operation, the strong bit lines are activated by input drivers to write the data into the memory. Depending on the current value there might be a short circuit condition and the value in SRAM is overwritten. The above mentioned of read and write operation for 1-bit 6T SRAM cell.

IV. PROPOSED DESIGN OF 6T SRAM CELL USING FINFET

To implement FinFET SRAM a new PTM (Predictive MOSFET model) is used. Predictive MOSFET model is critical for early circuit design research. In this work, a new generation of Predictive Technology Model (PTM) is developed, covering emerging physical effects and alternative structures. Based on physical models and early stage silicon data, PTM of bulk and double-gate devices are successfully generated.

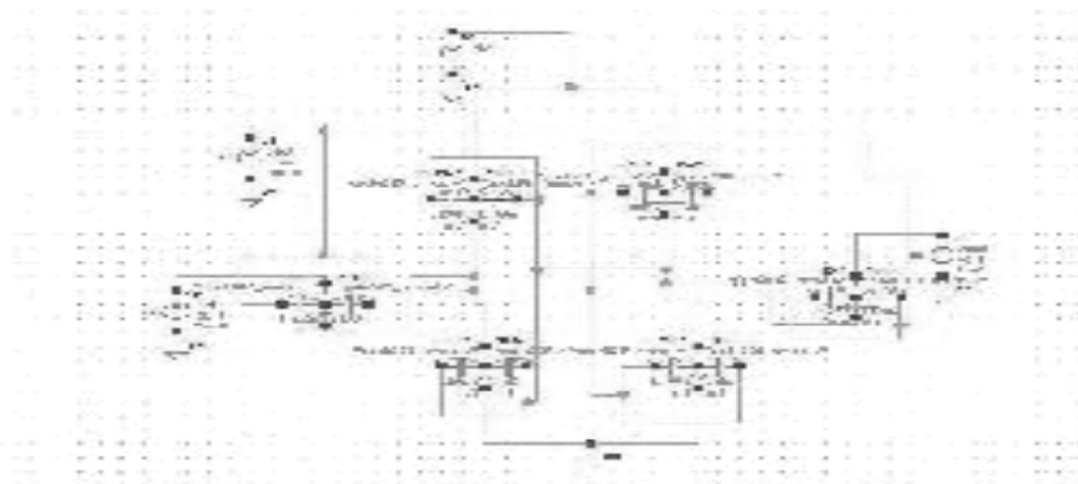

Figure 4.1: Diagram for 6T SRAM cell using FinFET

In the above design the Read Data stability increases than that of conventional 6T static CMOS SRAM cell. Power consumption of the whole circuit is also reduced by a good amount. FinFETs have emerged as the most suitable candidate for DGFET structure. Proper optimization of the FinFET devices is necessary for reducing leakage and improving stability in SRAM. The supply voltage (Vdd), Fin height (Hfin) and Vth optimization can be used for reducing leakage in FinFET SRAMs by increasing Fin-height which allows reduction in Vdd. However, reduction in Vdd has a strong negative impact on the cell stability under parametric variations. The device optimization technique for FinFETs to reduce standby leakage and improve stability in an SRAM cell is required.

V. SIMULATION RESULTS

A. Transient Response of 6T SRAM cell Using CMOS

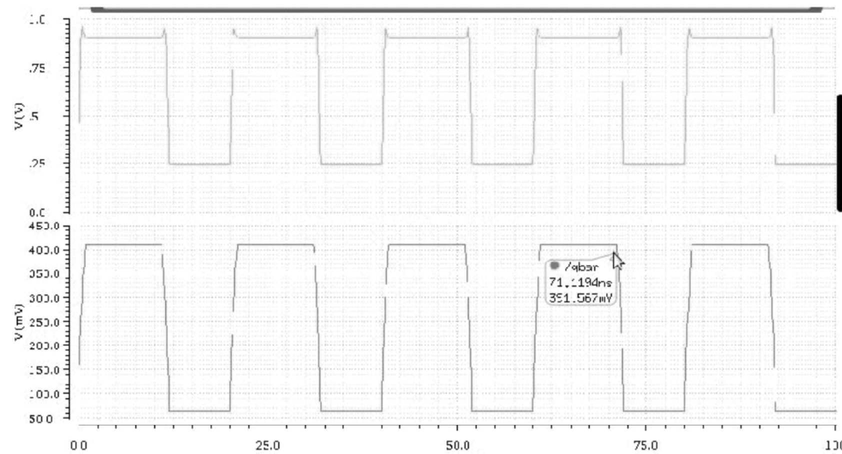

Figure 5.1: Transient response in read cycle for 6T SRAM cell using CMOS

Both the output q (red) and q_bar (green) is shown here as the transient response of the cell during the read operation. As we can see from the figure q hold its state in read cycle as there is no change in bit line in read operation. Bit_bar line discharge through the q_bar and the discharge transistor as the access transistor

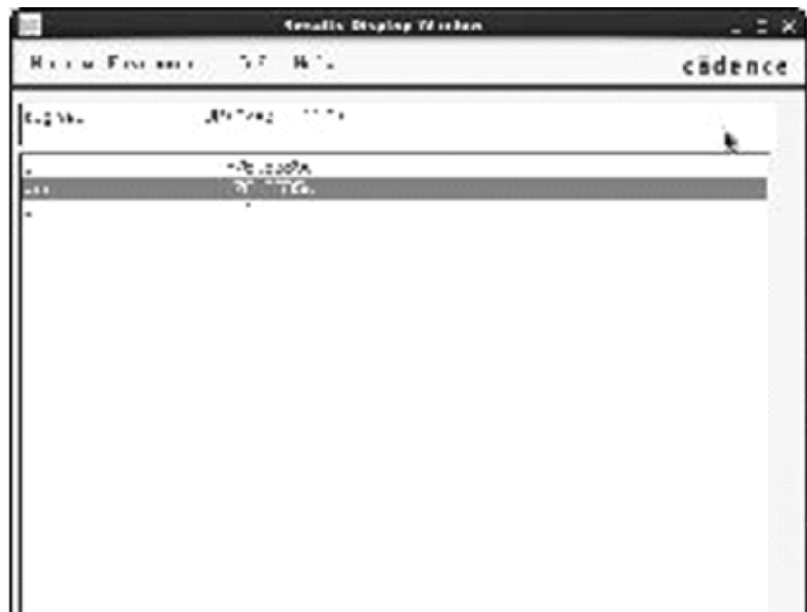

Figure 5.2: Power dissipation for 6T SRAM cell using CMOS

is on. In the result q_bar should stay in constant position for a stable read operation but here q_bar fluctuate a little to support current through the discharge transistor. For this reason often data loss phenomenon occurs. This situation can be avoided using FinFET technology. Power dissipation of the whole circuit also derived due to the 1v power supply to the SRAM cell.

VI. TRANSIENT RESPONSE OF 6T SRAM CELL USING FIN-FET

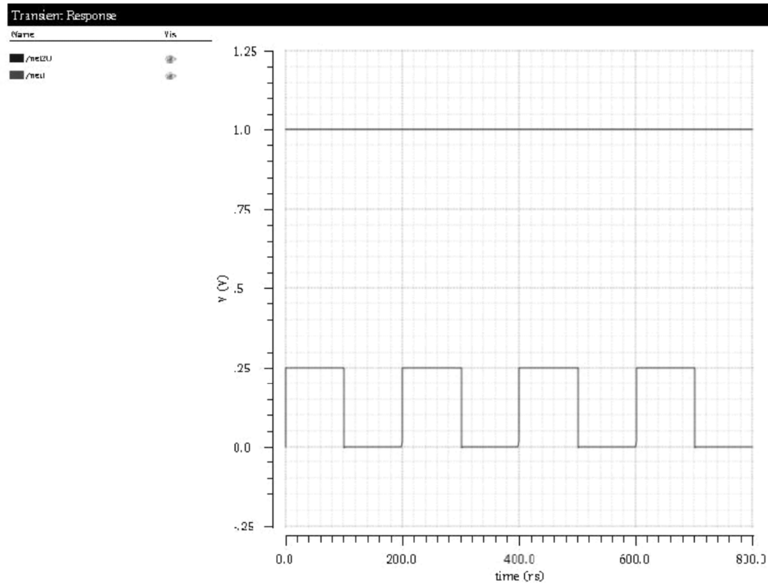

Figure 5.3: Transient response in read cycle for 6T SRAM cell using Fin-FET

The above fig shows the transient response for SRAM cell using Fin-FET is shown. As discussed earlier q_bar of the circuit is stable and q obeys the bit line. The Read data stability of the circuit is increased and no cross over condition occurs in the cell. Power consumption of the cell is also improves as we can see in the figure bellow for 1v power supply,

Figure 5.3: Power Dissipation for 6T SRAM cell using Fin-FET

VII. CONCLUSION

In this work I analyzed, that the Fin-FET based SRAM cell provides better read stability as well as less power dissipation. The comparison is shown bellow for 90nm technology.

TYPE	*PARAMETERS*		
CELL TYPE	*READ STABILITY*	*POWER*	*CURRENT*
6T SRAM CMOS	READ CYCLE IS NOT STABLE	76.9uW	76uAmp
6T SRAM Fin-FET	BOTH CYCLE ARE STABLE	51.1nW	51nAmp

The most important feature of the FinFET based SRAM cell is that there is no cross over conditions for SRAM read cycle so there is no data loss also, That makes the SRAM sell is more efficient

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