IJCTA, 9(10), 2016, pp. 4393-4399

Evaluation of Partially Connected Mesh Topology and Shared Queues Router Architecture for Network on Chip

***Chythanya.k **K. Somasundaram**

Abstract : Due to unremitting scaling down of CMOS technology, huge number of mixed devices is integrated on a chip. For the efficient communication between these devices routers are employed. Buffers are placed on either the input or in the output ports of a Network on Chip router. If a contention occurs in the output physical channel then input port holds the packet temporarily.During a traffic trace only 40% of the buffers are active and rest are left inactive. Power budgets and area requirements of buffers are high. This leads to the motivation for designing a router architecture with shared queues (RoSHAQ). RoSHAQ improves the buffer utilization by sharing of multiple buffers between different ports. In this paper, we projects a 3 dimensional Partial Mesh of Grid topology (PMG)and we use RoSHAQfor our design. We synthesises our topology using Network Simulator-2 tool. Experimental result concludes that PMG has improved performance in terms of latency, throughput and area in comparison with other topologies.

Keywords : Network on-chip, Router architecture with Shared-Queues, 3D partial Mesh of Grid Topology.

1. INTRODUCTION

During 90's communication between IP cores in SoC is was with the help of buses and point to point interconnects. System buses are used to interconnect many IP cores in a SoC. But due to some limitations of system buses such as, data transmissions and bandwidth, therefore it cannot meet all requirements of current system on chip [9]-[10]. Crossbar wasanother method to overcome few limitations of conventional buses.ButIt was only half way solution and it is not ultimately scalable one. Later, a dedicated point to point links are considered for SoC. They are favourable in terms of latency, power usage and bandwidth availability. But thecount of links will exponentially increases with increases in the count of cores. Thus the area and routing problem develops. To overcome these issues, Network on Chip (NoC) is proposed.NoC is a communication sub device on an integrated circuit, typically between IP cores in a SoC. There are 4 main components in a NoC, namely, cores, links, router and network adapters. Routers are the back bone for communication in Network on Chip. Every router will have at least five I/O ports, which depends on the router design. NoC has large number of data links interconnected by switches (routers). Several links are required to transmit messages from source core to destination core, by building switching decisions at the routers[2]-[6]-[7]. Modern telecommunication networks and Network on Chip are similar; both of them use multiplexed links for data transmission. There are several routing techniques proposed in the literatures. Wormhole routing improves the router performance. Information is transferred in the form of packets. The message signal will be divided into head flit, body flit, tail flit and then transmit. The packet mode of transmission will help reduce the buffer size. Reduction of buffer size will help to reduce power dissipation. These buffers can be

* Department of Electronics and Communication Engineering Amrita School of Engineering, Coimbatore Amrita VishwaVidyapeetham, Amrita University, India.

** Department of Mathematics Amrita School of Engineering,Coimbatore Amrita VishwaVidyapeetham, Amrita Unviersity, India. chythanyacalicut@gmail.com; s_sundaram@cb.amrita.edu

single queue or multiple queues. Generally buffers will utilise significant portion of router area and power budgets. In practical, all buffers will not contain the incoming data for the simultaneous transmissions. Also, most of the times, only 40% of buffers size is used and remaining 60% will be unutilized. This motivates to design router architecture with shared queue[1]. A Hamiltonian connected recursive topology and a routing algorithm for minimizing the congestion is shown [11]. Different types of topologies help the interconnection of IP cores for various applications. The drawbacks of communication over 2 dimensional NoCs are overcomed by the employment of 3 dimensional NoCs. Third dimensional NoCs has increased bandwidth, packet density and reduced power utilization. In 3 dimensional systems, Through-Silicon-Via (TSV) technology is utilised for communication. In [12], the authors were shown a 3D NoC architecture, specifically 3 dimensional Recursive Network Topology (3D RNT); we evaluate its performance using an analytical model and compare with 3D Flat Mess Topology (FMT).

2. TYPES OF ROUTERS

Different router architectures were proposed based on the number of buffers. For example, if the buffer in the router is single queue it is known as Wormhole (WH) router and if it has many queues in parallel it is known as Virtual-Channel (VC) router[8].A WH router having four pipeline stages, and this contain only one buffer and an input port for simple view. The flit reaches at the input port will go through four main pipeline stages and reached to output port is the working principle behind wormhole router as shown in fig.1.There are some disadvantages in this design. This head of the queue blocking problem is overcome in the Virtual Channel (VC) router. Stalling of packets occurs due to two reasons, they are: one is when switching allocator fails to grant signal or when input queue of the down router is fully packed.

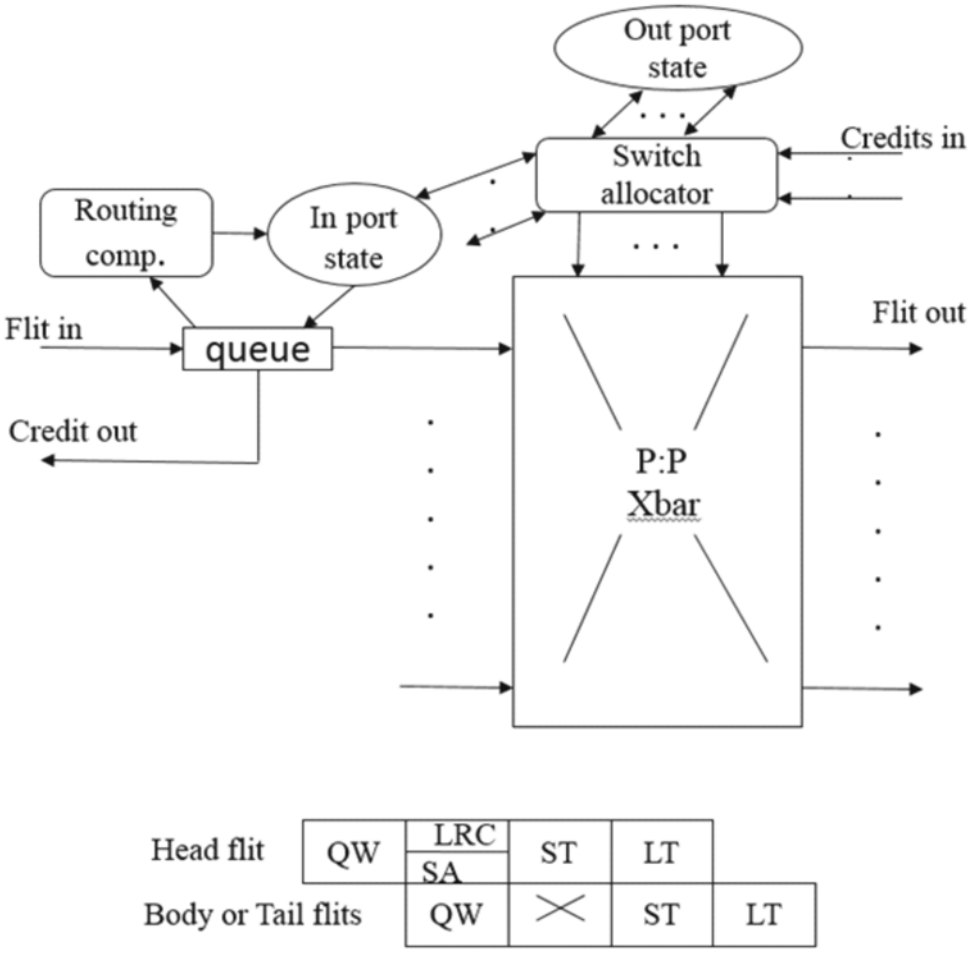

Fig. 1.

Four-stage WH router. QW- Queue Write, LRC-look ahead route computation, SA- switch allocator function, ST- switch traversal operation, LT-output link traversal or link crossing, (X)- pipeline bubble, P- number of input and output router ports.

In virtual channel router, an input or output port has several queues or buffers in parallel. Each one of them known as VC, which permits the temporarily storage of the packets from different queues and reduce the occurrence of packet stalling[1]-[2]-[3].

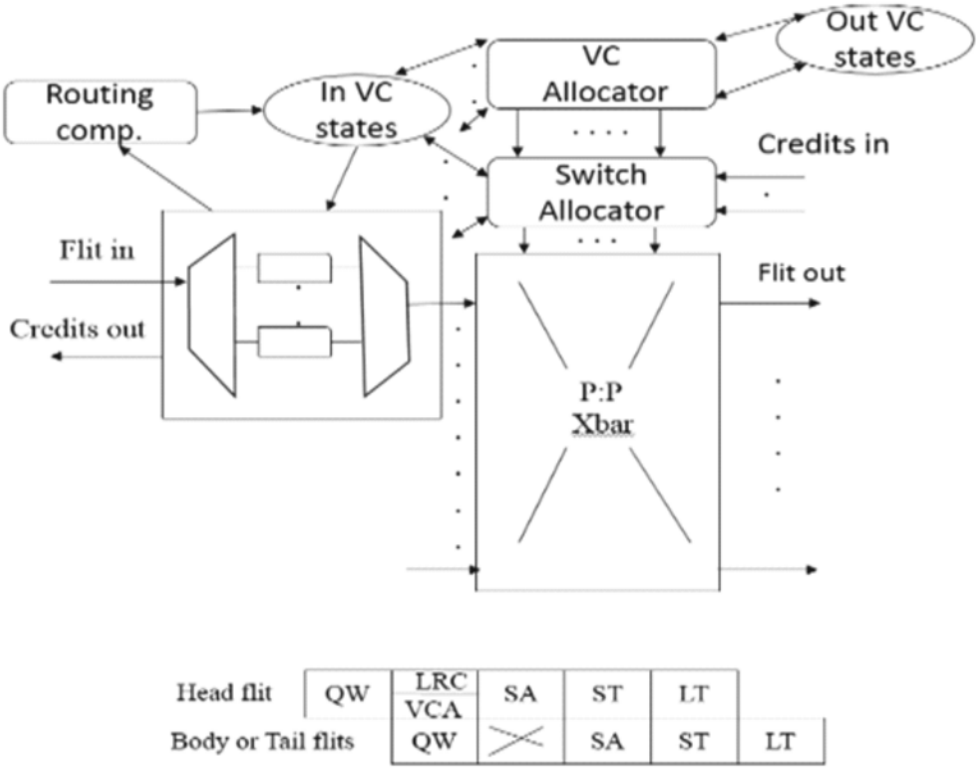

Fig. 2.

Five-stage Virtual Channel routers, QW- Queue Write, LRC-look ahead route computation, VCA- virtual channel allocation by virtual channel allocator, SA- switch allocation function, ST- switch traversal operation, LT-output link traversal or link crossing, (X)- pipeline bubble P- number of input and output router ports

The packet which reaches at the input port will go through five main pipeline stages and will reach output port as shown in figure 2. Even though VC router attains higherthroughput over WH router, it has higher latency due to deeper pipeline.VC also has some disadvantages. For example, if queues present at the input port fails to get SA then the packet get blocked or if all other output Virtual Channel queues are already full.

During a traffic trace not all buffers will have incoming packets to traverse the cross bar. Only 40% buffers will be in active state and 60% will be in idle state. Much money and space is spent for buffers and it is not utilised efficiently is the another disadvantage.

3. ROUTER ARCHITECTURE WITH SHARED QUEUES (ROSHAQ)

Even though the buffers are expensive and space consuming, they are not well used. All buffersin the input ports may not have packets for transferring. A few of their buffers will get packets most of the time while all others are regularly empty. Inactive queues have ability to share their storage capacity with queues of other input ports that are busy. Router architecture with shared queue overcomes this problem of virtual channel router and wormhole router shown in figure 3.First the packet will reach the input port this is called queue write or buffer write. After this packet will be send to both of the state modules. State modules generally will have main three function, first it will check whether the packet is head flit, body flit or tail flit, after this it will decide a particular output for this packets to traverse the cross bar and third is the grant signal generation. Statemodule_one will decide a shared queue for

the incoming packet and the state modules_two will decide a main output for the input packet to traverse the second crossbar. And the third function of this state modules are the generation andsending of request signal to shared queue allocator and output port allocator to indicate that there is a packet present in the input port.This request signal send by state module_one will go to the SQA(shared queue allocator) and this shared queue allocator will check whether the decided shared queue is empty or full. If it is empty it will send a grant signal back. At the same time state module_two will also send a request signal to the OPA(output port allocator) and then the output port allocator will check whether the requested output port is fill or empty if it is empty it will send a grant signal back to indicate that the packet present in the input port can traverse the cross bar. Sometimes both the OPA and SQA will send the grant signal at that same time then the priority will go to OPA and then the packet will traverse the second crossbar.

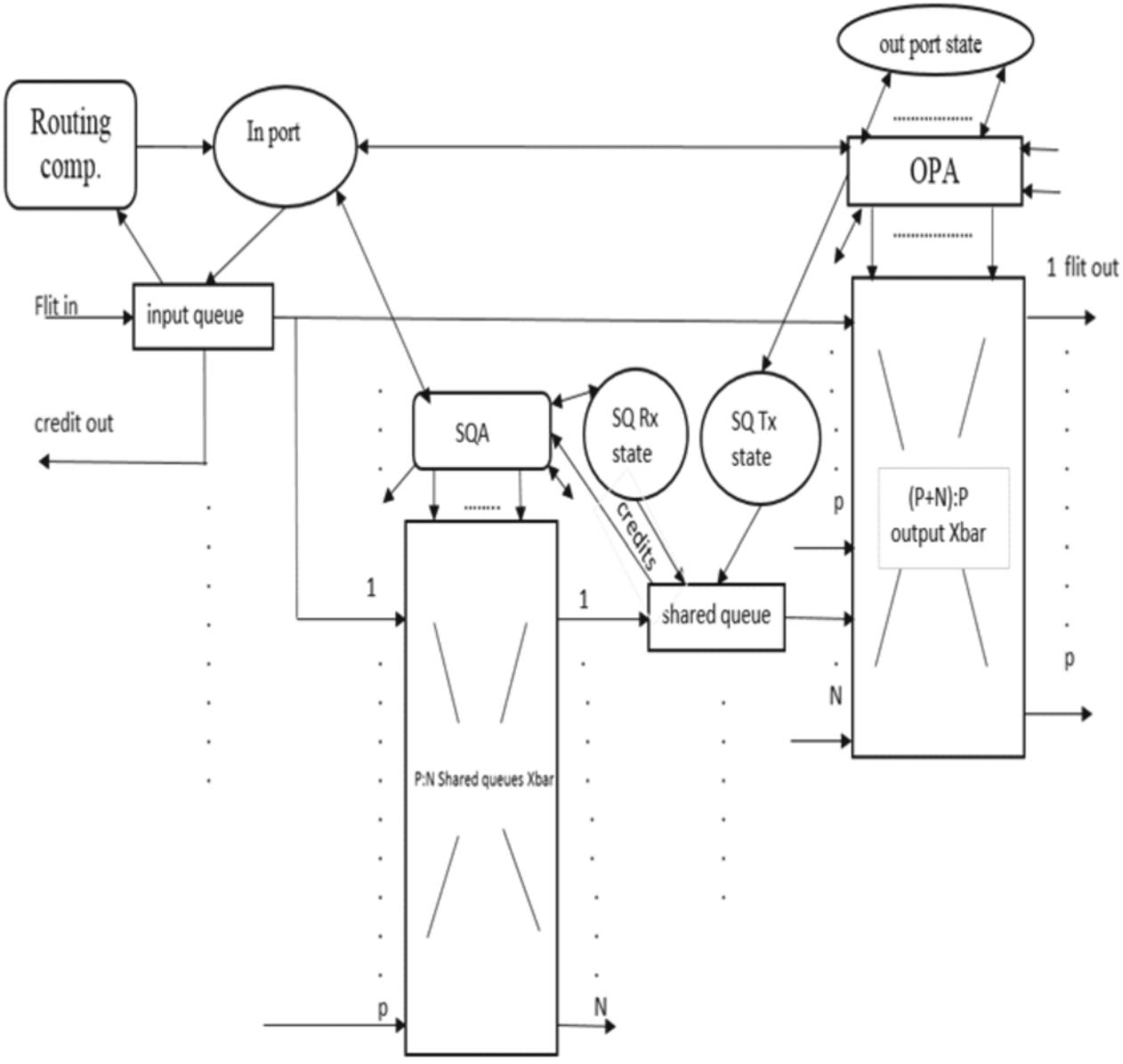

Fig. 3. RoSHAQ architecture.

Shared queue allocator will receive request from all the input queue and will give grant signal only if: 1) the shared queues are empty or 2) if more than one input ports is requesting for the same output port. This shared queue packet storing policy assurances deadlock-free for the networks. During light load condition packets usually avoid shared queues, then it works as a WH router. At heavy load conditions, the packets present at the input queues fails to receive grand from OPA, but can receive a grant signal from SQA and is then permitted to traverse

through the shared-queue crossbar, and in the next cycle it arbitrate for decided output port and would cross across the output crossbar and output channel. Visibly, in this instanceRoShaQ perform as an output-buffered router which is also act as deadlock-free.Generally 2D router will have 5 input and output ports, 4 will be connected to adjacent nodes and one is connected to the same IP core. Any 3D router has 7 input output ports, which include 2 extra ports for the adjacent.

4. 3D PARTIAL MESH OF GRID TOPOLOGY

The cost of network is mainly determined by the topology employed.An efficient topology could only manage area and power requirements of the network.In mesh of grid topology all nodes communicates with one another through links.In partial mesh of grid topology all nodes arranged in layers which are connected with the help of TSV[4]-[5].

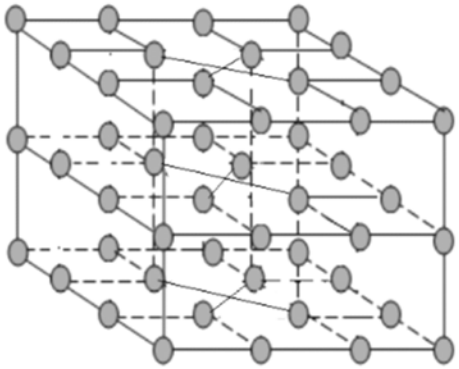

Fig. 4. 3 layer 4 × 4 partial mesh of grid.

The ultimate aim of designing PMOG topology is to reduce the number of interconnections when compared to MOG topology. It will reduce the complexity of the network.Due to this throughput is increased and power consumption is also less. A 3 × 4 × 4 PMOG topology is shown in figure 4.

5. DESIGNING OF PMOG

Mesh of Grid topology simulation is done using NS-2. In a MOG topology, entire nodes are interconnectedvia links. Increased Power and complexity are disadvantages of this design. The bandwidth of the link used here is 1 Mb and the propagation delay is 50ms. Different traffic patterns can be used to send messages from a source core to a destination core. Here, we have used CBR, i.e. constant bit rate. The agent considered here is User Datagram Protocol.

Similarly, for PMOG topology, we consideredpartially linked 48 nodes. Rest all parameters are same as that of MOG topology.

6. EXPERIMENTAL RESULTS

Table 1. shows the various parameters for the simulation of PMG topology. For PMG,throughput is 180.54 kbps and the latency is 0.478s when sending packets from node 0 tonode 41 with the bandwidth of the link being 1 Mb and the propagation of the link being 50ms. Using the tool NS-2, we obtain the packet loss percentage which is 4.1%. These results are tabulatedand compared with a Mesh of Grid topology. We observe that there is an improvement inpacket loss percentage and latency using PMG than MoG topology. Moreover, the throughputalso increases as the number of packets sent is more for a PMG in comparison with MoG.Area and power find out using Synopsys Design Compiler. Table: 2. shows the Analysis of the 3D router in our PMOG. We compare of RoSHAQ with VC router. The area requirement for the proposed work is82220.0 μm^2which is much lesser than other architecture. The power usage is also reduced in comparison to other router architecture. Fig.6 shows the output wave form of RoSHAQ**.**

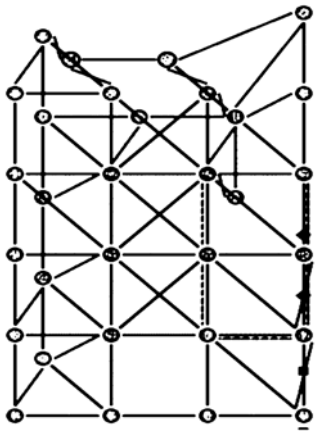

Fig. 5. Snapshot of the NS-2 Network Animator showing a PMOG

Table 1. NS-2 Synthesis Report

Topology	*MOG*	*PMOG*
Throughput (kbps)	72.09	180.54
Latency(s)	.1830s	.478s
No of packets send	2403	4134
No of packets loss	142	170
Packet loss in %	5.9	4.1

This observation conclude that the 3 dimensional partial mesh of grid has good performance than mesh of grid topology, and RoSHAQ has improved performance compared with Virtual Chanel router. RTL view of RoHAQ is shown in fig.7

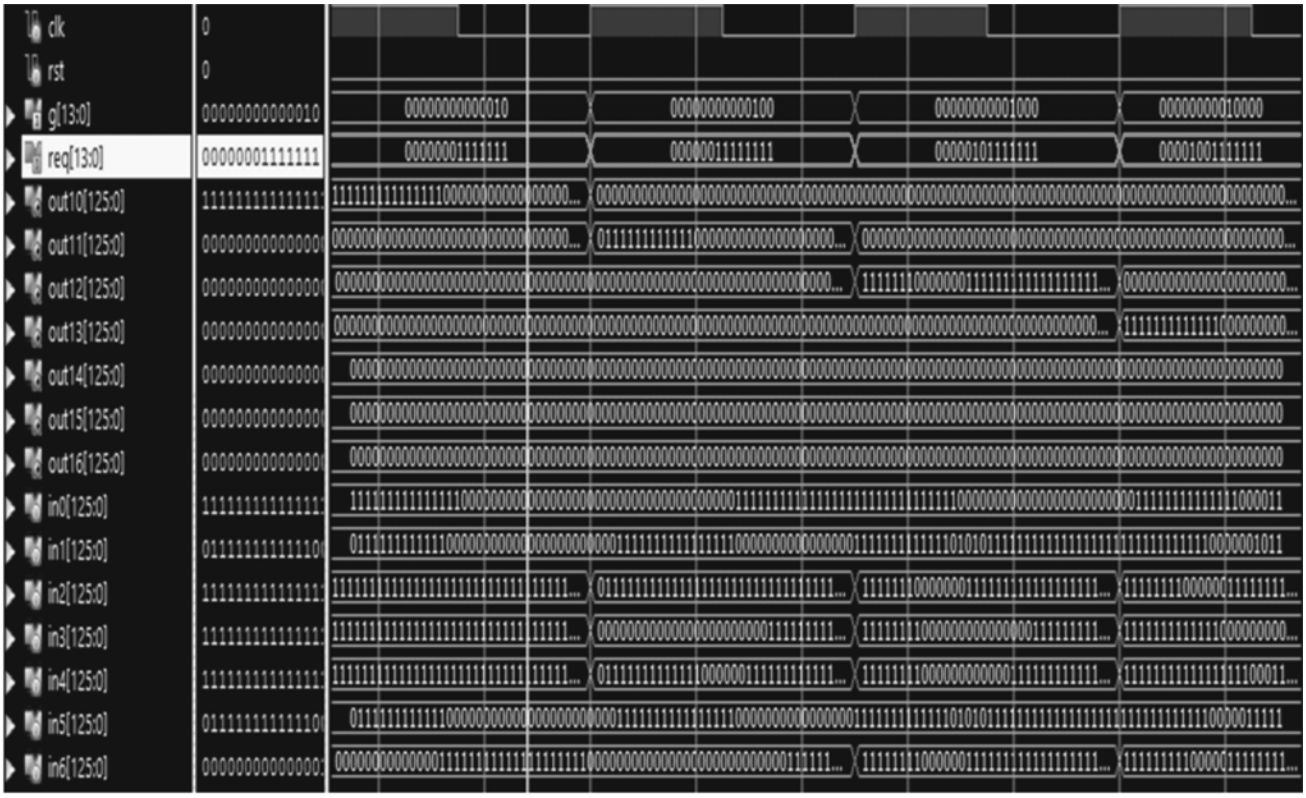

Fig. 6. Waveform of Virtual Channel Router.

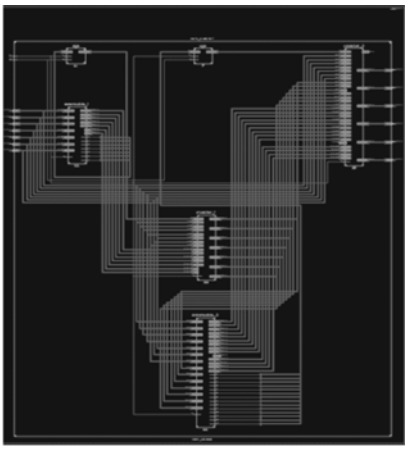

Fig. 7. RTL model for RoSHAQ.

7. CONCLUSION

In this paper, we proposed a 3D RoSHQrouter architecture and a Partial Mesh of Grid topology (PMG). We found that this architecture will greatly minimize the area and power constraints when compared to a virtual channel router. PMG topology enhances the overall throughput of the network when compared to a fully connected Mesh of Grid topology. The topology designed is dead- lock free. This PMG based NoC reduces the high chances of redundant connections. Because of the less number ofinterconnections it reduced the power consumption.

8. REFERENCES

1. Ann T. Tran,"Achieving High-Performance On-Chip Networks With Shared-Buffer Routers,"*IEEE Trans. on* Very Large Scale Integration(VLSI) System,Vol.22, No.6, june.2014
2. Anjali N.V, K. Somasundaram, "Design and Evaluation of Virtual Channel Router for Mesh-of-Grid based NoC," in *International Conference on Electronics and Communication System*,2014.
3. M. Modarressi, A. Tavakkol, and H. Sarbazi-Azad,"Virtual point-to point connections for NoCs ," *IEEE* Trans. Comput.-Aided Design Integr. Circuits Syst., Vol. 29, No. 6, pp. 855–868, 2010.
4. Kundu, Santanu, J.Soumya, and Santanu Chattopadhyay. "Design and evaluation of Mesh-of-Tree based Network-on-Chip using virtual channel router."[5] Y. Hoskote, S. Vangal, A. Singh, N. Borkar, and S. Borkar, "A 5-GHz mesh interconnect for a teraflops processor," *IEEE Micro*, Vol. 27, No. 5, pp. 51–61, 2007.
5. Y. Hoskote, S. Vangal, A. Singh, N. Borkar, and S. Borkar, "A 5-GHz mesh interconnect for ateraflops processor," *IEEE Micro*, Vol. 27, No. 5, pp. 51–61, 2007.
6. W. J. Dally and B. Towles, "Route packets, not wires: On-chip interconnection networks," in Proc. DAC, 2001, pp. 684–689.
7. Dally, William J. "Virtual-channel flow control." *IEEE Transactions onParallel and Distributed Systems*, Vol.3, No. 2, pp. 194-205, 1992.
8. L. M. Ni and P. K. McKinley, "A survey of wormhole routing techniques in direct networks," Computer, Vol. 26, No. 2, pp. 62–76, 1993.
9. P. Guerrier and A. Greiner, "A generic architecture for on-chip packet-switched interconnections" in DATE '00: *Proceedings of the Conference on Design, Au- tomation and Test in Europe*, pp. 250–256,2000.
10. S. Kumar, A. Jantsch, M. Millberg, J. Oberg, J. Soininen, M. Forsell, K.Tiensyria, and A. Hemani, "A network on chip architecture and design methodology," in ISVLSI '02: *Proceedings of the IEEE Computer Society Annual Symposium on VLSI*, pp. 117–122,2002.
11. K.Somasundaram,JuhaPlosila and N. Vishwanathan, "Deadlock free Routing Algorithm for Minimizing Congestion in a Hamiltonian Connected Recursive 3D NoCs", *Microelectronics Journal*, Vol.45, No.8, pp.989-1000, 2014.
12. N. Viswanathan, K. Paramasivam, and K. Somasundaram, "An Optimized 3D Topology for On-Chip Communications", *International Journal of Parallel, Emergent and Distributed Systems*, Vol.29, No.4, pp.346-362, 2014.