International Journal of Control Theory and Applications

ISSN : 0974-5572

Volume 10 • Number 28 • 2017

A Simple Control Algorithm for DSTATCOM Based on Improved Three-Phase SOGI-PLL under Grid Disturbances

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Abstract: This paper introduces a simple control algorithm based on three-phase Improved Dual Second Order Generalized Integrator based phase locked loop for the generation of reference source currents for DSTATCOM (Distribution Static Synchronous Compensator) even under grid disturbances. SOGI-PLL tracks the phase of a signal accurately even under grid disturbances. Therefore, in this controller, estimation of peak value of load currents and unit templates generation are done based on improved three-phase dual SOGI based quadrature signal generation (QSG) and PLL. This makes the controller simpler, effective and ease of implementation in real-time applications. The proposed algorithm for DSTATCOM is aiming to perform with dynamic compensation and low computational burden under distorted/step changes in load currents, presence of harmonics, unbalance and to provide good compensation even under grid harmonic conditions, magnitude variations, frequency variations. In this paper, Dual SOGI-PLL is adopted because of its dynamic performance, speed and tracking accuracy under all varying and distorted conditions. The effectiveness of the proposed controller is developed and tested using MATLAB/Simulink and the results found feasible and effective.

Keywords: Distribution Static Synchronous Compensator (DSTATCOM), Improved Second Order Generalized Integrator (ISOGI), Phase - Locked Loop (PLL) and Power Quality (PQ).

1. INTRODUCTION

The power generated by the conventional energy is decreasing day to day due to the depletion of resources such as coal, gas and oil etc. In the recent times, the development of non-conventional energy sources based Distributed Generation (DG) systems has fulfilled the shortage of fossil fuels. A variety of energy sources such as wind turbines, micro/pico hydro-turbines, photovoltaic arrays and battery energy storage systems are used in DG systems [1]. All these sources combine and form a DG and several such interconnections of DGs are forming as microgrids. Hence, a microgrid is a local grid comprising of several DG's with battery energy storage and various loads operating in grid connected mode or islanded mode in [2]. Various power quality issues are raised due to integration of RES to grid along with linear/nonlinear or power electronic based converter loads by [3]. In distribution systems, the application of non-linear loads such as variable speed drives, fluorescent lamps

and arc furnaces etc. are increasing widely and introducing harmonics and various other power quality issues into the distribution systems. The most common method of reducing harmonics and improving power factor in the system is by using passive filters. But, these are not preferred due to the drawbacks of fixed compensation, bulkiness and resonance by [4]. Therefore, Custom power devices (CPD's) such as DVR (Dynamic Voltage Restorer), DSTATCOM and UPQC (Unified PQ Conditioner) are more superior to passive filters and provide the best solution for power quality issues by [5].

The magnitude of the grid voltage varies because of non-linear loads such as variable frequency drives, large motors, reciprocating compressor and arc furnaces etc. The fundamental frequency of the grid voltage also varies because of the major loss of a generating station or tie line or major loads [6]-[7]. Due to these variations, the grid gets polluted. There are various standards which describes the characteristics of grid voltage. The Indian electricity grid code (2010) has specified a band of frequency range of 49.5 Hz to 50.2 Hz during 100% of time. Similarly, the IEC 61727 standard defines for a grid-tied PV system has a range of 49 Hz to 51 Hz and should be disconnected if the limits are exceeded. IEEE 1547 standard defines for a microgrid frequency range which should not exceed 0.1% while reconnecting to the grid. Standard C37.118.1 is defined for a P-Class PMU with a frequency range of 48-52 Hz and M-Class PMU of 45-55 Hz. The testing frequency for power quality measurement is defined in IEC standard 61000-4-30 of a frequency range of 42.5 Hz to 57.5 Hz for a standard 50 Hz system. PQ disturbances such as voltage flicker, swell, interruptions and sags are also defined in the IEEE 1159 and 1453 standards [8]-[12]. Therefore, an effective and robust computational technique is required to meet all the above mentioned standards including power quality analysis.

The aim of shunt active power filter is to compensate the harmonic current obtained by the non-linear loads. For effective control, fast and accurate tracking of fundamental and step changes in the current should be done. Therefore, a proper control strategy should be adopted and two such loops are identified. In the first loop, injected reference current should be calculated by extracting the currents and the second loop should guarantee the filter following the reference current adequately. Keeping accuracy and reliability in view, many PLL techniques are proposed in literature such as SRF-PLL, DDSRF-PLL, EPLL and SOGI-PLL [13]-[15]. Every PLL has its own advantages and disadvantages and SOGI-PLL has found satisfactory under distorted conditions and has low computational burden with only one control gain associated with it. SOGI-PLL has gained much attention in grid connected systems such as grid synchronization and further SOGI-Quadrature signal generation has further enhanced as SOGI-FLL for frequency estimation and for harmonic extraction MSOGI-PLL is used and for symmetrical component extraction [16]-[17]. Dual SOGI-PLL's are used and SOGI-PLL based control algorithm for shunt active power filter was developed [18]. But all these methods produce error if there is a presence of DC offset or inter-harmonics that are caused due to local loads. Therefore, an improved Dual SOGI-PLL was proposed to eliminate DC offset and unknown harmonic frequencies (Inter-Harmonics) present in the grid voltage signal [19].

In this paper, an improved Dual SOGI-QSG's are used for design and development of control algorithm for three-phase DSTATCOM and is implemented for harmonic mitigation, power factor correction, reactive power compensation, load balancing under unbalanced and linear/non-linear loads and under adverse grid conditions including DC offset. Three-phase PLL was designed using Improved SOGI and implemented for DSTATCOM application.

The proposed control structure has following advantages:

1. SOGI is capable of detecting the grid voltage/current under balanced and unbalanced conditions.
2. Higher ability to extract the fundamental components even under adverse grid conditions and its response is faster and accurate compared to conventional SOGI-PLL.

3. The performance of the PLL is not affected with the ripple frequency, Inter-harmonics, DC offset, distortions or noise and also robust w.r.t transient and steady state disturbances.

However, the Improved Dual SOGI-PLL implementation for a three-phase DSTATCOM is reported in this paper. Various tests are carried out to test the functionality using MATLAB/Simulink.

2. PROPOSED CONFIGURATION AND CONTROL ALGORITHM

The DSTATCOM shown in Figure 1 is a Three-leg VSC consisting of 6 IGBT switches. An interfacing inductor L_f is connected across the source and load at the PCC (Point of Common Coupling). There are several DG units (Distributed Generation) are connected to the local grid through the point of common coupling. Switching on and off of DG units are producing many variations in the grid voltages and currents supplied to the local loads. The proposed three-phase dual SOGI based control algorithm for DSTATCOM is capable of maintaining the THD % (Total Harmonic Distortion) within the IEEE 519-1992 limits. The proposed control algorithm is capable of handling Load balancing, power factor correction and harmonic compensation under adverse grid conditions. The ratings of the proposed system are listed in appendix. To test the dynamic performance under adverse grid and load conditions, Non-linear load (Steady and increase in load) and grid disturbances (sag, swell, unbalance, DC offset and harmonics) conditions are also tested.

The performance of the DSTATCOM depends on the value of DC bus capacitor. For reliable operation, the reference value of DC bus voltage should be 1.6 times more than the peak value of PCC voltage.

The proposed SOGI based controller mainly contains of peak amplitude extraction and reference source current generation using unit templates produced by the proposed PLL. Improved Dual SOGI-PLL is used to enhance the power quality under adverse grid conditions and distorted load conditions.

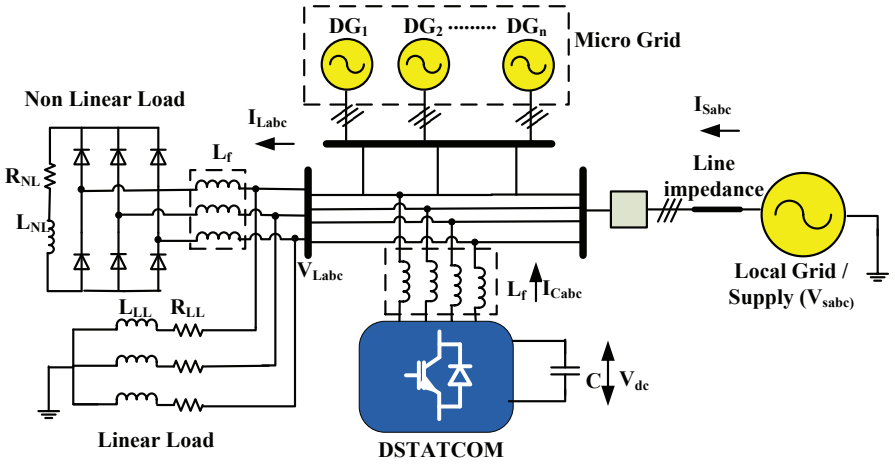

Figure 1: Line Diagram of the Proposed System

A. SOGI-PLL

This subsection introduces a basic SOGI functionality and its application in the proposed controller. If the grid voltage signal has distortions, harmonics and noise, then a filter is required to eliminate the effect in the phase tracking. The SOGI acts as an adaptive filter which generates orthogonal signals even under grid distortions. The block diagram of SOGI quadrature signal generation and PLL are shown in Figure 2 and 3 respectively. Proper tuning of K is required in such a way that the filtering response should be effective under distorted conditions. Where, K is called Damping Factors and chosen as 1.6.

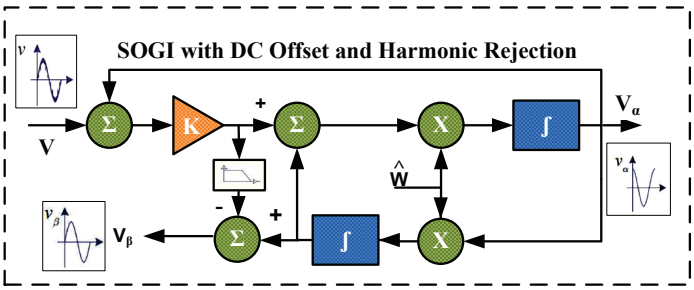

Figure 2: Improved SOGI-Quadrature Signal Generation

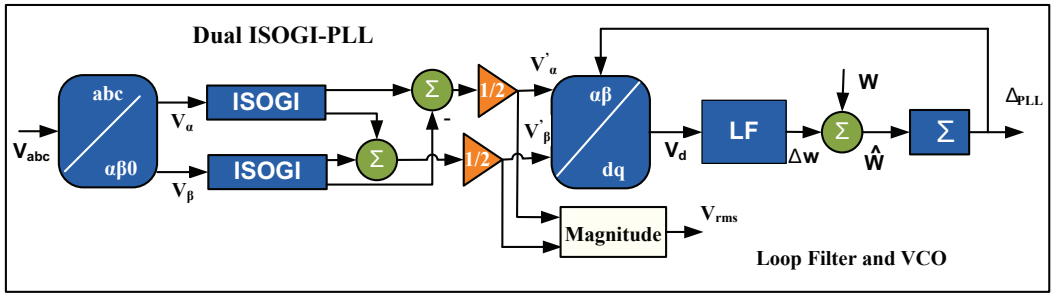

Figure 3: Improved Dual-SOGI Based PLL

In order to extract exact magnitude of in - phase and quadrature outputs, the input nominal frequency must be equal to the frequency estimated by the SO-SOGI-PLL.

The entire design procedure of ISOGI-PLL is clearly explained in [19].

B. Estimation of Unit Voltage Templates

Figure 3 shows the closed loop block diagram of Dual ISOGI-PLL. Three-Phase PLL is used to generate required in-phase and quadrature templates separately. The output phase angles (U_a, U_b, U_c) that are generated from the ISOGI-PLL are considered as unit templates.

C. Reference Current Generation

The peak amplitude of active component of current is calculated similarly as shown in Figure 3. I_{Labc} is supplied to ISOGI based quadrature signal generation for estimation of peak load current. The voltage (V_{dc}) across the DC bus capacitor is compared with the V^*_{dc} (reference DC bus voltage) and the error signal is passed through a Proportional-Integral Controller to regulate the DC bus voltage. The error of the signal is given by:

$$V_{loop}(n) = V^*_{dcref}(n) - V_{dc}(n) \tag{1}$$

The error is then supplied to PI controller to regulate the voltage of DC bus of DSTATCOM. The output of the PI controller is given by:

$$I_{cd}(n) = I_{cd}(n-1) + k_p\{V_{loop}(n)\} + k_i V_{dcer}(n) \tag{2}$$

where, k_p and k_i are gains of PI controller.

The average magnitude of current (I_p) and the output of the PI controller (I_{cd}) are summed up ($I_P = I_p + I_{cd}$). Finally, the resultant active component of current is multiplied with the unit templates (U_a, U_b, U_c) that are generated by the grid voltage to generate three reference source currents. These three estimated three-phase reference source currents (i^*_{sa}, i^*_{sb}, i^*_{sc}) are compared with the source currents sensed at the point of common coupling

(i_{sa}, i_{sb}, i_{sc}) to estimate the error in currents. The error currents generated are supplied to a PWM controller to generate PWM gating pulses for DSTATCOM as shown in Figure 4.

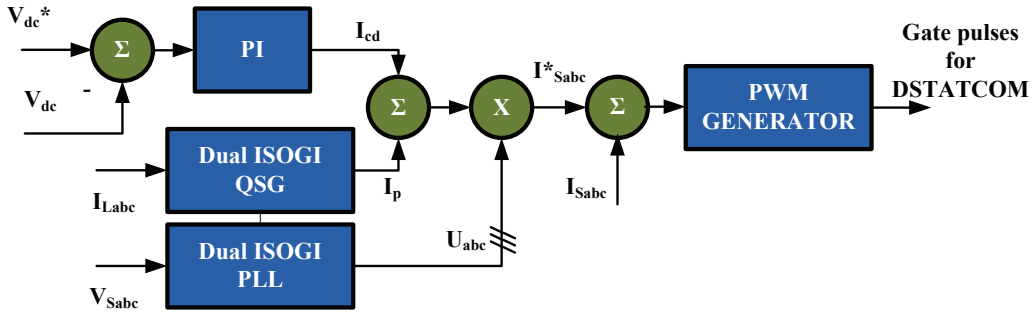

Figure 4: Proposed Control Algorithm based on Dual ISOGI

$$i^*_{sa} = I^*_P U_a,\ i^*_{sb} = I^*_P U_b,\ i^*_{sc} = I^*_P U_c \tag{3}$$

3. SIMULATION RESULTS AND DISCUSSION

In this section, the improved control algorithm is evaluated and tested using MATLAB/Simulink on a three-phase distribution system loaded with linear and non-linear loads as shown in Figure 1. Fixed time step of 10µs with ode1 (Euler) solver is chosen for simulation. In the test cases mentioned below, the load currents and source voltages are distorted and unbalanced. If the source voltages become distorted then the unit templates generated by the distorted signals produce erroneous outputs. To overcome this limitation, an ISOGI based PLL is used which acts as adaptive filter in distorted conditions and produce an exact result within the shortest period of time even when a DC-offset is produced due to A/D conversions. Once the outputs generated by the ISOGI are obtained, the commands are then supplied to generate reference source currents as shown in Figure 4.

Some of the below test cases are chosen in the simulation. Source Voltages, Source Currents, Load Currents, Injected Currents, Estimated Peak Current and DC link Voltage are observed.

1. Performance of the proposed system with ideal grid conditions and with DSTATCOM under balanced Non-linear Load.

   In this condition, a steady non-linear load is applied and the source current is balanced and sinusoidal. The results are proved satisfactory performance with reactive and harmonic compensation as shown in Figure 5.

2. Performance of DSTATCOM with ideal grid conditions and Un-balanced linear and non-linear loads.

   In this condition, load is made unbalance and the source current is still balanced as shown in Figure 6.

3. Ideal grid conditions with sudden increase of loads.

   To test the dynamic performance of the system, a sudden increase in load is applied and compensation is done effectively as shown in Figure 7.

4. Balanced Voltage sag and swell (0.5 p.u.), sag with phase jump (30^0) is introduced in the grid voltage as shown in Figure 8, 9 and 10.

   These PQ problems are introduced in the grid voltage signal to test and evaluate the performance of the PLL control algorithm. The compensation is not affected even the grid is distorted.

5. Un-Balanced Voltage sag is introduced in the grid voltage (Figure 11).

   When the grid voltage is made unbalance, then the source current is also affected if there is no proper compensation algorithm. But the proposed algorithm made the source current balanced and sinusoidal.

6. Harmonics injected (5^{th} & 7^{th}) into the grid voltage.

   Due to change in the grid impedance, grid voltage and currents are affected. But, the source current is not affected due to harmonics in the grid voltage because of an effective compensation provided by the DSTATCOM as shown in Figure 12.

7. DC offset (10%) is produced in the grid voltage.

   In real time applications, production of DC offset is very common due to A/D conversions. But, the overall performance is not affected as shown in Figure 13. Improved SOGI eliminates DC-offset signal presented in the signals.

8. A Frequency step of 5 Hz is introduced in the grid voltage (50Hz to 55Hz) (Figure 14).

   Frequency is changed beyond the normal operation due to sudden switching off loads or any major loss in tie-line. This condition is executed to test the performance of the PLL under frequency changes.

These are the test cases considered for verifying the dynamic performance of control algorithm employed for DSTATCOM. The ability to track the phase angle even under several grid distortions is made simpler and accurate with the proposed PLL. Mostly electric networks are of meshed grids in many countries. Therefore, the equivalent impedance is very low and grid is considered as strong grid. If few lines are disconnected from the supply, then the equivalent impedance may change or increased. This condition is leading to weak grid. Similarly, voltage dips are also one of the causes for the system to become unstable. The DSTATCOM maintains the source current in phase with the local grid voltage in all conditions and the THD (% < 5%) is within the IEEE limits. All these test cases are considered to prove the tacking effectiveness of the PLL.

THD (%) is measured for all the cases as shown in Table II. For the ideal grid conditions (1, 2 and 3), the source current is maintained within IEEE limits. When the grid voltage is affected, then the source current THD is increased. But, the source current is still within IEEE 519-1992 limits which prove the effectiveness of harmonic and reactive power compensation.

A similar research was carried out in [20], but this theory uses an EPLL and the output THD (%) presented in the paper is nearly 4% which is greater than the proposed method. The research was carried out under ideal grid voltage conditions and weak grid conditions are not presented because of the poor response of an EPLL [21]. In [21], PLL algorithms are compared and SOGI-PLL was found effective compared to conventional PLL's.

4. CONCLUSION

In this paper, a simple and effective control algorithm for DSTATCOM is implemented based on Dual ISOGI-PLL. The controller has been analyzed, presented and validated using MATLAB/Simulink. This theory is adopted to work in ideal and weak grid voltage conditions. The source current is maintained within IEEE limits 519-1992. This algorithm is tested under non-linear load current and grid voltage conditions including grid harmonics, frequency step change and dc offset and found satisfactory for reactive current and harmonic compensation. The DC bus voltage is also regulated to avoid unbalancing problems and power losses.

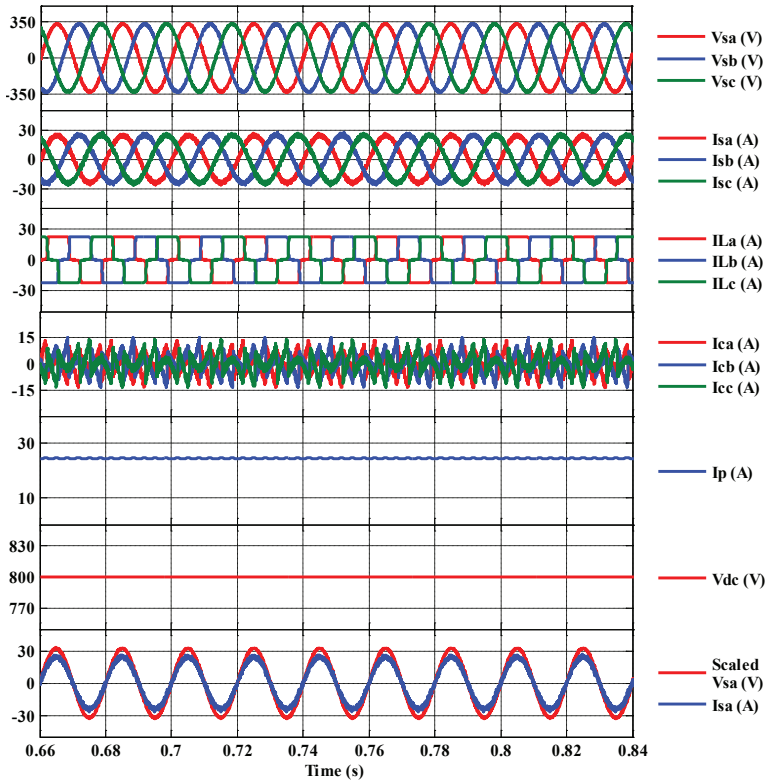

Figure 5: A Steady Non-Linear Load is applied

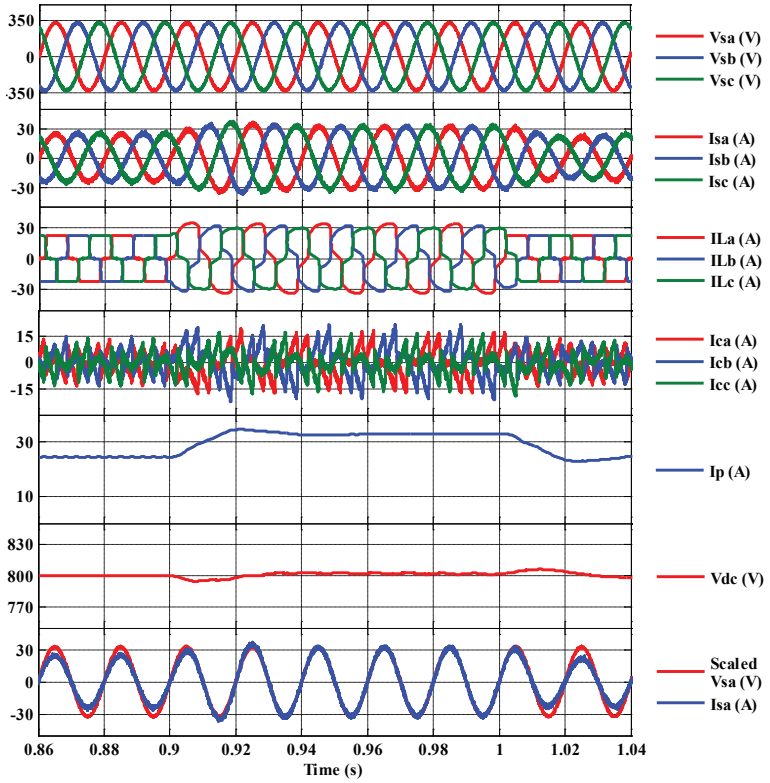

Figure 6: Unbalance in Load is applied

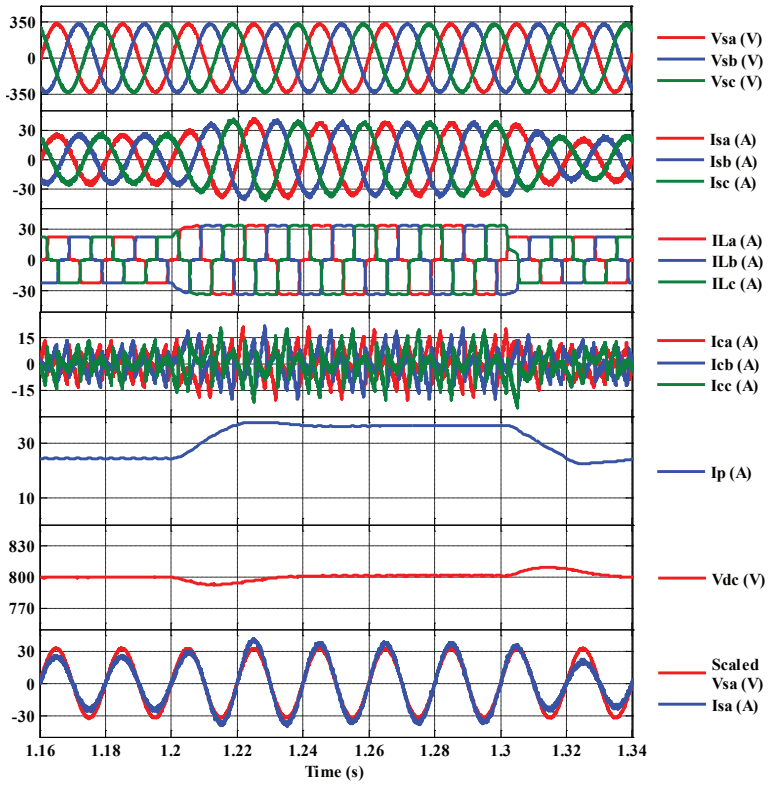

Figure 7: Sudden Increase in Load is applied

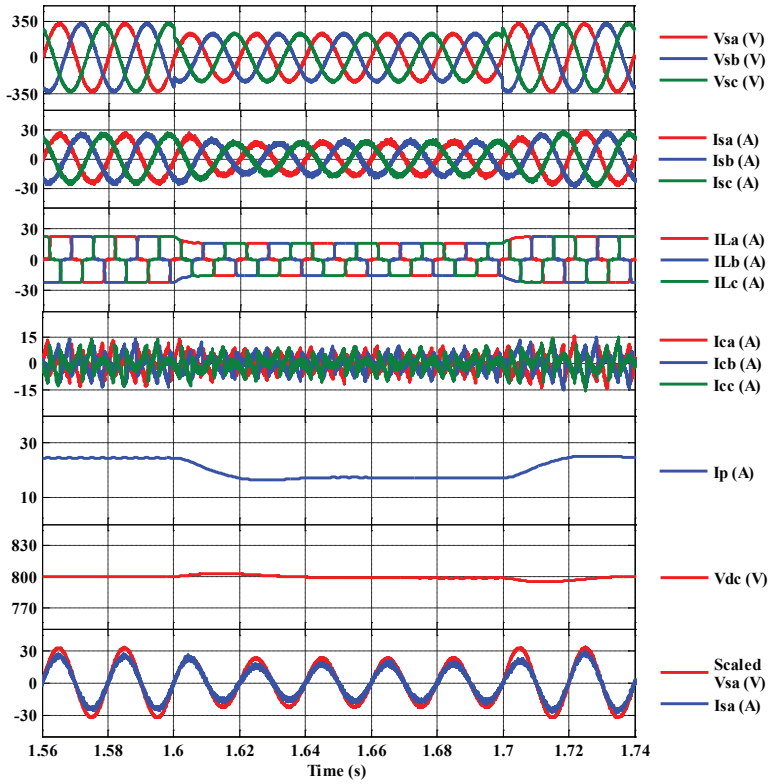

Figure 8: Balanced Voltage Sag (30%) is applied

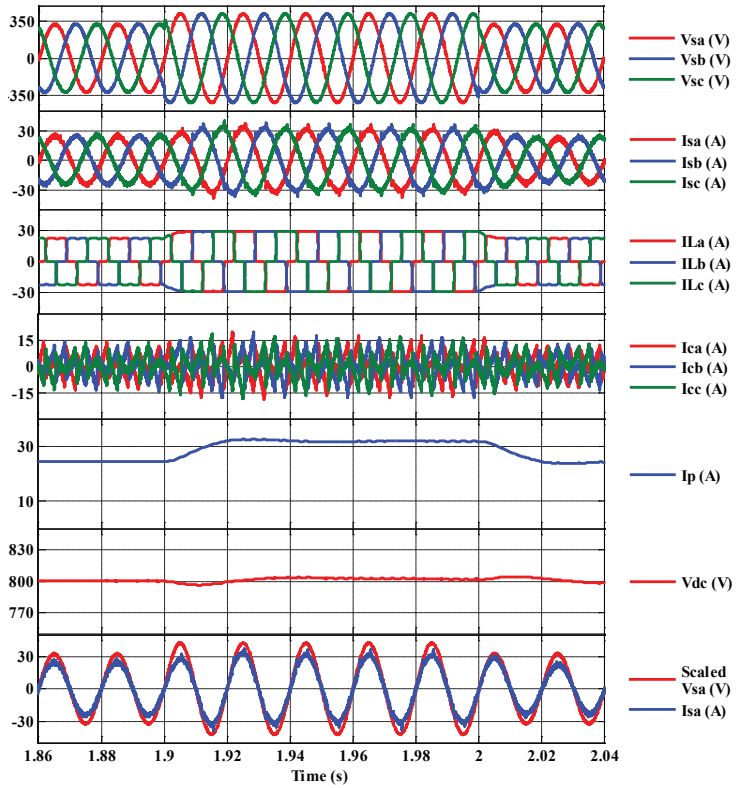

Figure 9: Balanced Voltage Swell (30%) is applied

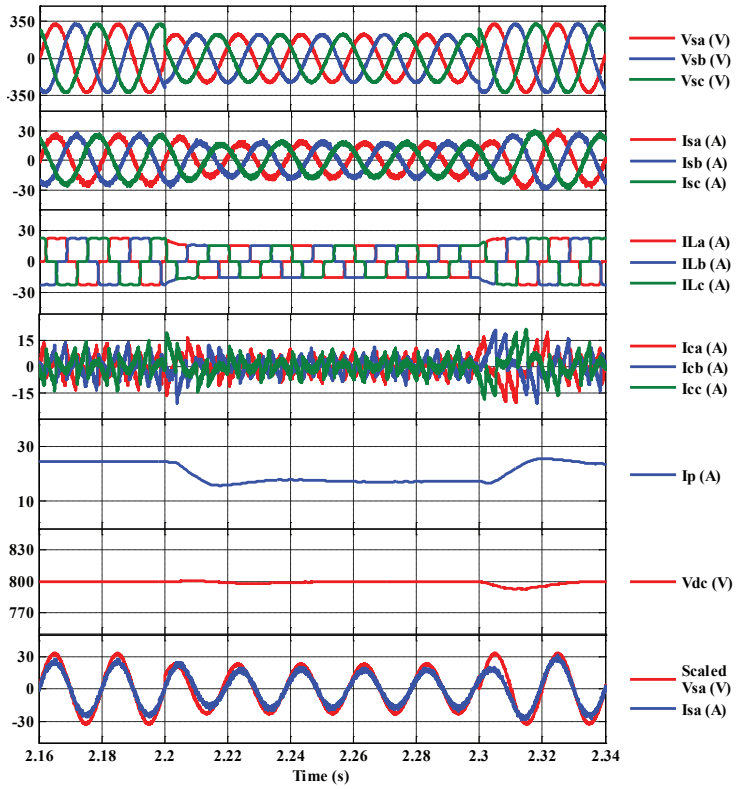

Figure 10: Balanced Voltage Sag (30%) with Phase Jump (30^0) is applied

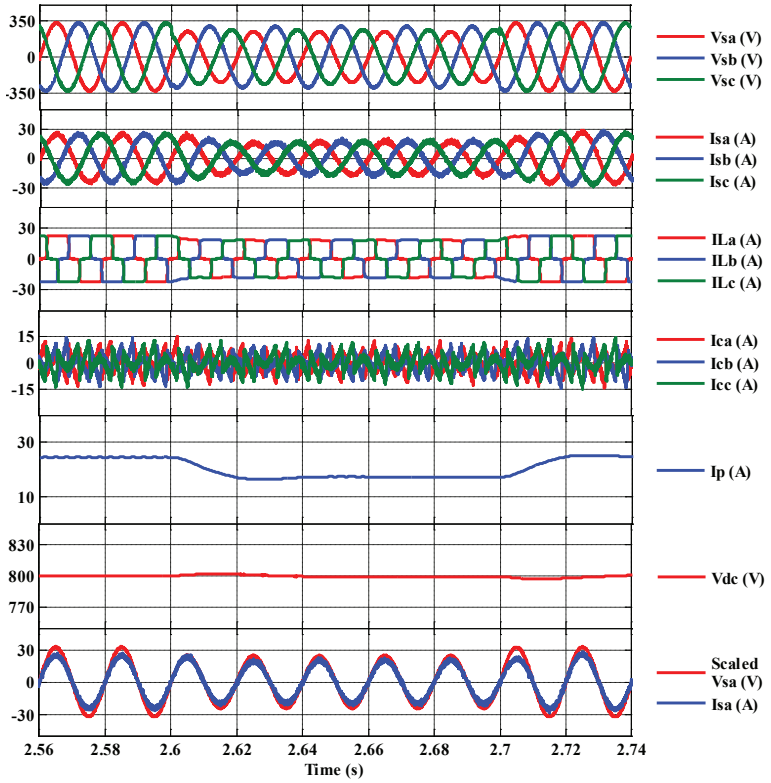

Figure 11: Un-Balanced Voltage Sag is applied

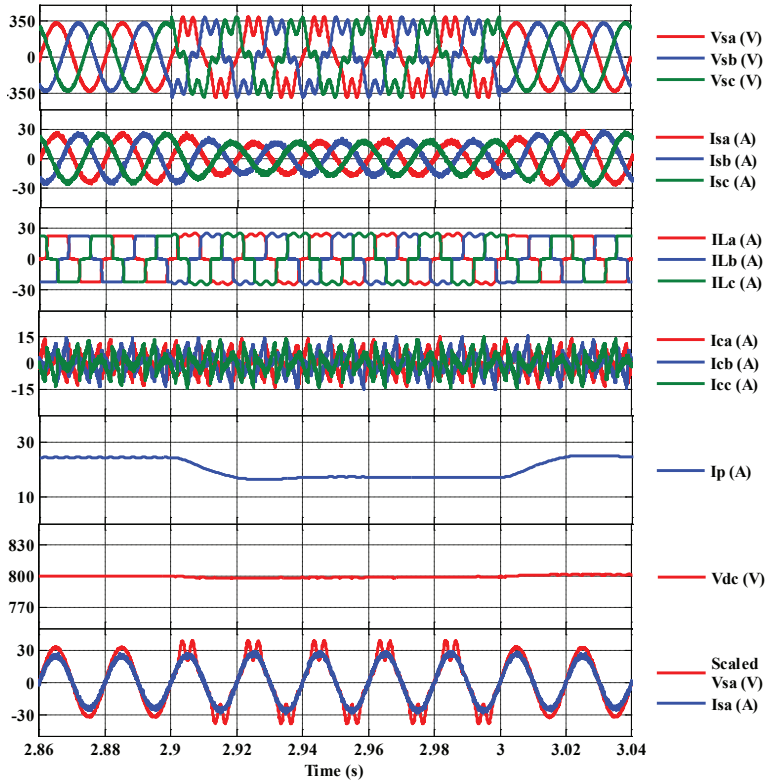

Figure 12: Harmonics injected into the grid voltage

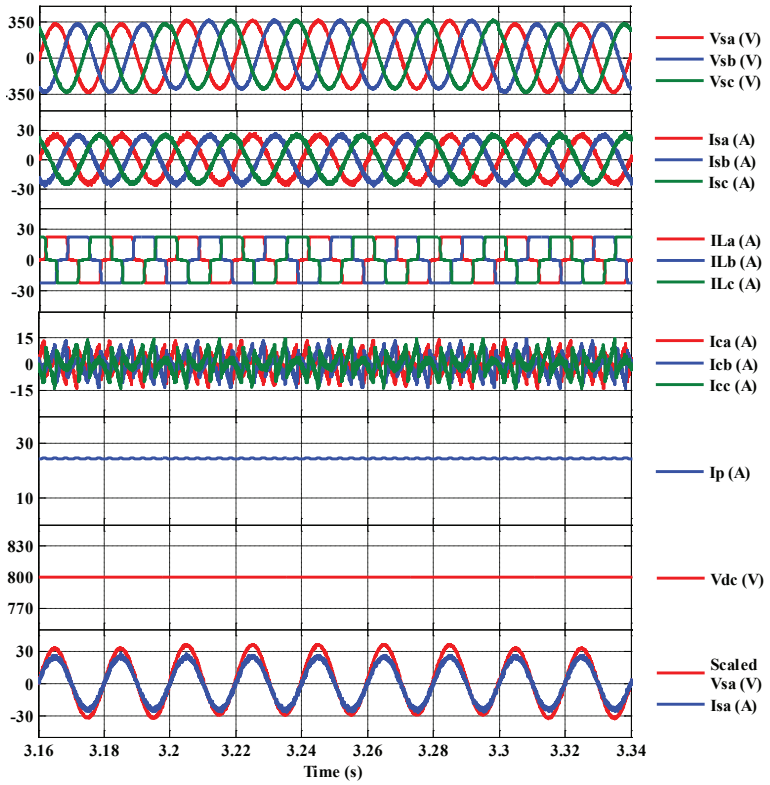

Figure 13: DC offset is produced in the Grid Voltage

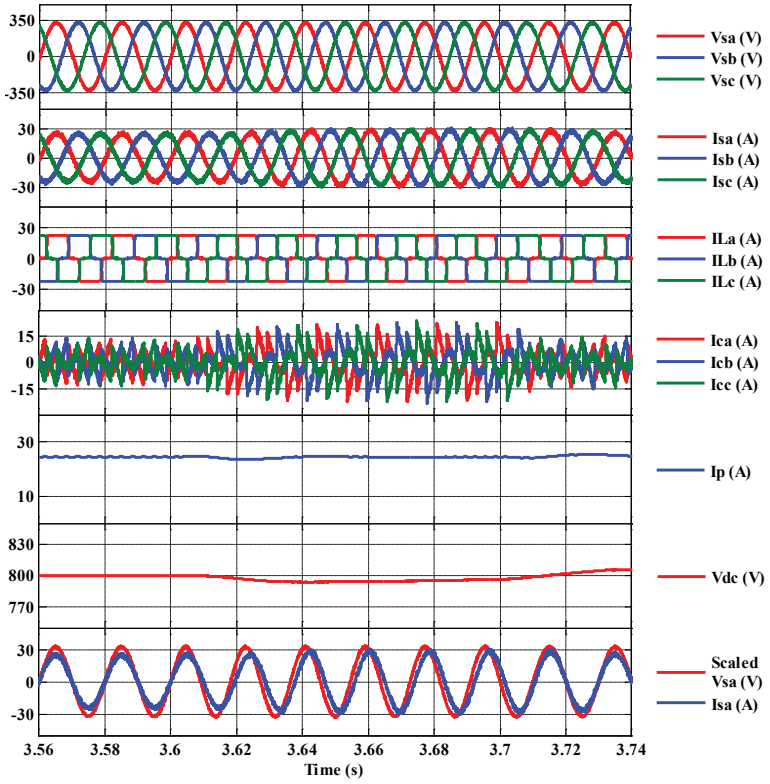

Figure 14: Frequency Step (50 to 55 Hz) is introduced in the Grid Voltage

Table 1
Appendix

Parameter	*Value*
AC supply source & Frequency	3-Phase, 415 V (L-L), 50Hz
Source Impedance	Rs = 0.03 Ω, Ls = 1.8mH
Non-linear: Three-phase diode bridge rectifier	R = 45 Ω, L = 250mH,
Linear Load	R = 48 Ω, L = 50mH
Rating of VSC	10 KVA
PWM Switching frequency	8kHz
Reference voltage of DC bus	850V
Interfacing inductance	L_f = 12mH
DC bus gains of PI controller	kp = 0.45, ki = 4

Table 2
THD (%) of Test Cases

Fig. No.	V_{sa}	I_{sa}	I_{La}	*Fig. No.*	V_{sa}	I_{sa}	I_{La}
5	0.08	2.3	25.17	10	0.09	2.75	25.14
6	0.07	1.78	16.75	11	0.08	2.15	26.84
7	0.07	1.71	23.93	12	24.68	2.33	24.40
8	0.10	2.69	25.12	13	0.07	2.18	25.16
9	0.10	3.61	25.17	14	24.19	23.04	33.52

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