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Implementation of Different Sensing Scheme For SRAM

Mohammad Jafar Umer* and P. Aruna Priya**

ABSTRACT

Static Random-access Memory (SRAM) takes up a large portion in the design of the System-on-Chip (SoC) area. In addition, the total power consumption of the SoC is dominated by the leakage and dynamic power of SRAM. Although using small-size transistors and lowering supply voltage (VDD) can reduce the SRAM area and power consumption, respectively, both of these methods degrade the noise margin and increase the vulnerability to process variation. In particular, the read stability of conventional 6T SRAM is significantly degraded because the 0 storage node is increased by bit-line (BL) charge injection during the read operation. To overcome the above problem the we implement the following precharge sensing scheme [1]Domino Sensing[2]Pseudodifferential Sensing [3] Coupled [4] Trip point Sensing.

Keywords: Bit line (BL),local bit line (LBL),static random access memory(SRAM),system on chip(soc) .

1. INTRODUCTION

The major problem in modern IC design is power consumption. In order to reduce the power consumption we scale down the transistor size due to which the stability of the SRAM cell is decreased because of reduced in noise margin. In order to improve the stability we have to increase the size of transistor but that is not a good assumption[1] [2].

In conventional 6T SRAM cell the stability is decreased while reading the data because the precharged bit-line (BL) injects charges into '0' storage node causing to flip the data during read operation. To overcome this, SRAM cell is provided with separate read path which is shown in Fig 1.The structure which is shown in fig 1 is known as 8T SRAM cell which uses two nMOS transistor. The read operation is performed by detecting Read BL (RBL) voltage while asserting Read Word Line(RWL). When the selected SRAM cell stores the data 0, which means the right storage node stores 1, current flows through the read path, and the RBL voltage becomes low. If the selected SRAM cell stores 1, the RBL voltage remains high by maintaining the voltage that is close to the RBL precharge voltage[3]

In order to improve the speed of the SRAM cell we are implementing the different sensing scheme for SRAM and also in order to decrease the power consumption the 8T SRAM cell is replaced by 10T

SRAM cell which is merged with different sensing scheme and give better performance.

In this paper we present a compressive comparison of 8T and 10T in term of power, delay, and power delay product. we also compare the different sensing scheme .The rest of paper is organized as follow. In Section 2 we introduce 10T SRAM cell and discuss how is different from 8T.In section 3 we discuss about different sensing scheme and their implementation in cadence virtuoso on 45nm technology also discuss on the analysis. section 4 deals with the result and comparison between 8T and 10T.The comparison between different sensing scheme is also discussed in this section. Section 5 conclude the paper.

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2. 10T SRAM CELL

The figure 2 shows the implementation of 10T SRAM cell in cadence virtuoso, the 10T SRAM cell make use of transmission gate structure in the read path. The write operation of the cell is same as the conventional SRAM cell but the read operation uses four extra transistor than conventional 6T SRAM cell. The advantage of structure is that, the RWL and RWL bar signal feed to both gates of pass transistor logic. So either change in q or qbar get reflect when RWL is asserted so we can get better stability. The figure 3 shows the transient analysis of 10T SRAM cell.

In the waveform the different signal shows which is given to SRAM cell in the pulses. The output of 10T SRAM is taken at RBL which is Same as qbar output because the qbar out is fed to the Transmission gate, the transmission gate allow the full swing and also reduces the glitches which present in the on the qbar output so we better output and also the stability is improved.

3. SENSING SCHEME

This section discuses the four kinds of sensing scheme which are as follow, (a)Domino sensing (b)Pseudodifferential sensing (c)AC coupled sensing (d)Trip point bitline precharge sensing.

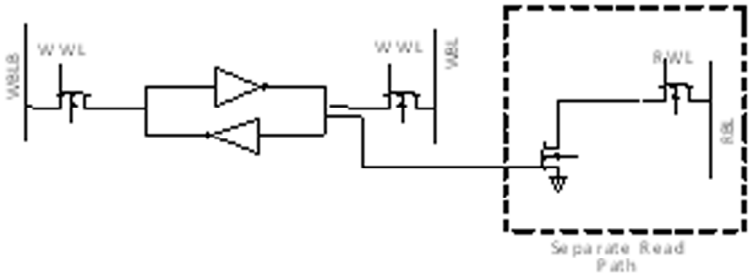

Figure 1: 8T SRAM Cell

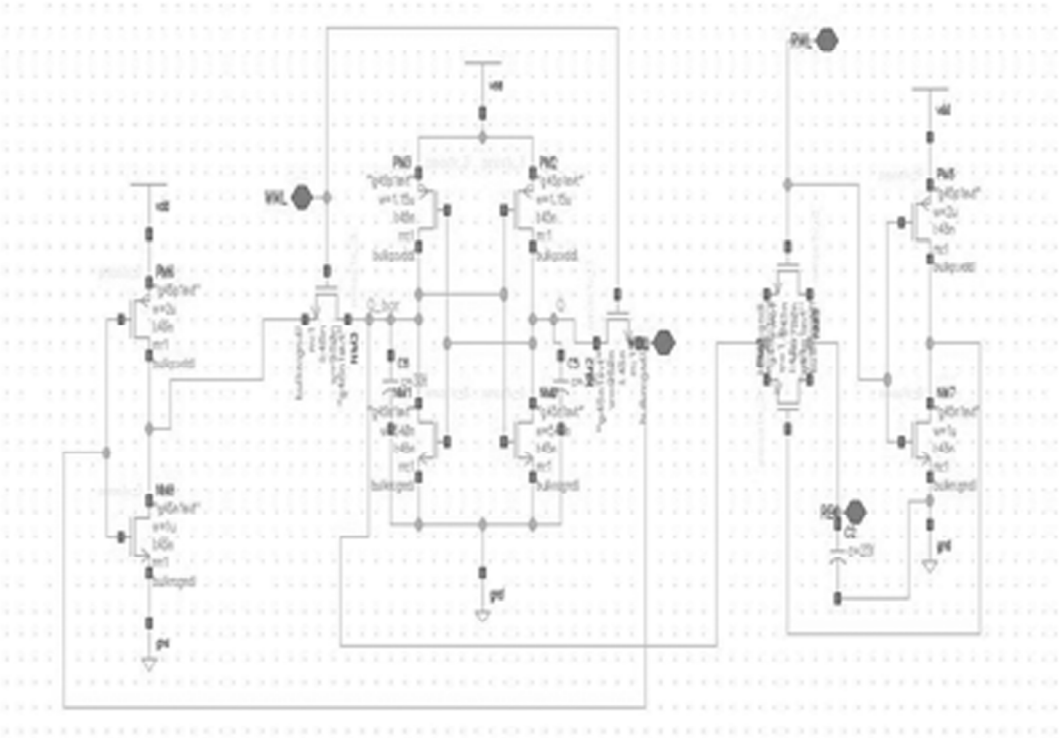

Figure 2 : 10T SRAM cell

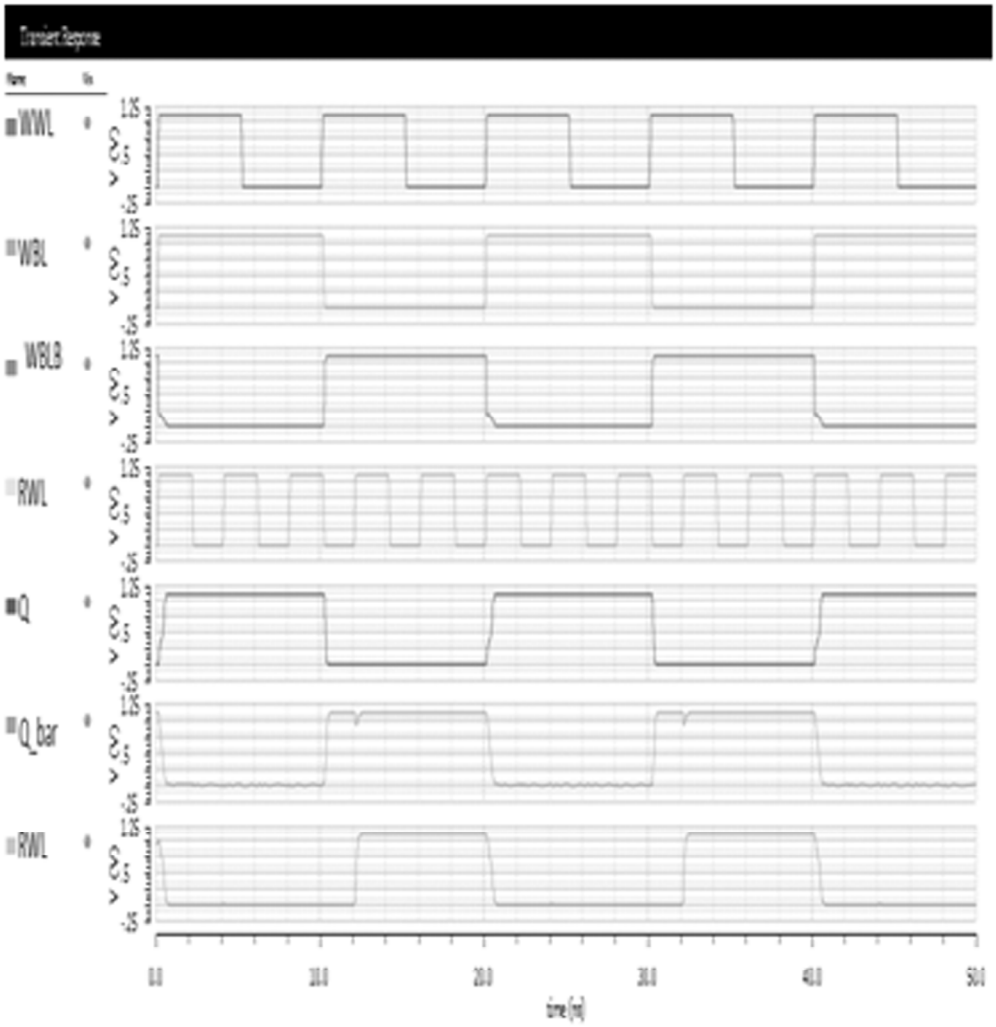

Figure 3: Transient Analysis of 10T SRAM

3.1. Domino Sensing

The Domino sensing is a simplest sensing scheme which is shown in figure 4**,** the local BL is connected to a pmos transistor while sensing zero the pmos transistor turned on which will further turn on the other

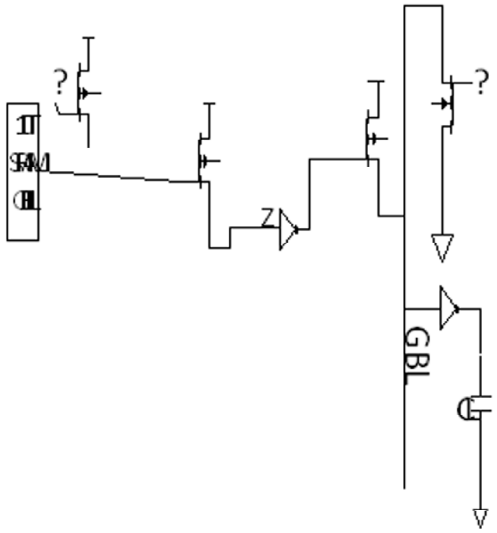

Figure 4: Domino Sensing

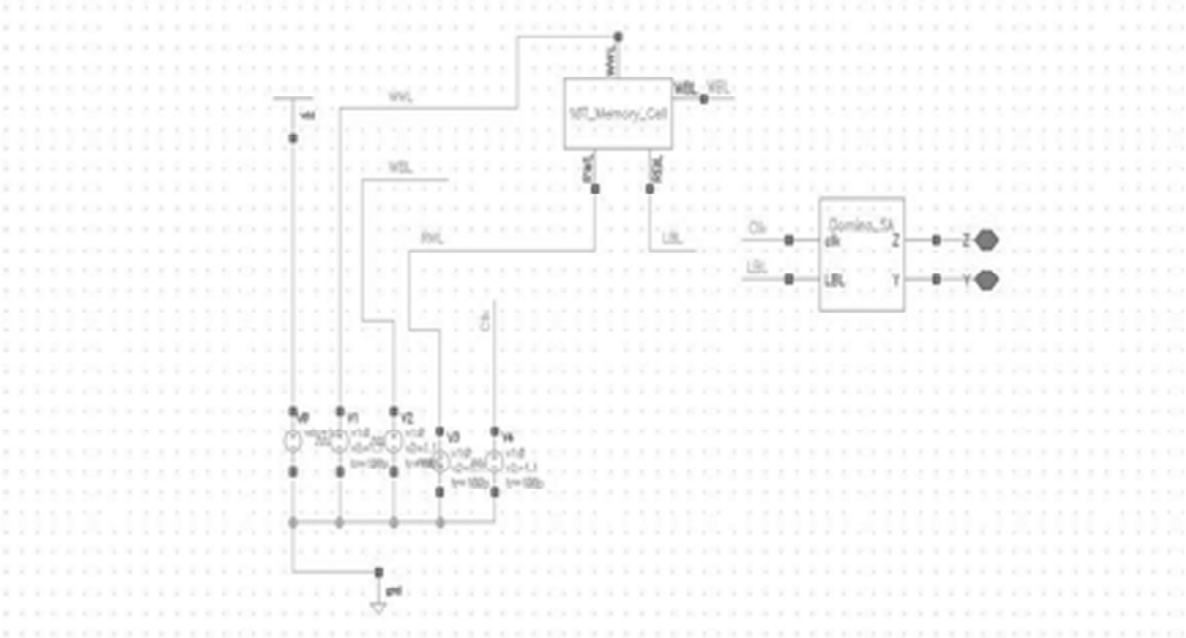

Figure 5: Implementation of Domino sensing

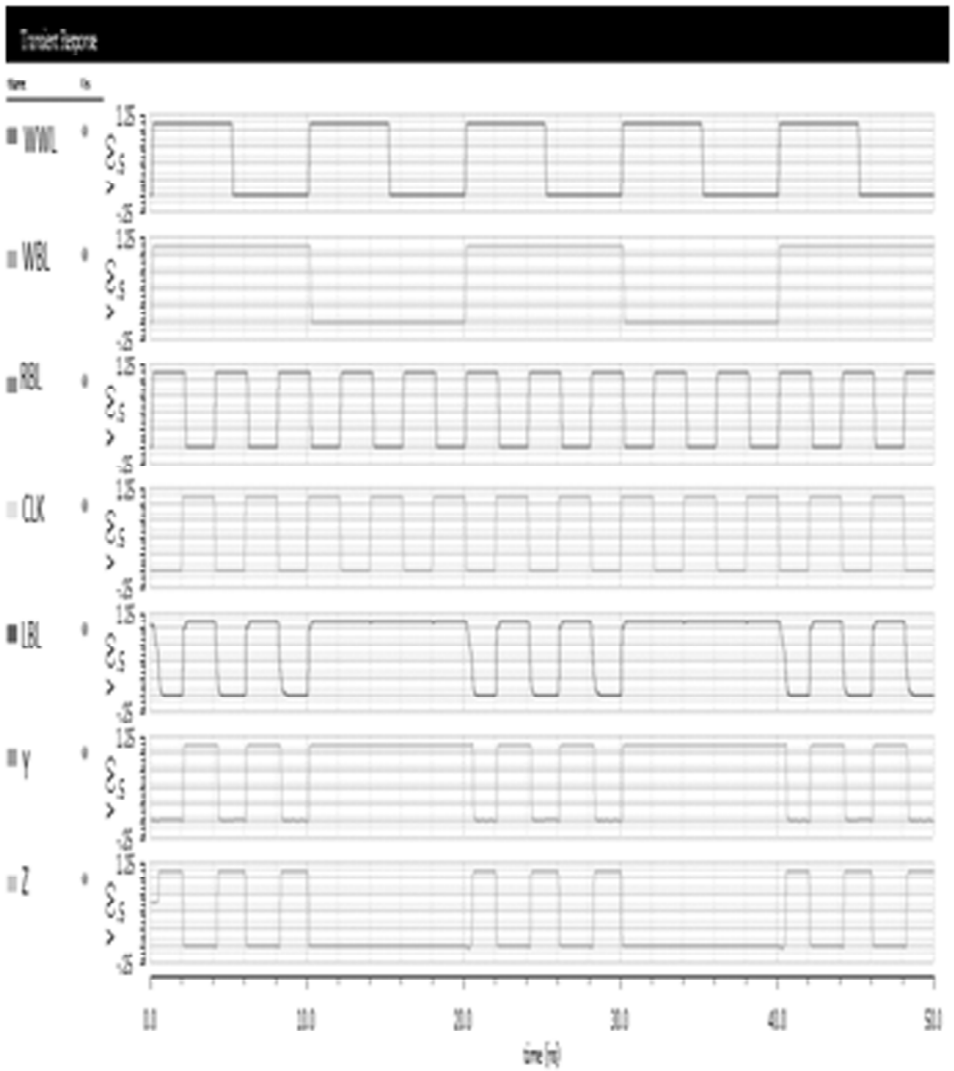

Figure 6: Transient analysis of Domino sensing

pmos transistor through inverter which will charged global BL(GBL).The performance of Domino sensing is degraded because of large capacitor is required. The figure 5 shows the implementation of Domino sensing with 10T SRAM cell in cadence virtuoso on 45nm technology. The figure 6 shows the transient analysis of Domino sensing[3].

3.2. Pseudodifferential Sensing

The figure 7 shows the Pseudodifferential sensing, It consist of a latch type of voltage sense amplifier and a reference input. The advantage of the circuit is to amplify the small voltage difference into logic level. It does not required full swing RBL which will reduced the power consumption of the sensing. The reference input is used to discharge the BL slower for data '0' cell but faster than the data '1 cell. The use of reference input and strobe signal may cause the adverse effect on process variation temperature, which will degrade the performance[3-5].

The figure 8 and 9 shows the implementation of pseudodifferential sensing scheme in cadence and transient analysis for same respectively. The sensing scheme is implemented with the 10T SRAM cell. The waveform will describe the behavior of the sensing scheme. The input to the sensing scheme is LBL and output is taken on the node Y. The latch will suppress the unnecessary transition on the LBL[6, 8].

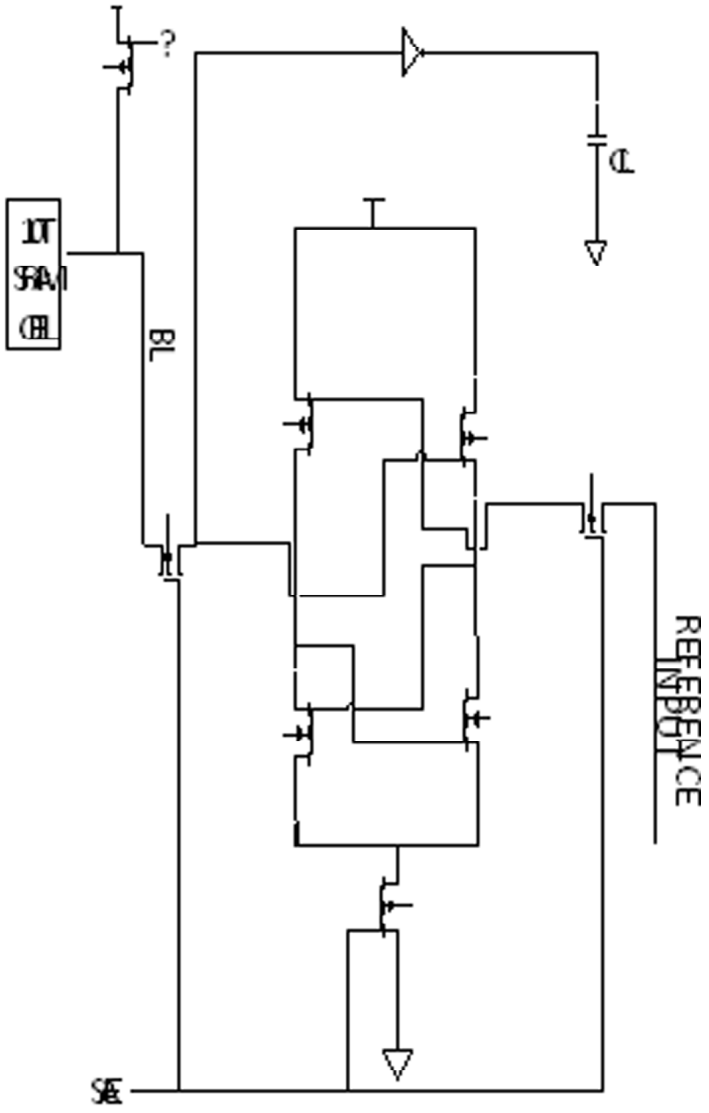

Figure 7: Pseudodifferential Sensing

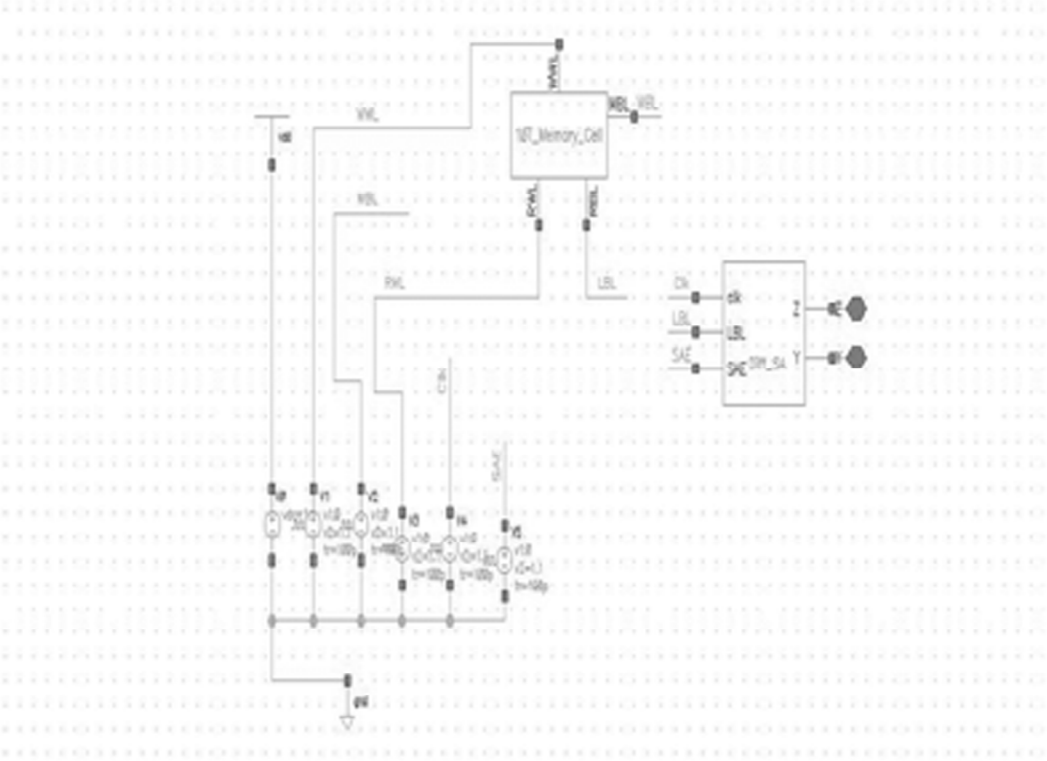

Figure 8: Implementation of Pseudodifferential Sensing

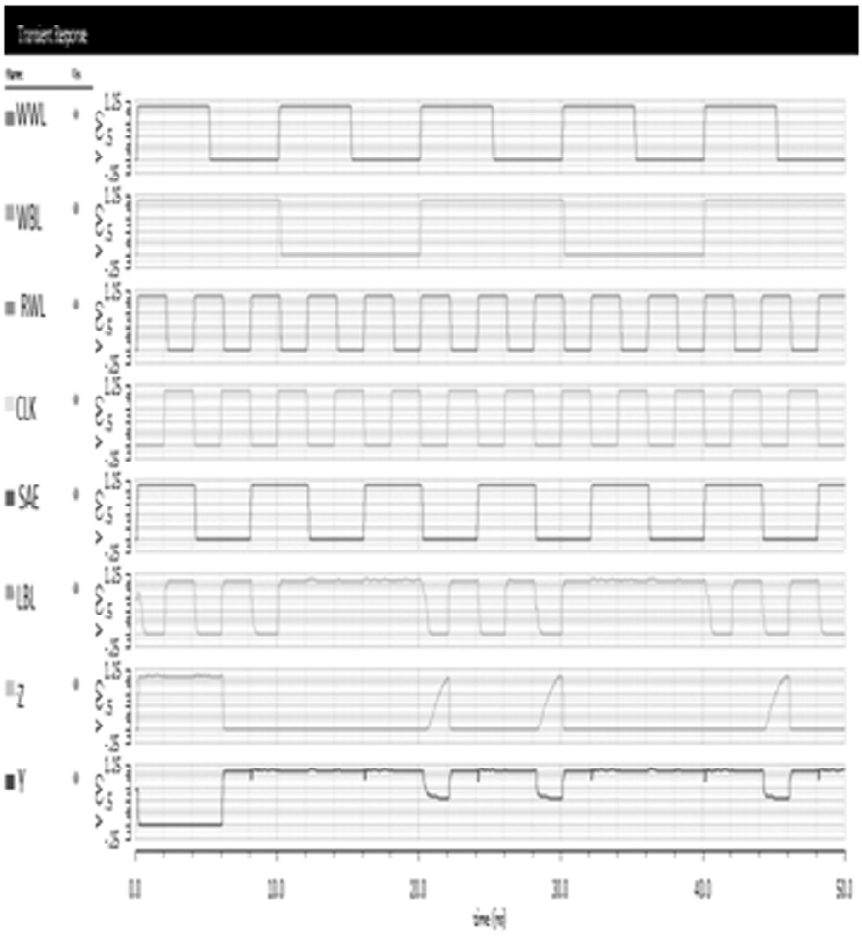

Figure 9: Transient Analysis of Pseudodifferential Sensing

3.3. AC Coupled Sensing

The AC coupled sensing scheme is shown in figure 10 which consist of the coupling capacitor (C_{in}), a CMOS inverter INV_A and a equalizing pMOS transistor. The inverter INV_A consist of a extra nMOS transistor M_{EN} which is used to enable during read operation in order to reduce the static power consumption. The sensing scheme operate in two modes, prechage mode and evaluation mode .In precharged mode the node voltage X_1 and Y_1 are equalized by transistor M_{EQ}. In evaluation phase the circuit will sense the signal which is present on the LBL[7].

Figure 11 and 12 shows the implementation of AC coupled sensing scheme and transient analysis respectively. The sensing scheme is implemented with 10T SRAM cell. The waveform shows the behavior of the circuit to different signal.

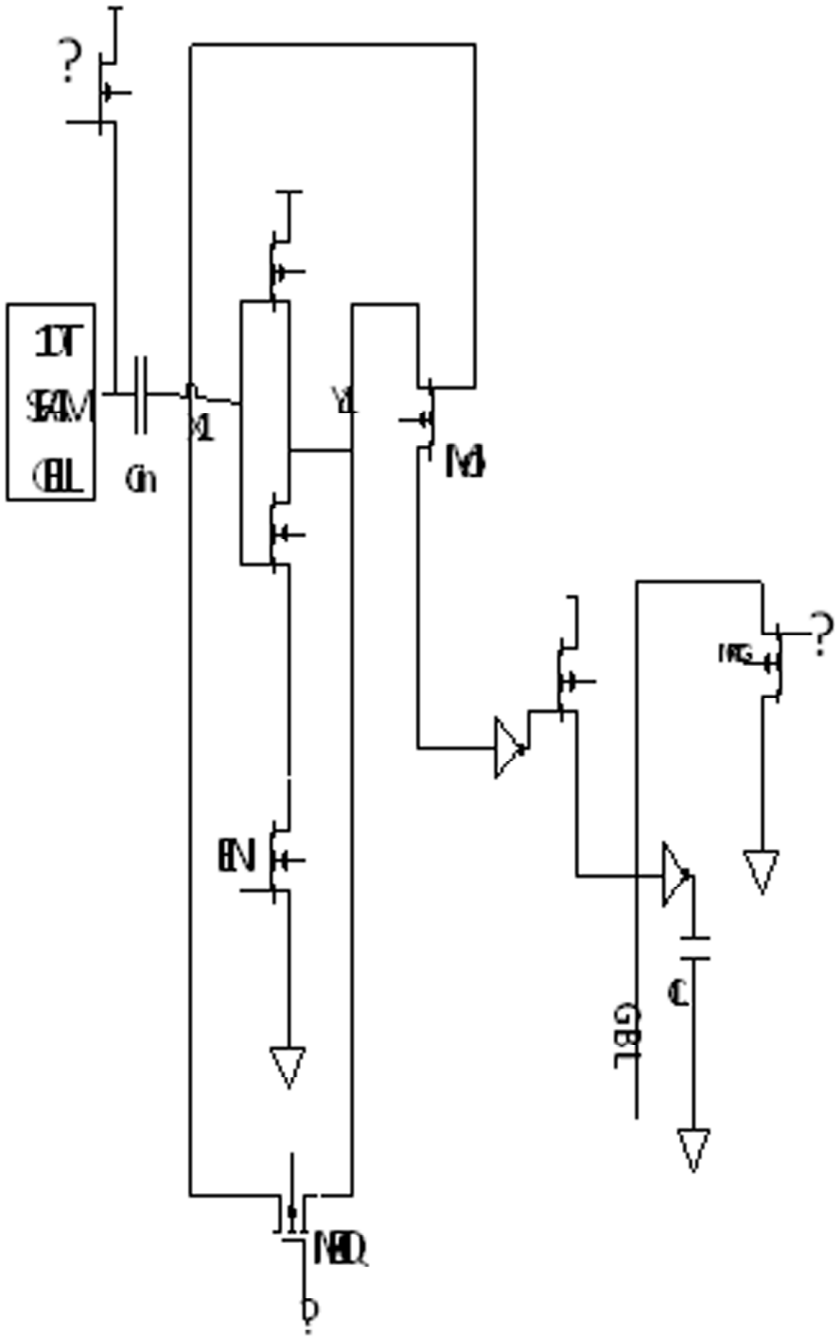

Figure 10: AC Coupled Sensing

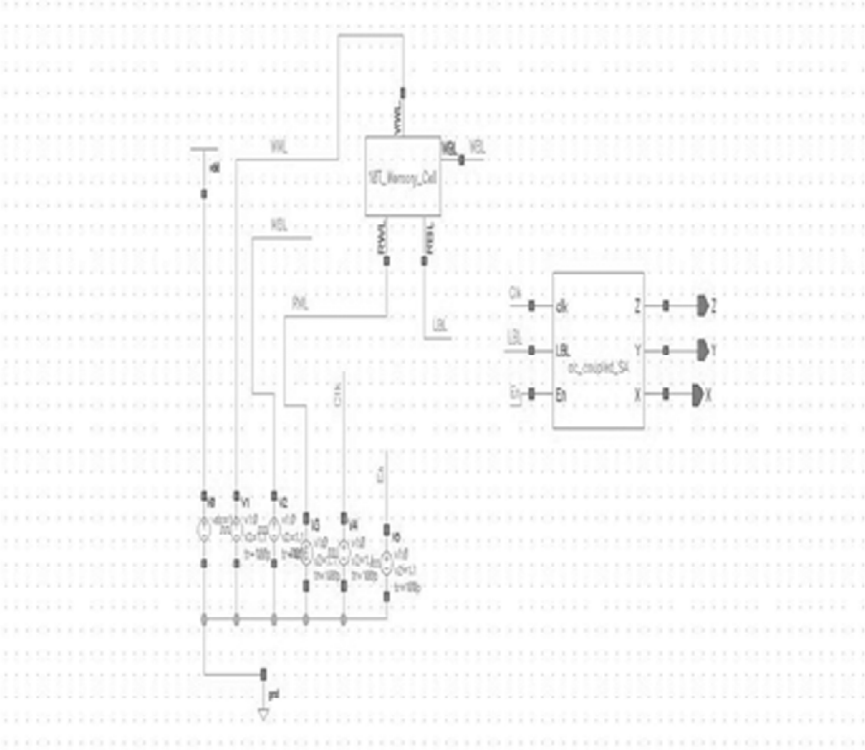

Figure 11: Implementation of AC Coupled Sensing Scheme

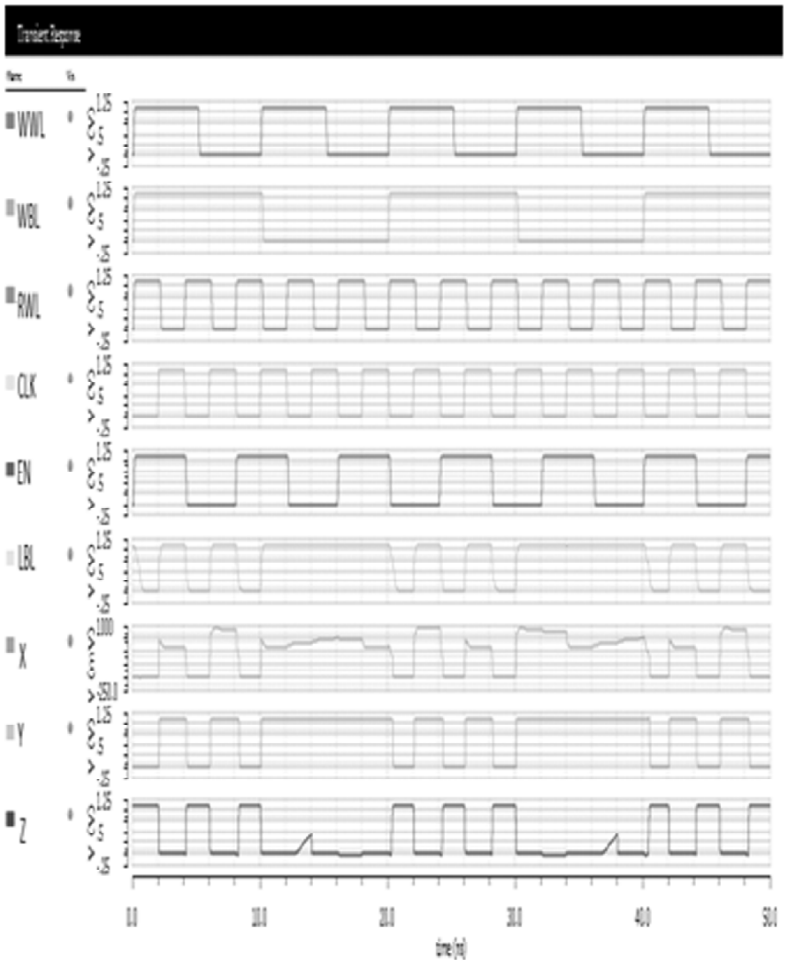

Figure 12: Transient analysis of AC Coupled Sensing Scheme

3.4. TBP Sensing Scheme

TBP is referred as (trip point bit line precharge) the structure of the TBP sensing scheme is quite similar as AC coupled sensing but there are two major changes, first the pMOS transistor which is used for precharging the LBL is replaced with nmos transistor and second the transmission gate is used in place of equalizing pMOS transistor. The structure of TBP sensing scheme is shown in figure 13. The TBP sensing scheme is

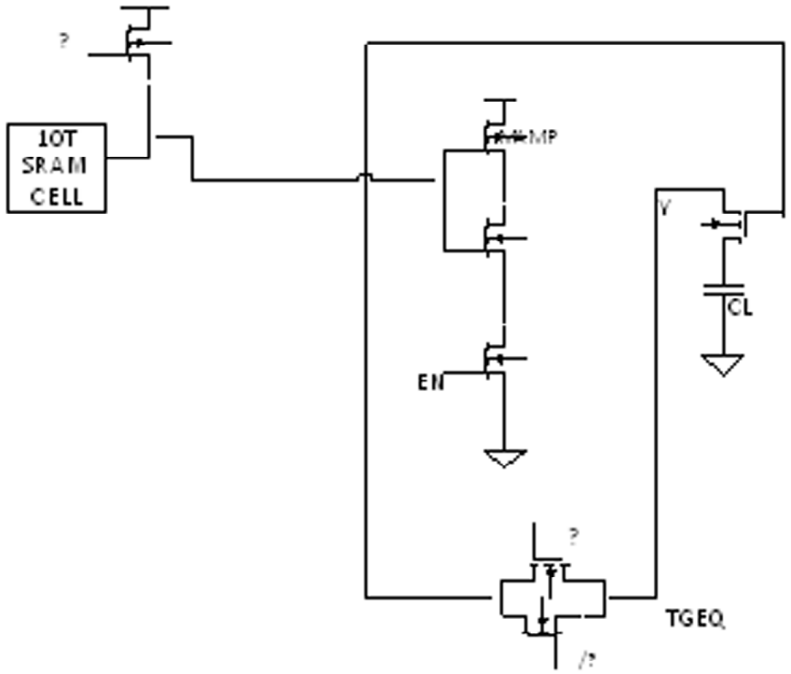

Figure 13: TBP Sensing Scheme

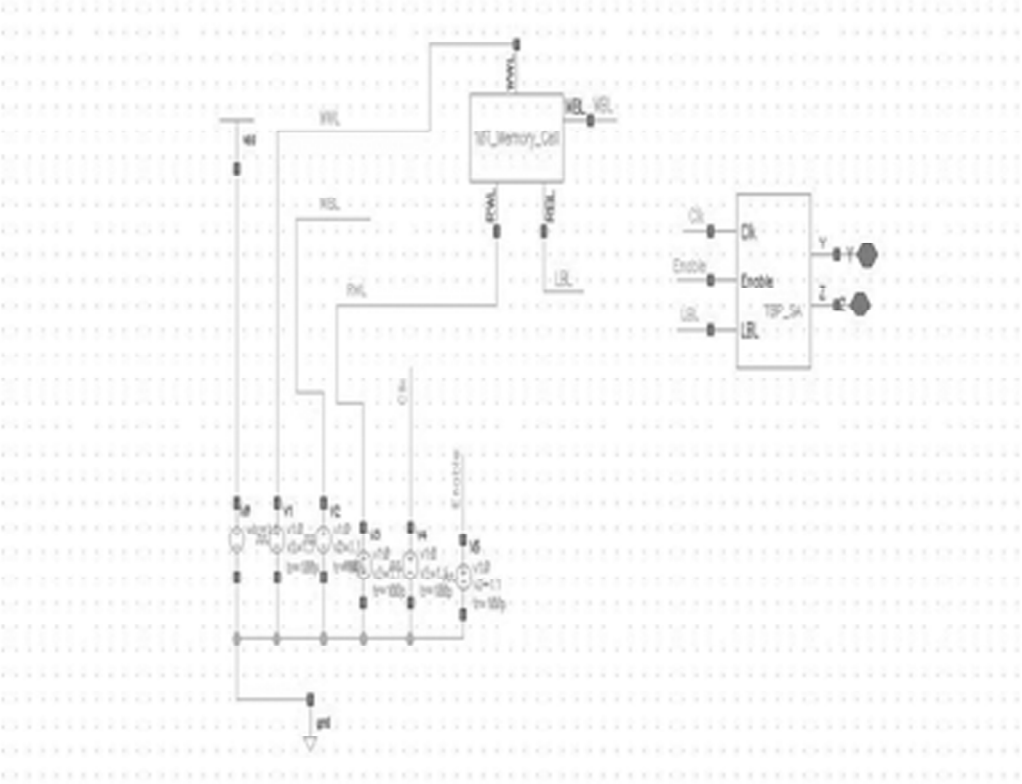

Figure 14: Implementation of TBP Sensing Scheme

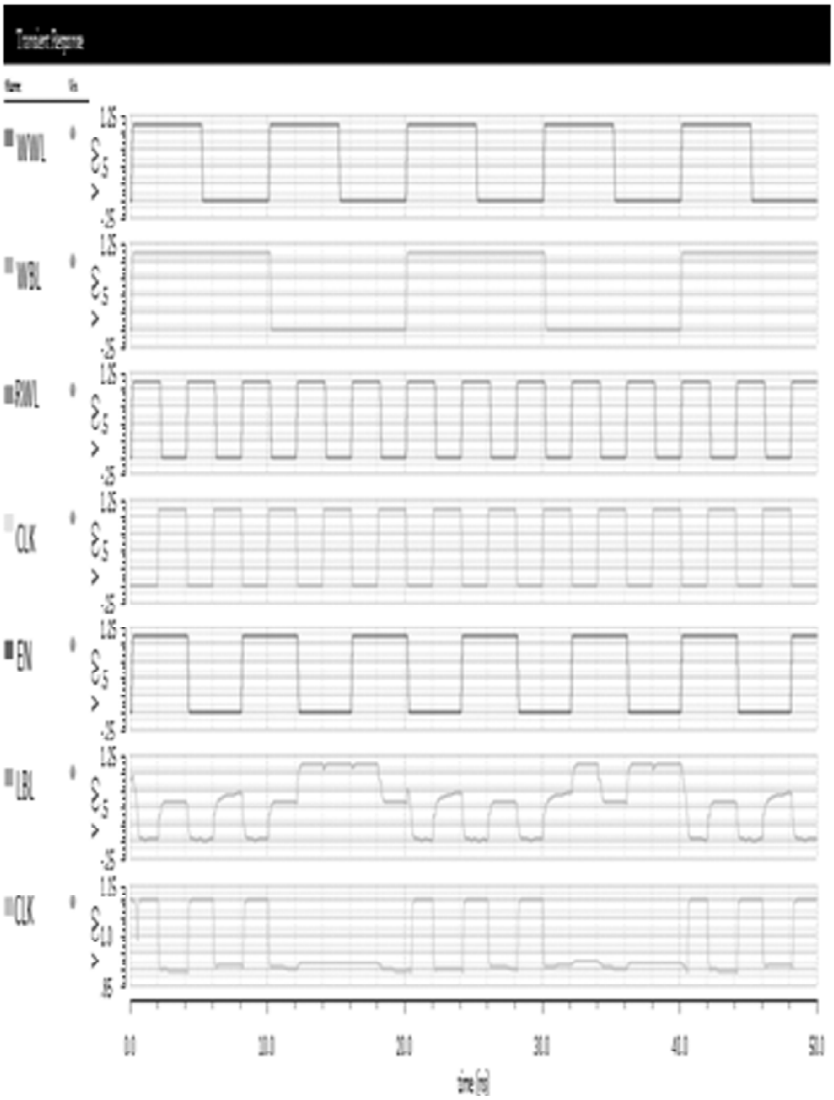

Figure 15: Transient Analysis of TBP Sensing Scheme

directly precharge the LBL near to the trip point of INV_T. During precharge the nmos transistor precharge the LBL and also at the same time the transmission gate T_{GEQ} and equalized the output to the inverter with the input. The use of transmission gate in the TBP sensing scheme removes the adverse effect of the pMOS which will present in AC coupled sensing scheme. Sensing the data which is present on the LBL is similar to AC coupled sensing scheme, here the INV_T charges node Y, due to high gain near the trip point while sensing '0'.The advantage of this sensing scheme is that it requires small BL capacitor which improve the performance of the sensing scheme[3].

The figure 14 and 15 shows the implementation of the TBP sensing scheme in cadence tool with 10T SRAM cell and the transient analysis waveform.

The drawback of the TBP sensing scheme is that, due to lower in BL the cell current is reduced which will deceased the performance but on the other hand due to lowering in current it will improve sensing margin and by decreasing DIBL i.e. drain induced barrier lowering of the unselected cell

4. SIMULATION RESULT

The table 1 shows the result of 8T and 10T SRAM cell, The simulation of the cell are done on cadence virtuoso on 45nm technology with the applied voltage is 1.25V. Here we have calculated

Table 1
Comparison Between 8T and 10T SRAM Cell

Specification	*8T SRAM*	*10T SRAM*
Power(μwatt)	52.39	9.311
Delay(nsec)	7.17	28.07
Power Delay product(fjoule)	375.63	261.4

Table 2
Comparison of Different Sensing Scheme

Specification	*Domino Sensing*	*Pseudo differential Sensing*	*AC Coupled Sensing*	*TBP Sensing*
Power(μwatt)	37.62	30.18	40.56	22.76
Delay(nsec)	14.82	13.01	7.942	3.906
Power Delay product(fjoule)	557.94	392.6	322.12	88.9

the power, delay and power delay product(PDP). The power delay product is nothing but the figure of merit which is defined as the power consumed over a period, which is measured in joule. As the PDP is less the circuit performance is good. The reason that 10T SRAM cell consume less power than that of 8T because of in 10T we are not preccharge the bit line and also it uses transmission gate which allow full swing but the delay will increase because of more no of transistor is used compare to 8T SRAM.

The table 2 shows the simulation result of different sensing scheme with the 10T SRAM cell on 45nm technology at 1.25V supply voltage. Here we have calculated the power, delay and power delay product(PDP). The TBP sensing gives us better result because it uses less number of transistor and also it uses transmission gate which allow full swing.

5. CONCLUSION

From the analysis of table 1 comparison we come to know that the 10T SRAM cell is better in performance than the 8T SRAM cell in term of power delay and power delay product(PDP).

In this paper we implemented the sensing scheme with the 10T SRAM cell. The table 2 shows the result for different sensing scheme from the above analysis of table we came to conclude that TBP sensing scheme is better among all sensing scheme.

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