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Harmonic Analysis and Comparitive Study of Various SVPWM Techniques Using Matlab

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Abstract : In general all ac drives fed with three-phase voltage source inverter (VSI) in order to obtain Variable voltage, variable frequency supply. Different Pulse width modulation (PWM) techniques can be employed to achieve variable voltage and variable frequency supply from three – phase VSI. Among all the PWM schemes, Space Vector PWM (SVPWM) and carrier-based sinusoidal PWM are the most widely used PWM schemes. The usage of Space Vector PWM is increasing day by day due to their effortless digital realization along with desirable dc bus utilization. In this paper comparison of different PWM techniques - conventional SVPWM, symmetric aligned sequence SVPWM, alternate aligned sequence SVPWM, hybrid PWM technique, Basic Bus Clamping Strategy PWM technique, and Boundary Sampling Strategy PWM technique is carried out using switching losses and THD as parameters. MATLAB/Simulink environment is used to simulate different PWM schemes with different switching patterns.

Keywords : VSI, SVPWM, THD, SIMULINK.

1. INTRODUCTION

In recent years due to lots of advances in solid state power devices, variable speed AC Induction motors powered by switching power converters are becoming more and more popular in all industrial sector due to their high efficiency and noise less performance. To reduce the harmonic content produced in the inverter circuit voltages is one of the major problems faced by many power electronic. In the low power application, classical square wave generator was used but it has some disadvantages such as it contains lower order harmonic in output voltage and it is very difficult to reduce them. One of the solutions to enhance the harmonic free environment in high power application is to use PWM techniques. [1]

In this regard several PWM techniques plays vital role in the Power sector and predominantly Space Vector PWM technique becomes the most popular technique because of its numerous advantages. It has potential of producing largest fundamental output voltage with output current having low harmonic distortion and is fit for digital implementation. By time averaging two active states and two zero states in every sampling period, the reference voltage vector is synthesized. In dividing the duration of zero states it offers more degrees of freedom compared to the TC approach and it is general. [2]

This paper mainly focuses on implementation of simple MATLAB/Simulink model. The reason behind choosing specifically this platform as development tool is because it is greatly used simulation software in Electric field. In this paper firstly principles of SVPWM presented followed by different SVPWM strategies and finally MATLAB/Simulink model with the simulated results for the proposed schemes.[8]

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2. THREE PHASE VOLTAGE SOURCE INVERTER (VSI)

The schematic diagram of a three-phase VSI is shown in Fig. 1 having six switches and each inverter leg is composed of two back-to-back connected semiconductor devices. In these two devices one device is a diode for protection and the other device is a controllable device.

Space vector is defined as; $Vs = 2/3(V_a + a^*V_b + a^{*2}V_c)$ (1)

The space vector is a function of time in contrast to the Phasor and is a complex variable. Where 1, 2, 3, 4, 5, 6 represents power switches (MOSFET) and $a^* = \exp^{(j2\pi/3)}$. The switching states of three-phase voltage source inverter are as shown in Fig. 2.1. There are eight switching states for inverter among which two are zero states and six other are switching states (- - - and + + +), which short the 3-phase motor terminals. [6]

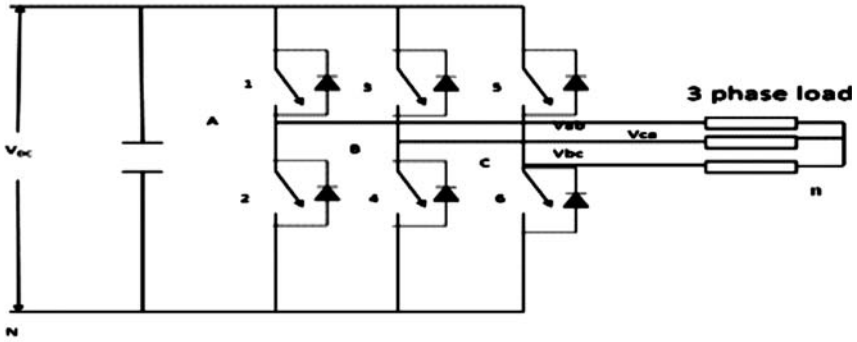

Fig. 1. Power circuit of 2-level VSI.

The other six states, are the active states, produce an active voltage vector each. These active vectors divides the space vector plane into six sectors and are of equal magnitude as shown in Fig. 2. By taking V_{DC} the magnitudes are normalized. In space-vector PWM, for every sub-cycle, Ts, the voltage reference vector is provided by rotating., T_1, T_2, and T_z are dwell times of active vector 1, active vector 2 and zero vector in the sub-cycle are given respectively.

$$T_1 = (V_{ref} * T_s^* \sin(60-\alpha))/(\sin(60°)) \quad (2)$$

$$T_2 = (V_{ref}^* T_s^* \sin(\alpha))/(\sin(60°)) \quad (3)$$

$$T_Z = T_s - T_1 - T_2 \quad (4)$$

By dividing Tz equally between 0 and 7 the switching sequence 0-1-2-7 or 7-2-1-0 in a sub-cycle in sector 1 is employed. However, a multiplicity of sequences are possible since the zero can be applied rather using 0 or 7, and also an active state can be applied more than once in a sub-cycle. The conditions of valid sequence in sector I are as follows.

1. In a sub-cycle, the active state 1 and active state 2 must be applied at once.
2. In a sub-cycle, either zero state 0 or zero state 7 must be applied at once.
3. The total duration for which the active state is applied in a sub-cycle must satisfy above condition (1), in case of multiple actions.
4. The total duration for which the Zero vector (either using the zero
4. State 0 or the zero state 7) is applied in a sub-cycle must satisfy above condition (1).
5. For a state transition, only one phase must switch.
6. In a sub-cycle total number of cycles must be less than or equal to three.

Volt-second balance is ensured by conditions 1 to 4.Unwanted switching's are avoided which is used to keep the switching losses low by using condition 5.The average switching frequency is ensured by condition 6 which is less than that of CSVPWM for a given sampling frequency. The applied inverter states are 0, 1, 2, or 7 at any arbitrary instant in sector I.

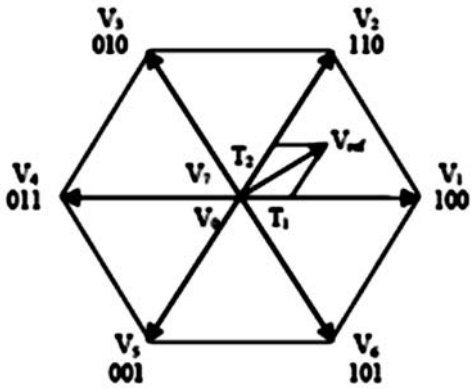

Fig. 2. The discrete phase voltage space vector positions.

Table 2. Different switching states with phase voltage values.

State	*Switch on*	*VA*	*VB*	*VC*
1	1,4,6	(2/3)VDC	-(1/3)VDC	-(1/3)VDC
2	1,3,6	(1/3)VDC	(1/3)VDC	-(2/3)VDC
3	2,3,6	-(1/3)VDC	(2/3)VDC	-(1/3)VDC
4	2,3,5	-(2/3)VDC	(1/3)VDC	(1/3)VDC
5	2,4,5	-(1/3)VDC	-(1/3)VDC	(2/3)VDC
6	1,4,5	(1/3)VDC	-(2/3)VDC	(1/3)VDC
7	0	1,3,5	0	0
0	2,4,6			

The switch state of inverter legs in the figure is indicated by the binary number. 1 implies upper switch being on and 0 refers to the lower switch of the leg being on. The most significant bit is for leg A, the least significant bit is related to leg C and the middle is for leg B. We now focus on the effective voltage that makes an actual power flow between inverter and load. When the switching state of each phase becomes 0 to 1at different times during one sampling interval, an effective voltage is applied to the load side. TS denote the sampling time and Teff denotes the time duration in which the different voltage is maintained.

$$T_{as} = (T_s/V_{dc})*V_{as}^*$$
$$T_{bs} = (T_s/V_{dc})*V_{bs}^*$$
$$T_{cs} = (T_s/V_{dc})*V_{cs}^*V_{as}^* ,V_{bs}^*, V_{cs*} \quad (5)$$

are the A-phase, B-phase, and C-phase reference voltages. This switching time could be negative in case where negative phase voltage is commanded. Therefore, this time is called the "imaginary switching time". Now the effective time can be defined as time duration between the smallest and the largest of three imaginary times, as given by

$$T_{eff} = T_{max} - T_{min} \quad (6)$$

Where

$$T_{max} = \max(T_{as}, T_{bs}, T_{cs}) \quad (7)$$
$$T_{min} = \min(T_{as}, T_{bs}, T_{cs}) \quad (8)$$

When actual gating signals for power devices are generated in the PWM algorithm, there is one degree of freedom by which effective time can be reallocated anywhere within the sampling interval. Therefore, a time-shifting operation will be applied to the imaginary switching times for each inverter arm. This is accomplished by adding Toffset to the imaginary times.

$$T_{ga} = T_{as} + T_{offset},$$
$$T_{gb} = T_{bs} + T_{offset},$$
$$T_{gc} = T_{cs} + T_{offset} \quad (9)$$

This gating time determination is only performed for the sampling interval in which all of the switching states of each arm go to 0 from 1. This interval is called "OFF SEQUENCE." In order to generate a symmetrical switching pulse pattern within two sampling intervals, the actual switching time will be replaced by the subtraction value, with sampling time as follows

$$T_{ga} = T_s - T_{ga},$$
$$T_{gb} = T_s - T_{gb} \quad (10)$$
$$T_{gc} = T_s - T_{gc} \quad (11)$$

To guarantee the full utilization of dc-link voltage, the actual gating times should be restricted to a value from 0 to TS as follows

$$0 \leq T_{min} + T_{offset},$$
$$T_{max} + T_{offset} \leq T_s \quad (12)$$

The range of available offset time can be calculated as follows

$$T_{offset\ min} \leq T_{offset} \leq T_{offset\ max} \quad (13)$$

Where $T_{offset\ min} = -T_{min},$

$$T_{offset\ max} = T_s - T_{max.} \quad (14)$$

Therefore $T_{offset} = .5T_0 - T_{min},$

$$T_0 = T_s - T_{eff} \quad (15)$$

3. DIFFERENT TYPES OF PWM STRATEGIES

3.1. Conventional SVPWM technique

In this technique when the reference vector is in first sector, the conventional switching sequence (0127 – 7210) is used for two alternate samples. In Fig.3. the switching sequence 7210 is shown where dark region indicates for ON state and light region for OFF state of the given switch.

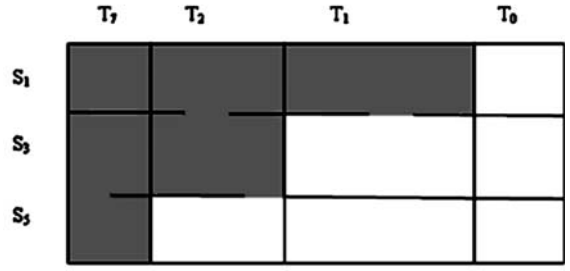

Fig. 3.

3.2. Symmetric aligned switching sequence of SVPWM

In this type of PWM technique the switching sequence (0127210) is used in one sampling period in sector I as shown in Fig. 4. The zero states are used first, last and middle of the sampling period.[3]

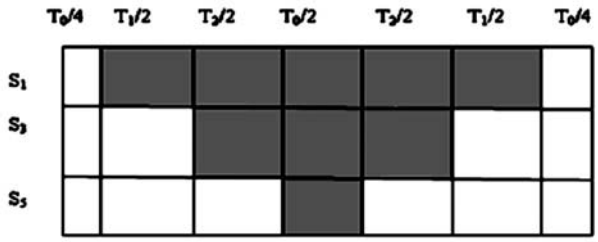

Fig. 4.

3.3. Alternate switching sequence of SVPWM

In this PWM technique the switching sequence (127 - 721) is used in sector I. the switching vectors in the remaining sectors is shown in table in previous chapter. Fig. 5 shows the switching sequence 127 in sector. [5]

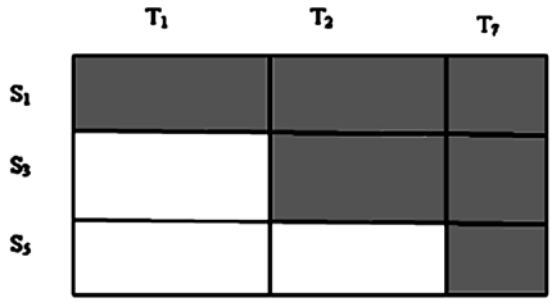

Fig. 5.

Three zone hybrid PWM technique: In this PWM technique each sector is divided into four sectors equally and different switching sequence is used in each division. In first sub-division switching sequence (1012 - 2101) is used, and in middle two sub-divisions switching sequence (0127 - 7210) is used, and In last sub-division switching sequence (2721 - 1272) is used as shown in Fig. 6.

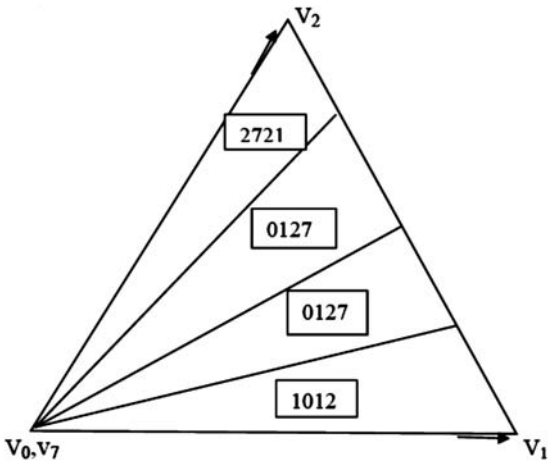

Fig. 6.

3.5. Basic Bus Clamping Strategy

PWM waveforms with P = 5, 9, 13, 17….. (P – Pulse number), preserving the waveform symmetries can be produced by developing bus clamping strategy which is the main objective of BBCS. The pulse number P is equal to total number of switching's of the three phase or the number of state transitions within a sector. At least one switching of the unclamped phase and one switching will generate an arbitrary sample. The needed clamped phase is equal to total number of switching's of the three phase or the number of state transitions within a sector. At least 2N switching's are required for N samples per sector. At least one extra switching is required to change the zero state used once in every sector. For maintaining the waveform symmetries the minimum value of P required to generate N samples per sector is P = (2N + 1). If P = 5, 9, 13, 17… and P = 2N + 1, then N must be even for this strategy [4].

3.6. Boundary Sampling strategy

Only one active vector is needed to generate a sample on a sector boundary n this strategy. Using the sequence 010 or 101, with either T_0 or T_1 is divided into two equal halves, a sample on the boundary between sector VI and I is generated. It is known as "boundary sample," and the sequence as "boundary sequence". On every sector boundary there is a sample, and the zero-changing is done as in BBCS.[7]

4. SIMULATION STUDY AND RESULTS

All the six PWM techniques are implemented in MATLAB 2008a version. The block diagrams of simulation model are shown in Fig. 7, Fig. 8. The results of the simulation of simulation are provided in next chapter and comparison of different PWM techniques is done.

4.1. Simulation Block Diagram for conventional SVPWM and Symmetric and Alternate sequence SVPWM techniques:

To simulate Conventional, Symmetric sequence and alternate sequence SVPWM techniques below shown SIMULINK model is used in MATLAB. The different blocks in this model are 3-phase sine generator, Toffset calculation and voltage measurement blocks. The simulation of these techniques has done by taking sampling time of 2 msec.

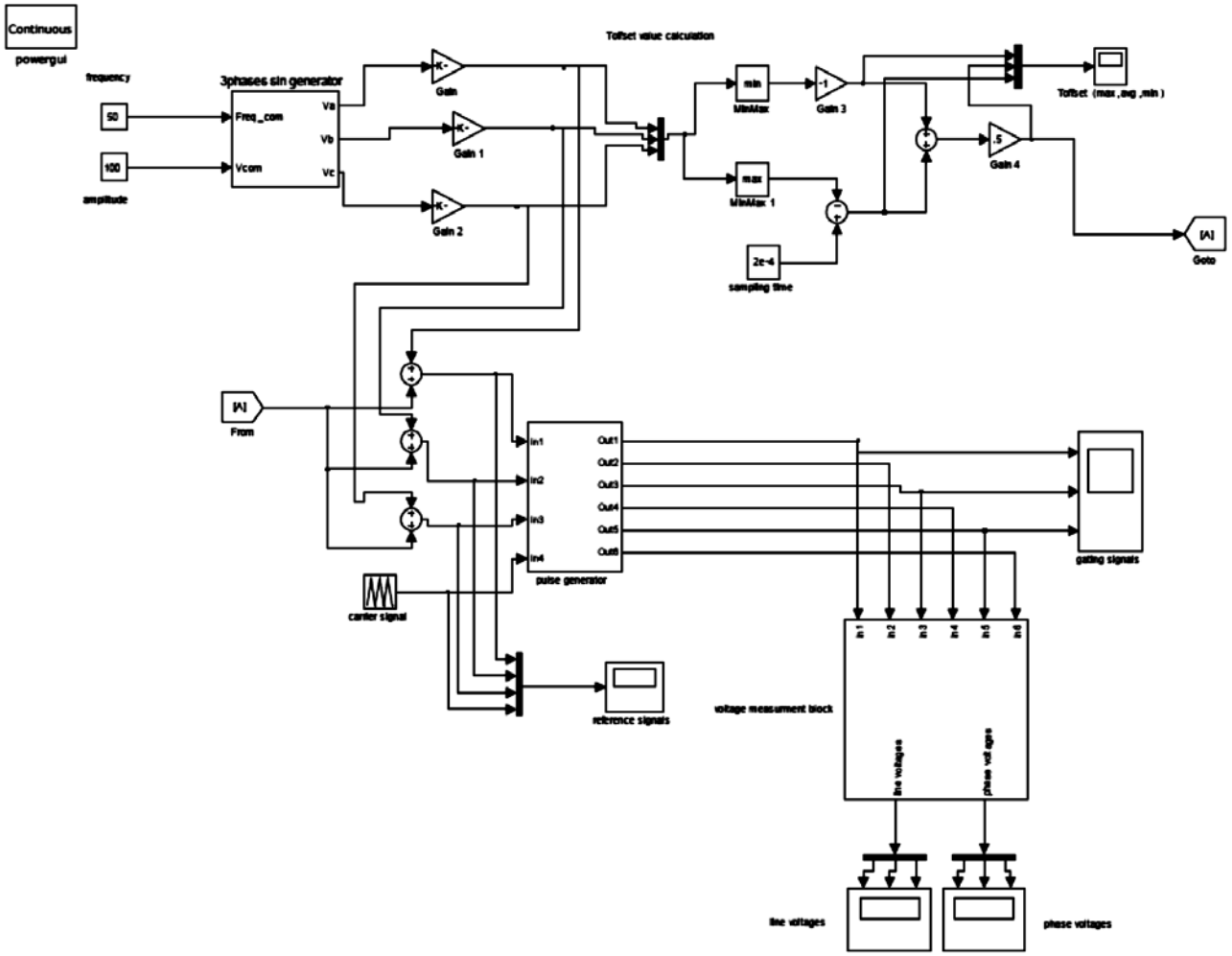

Fig. 7. Simulink model.

4.2. Simulation Block Diagram for hybrid SVPWM, BBCS and BSS PWM techniques

To simulate of the Basic Bus Clamping strategy and Boundary Sampling Strategy SVPWM techniques above shown SIMULINK model is uesd in MATLAB. In this the first block is used for calculating Vref, sector number and reference angle. The found vref, sector number and vref angle are used for calculating dwell times. Using these dwell times the pulses are given to the mosfets of the inverter power circuit

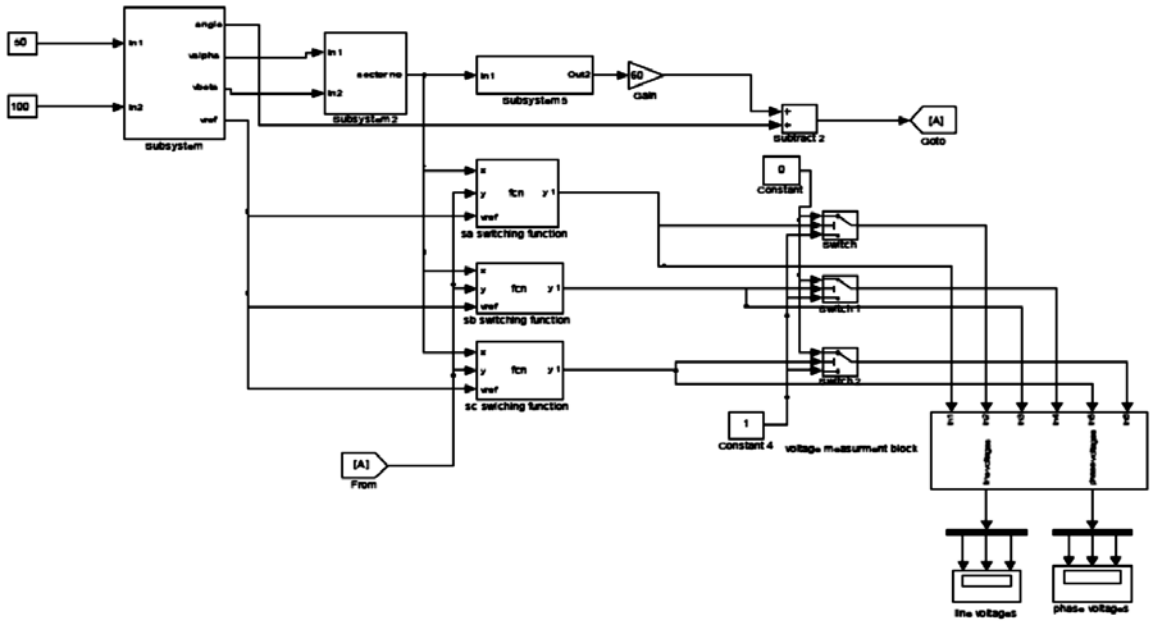

Fig. 8. Simulink model.

4.3. Output line and phase voltages (simulation results)

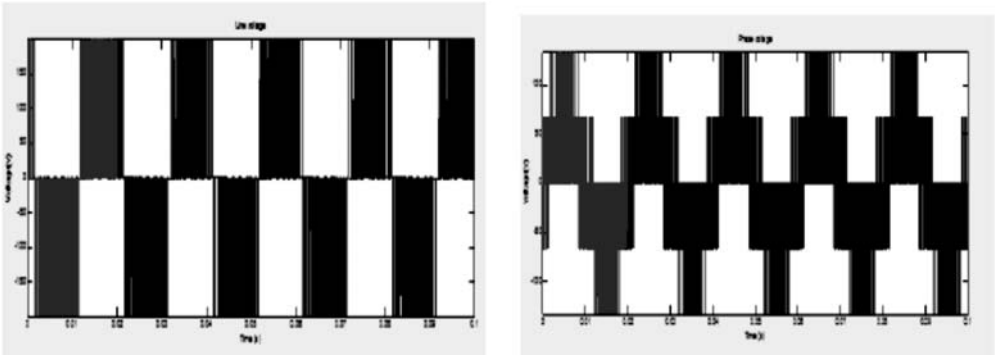

Fig. 9. Line and phase voltages of conventional SVPWM.

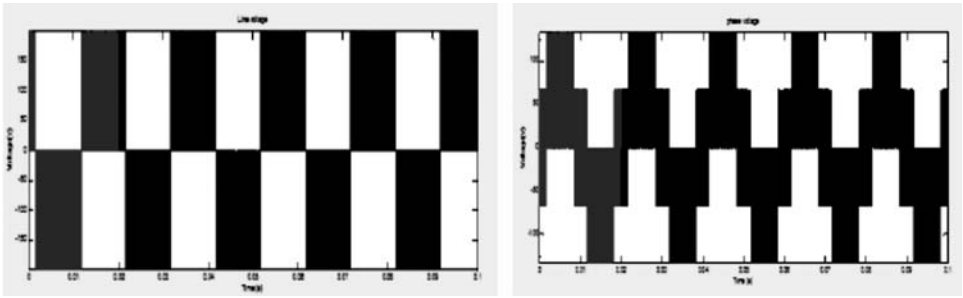

Fig. 10. Line and phase voltages of symmetric aligned sequence SVPWM.

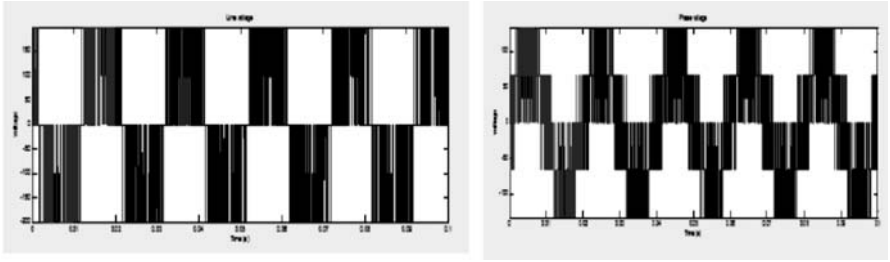

Fig. 11. Line and phase voltages of alternate aligned sequence SVPWM.

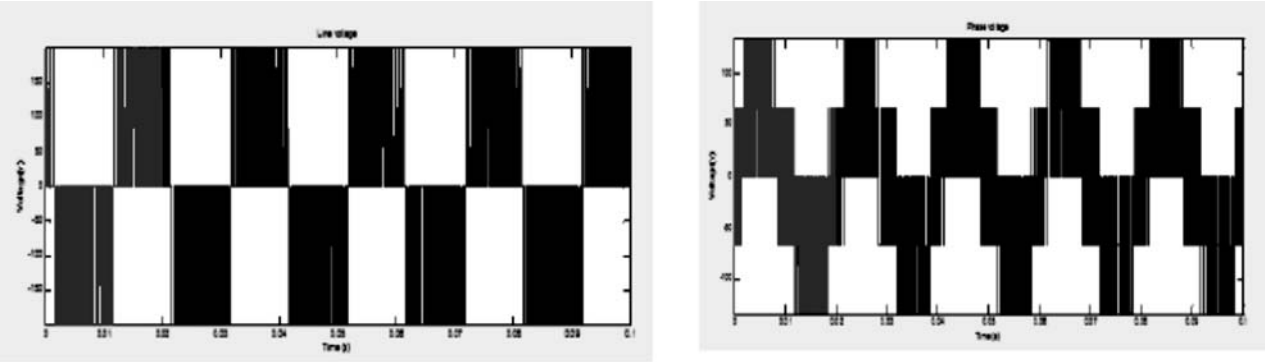

Fig. 12. Line and phase voltages of hybrid PWM technique.

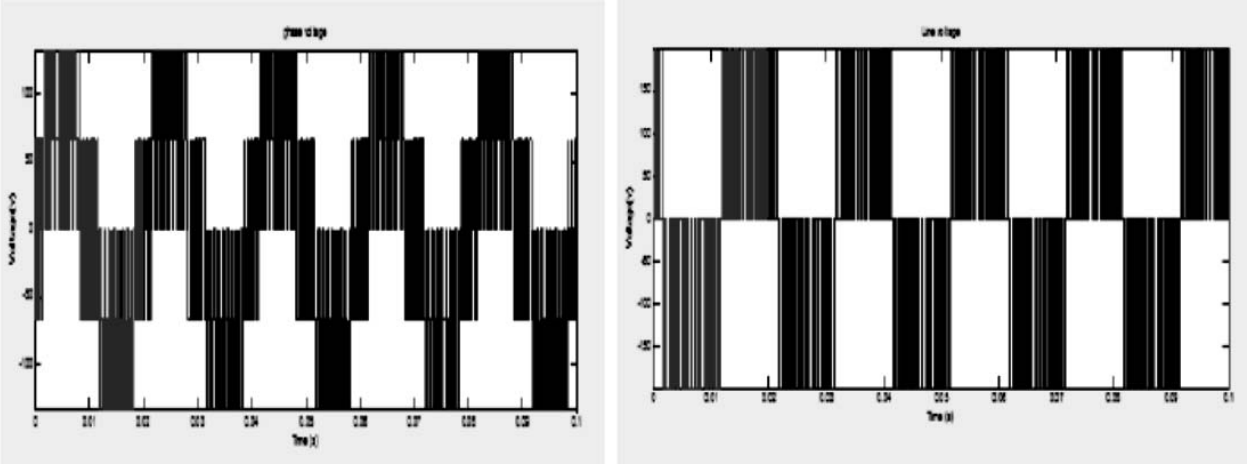

Fig. 13. Line and phase voltages of Basic Bus Clamping Strategy PWM technique.

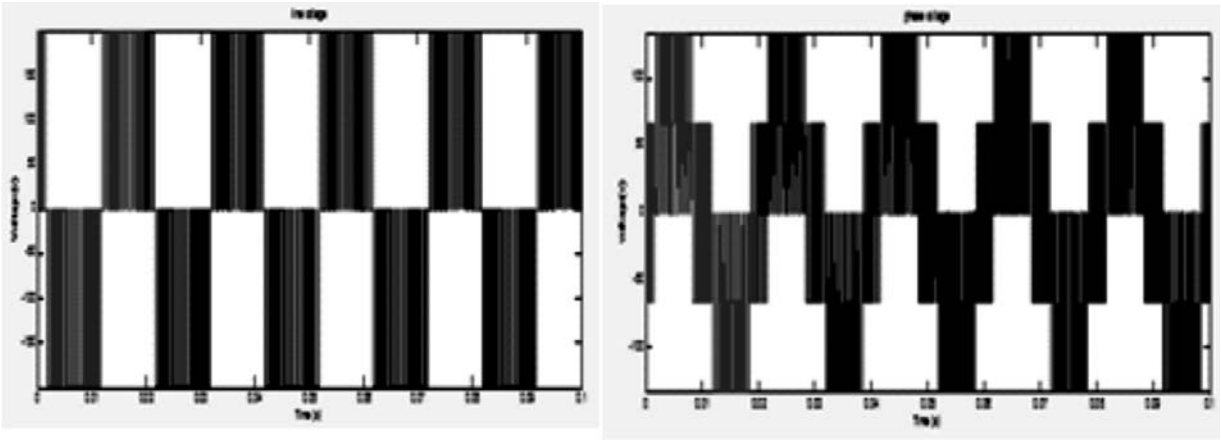

Fig. 14. Line and phase voltages of Boundary Sampling Strategy PWM technique.

4.4. Comparison of Total Harmonic Distortion of the Line voltages (in percentage)

All the six PWM techniques have simulated for different modulation indexes (for linear modulation indexes) and THD are tabulated. The higher order harmonics are high in BBCS and BSS techniques, which can be eliminated easily and in conventional.

All the six PWM techniques have simulated for different modulation indexes (for linear modulation indexes) and THD are tabulated. The higher order harmonics are high in BBCS and BSS techniques, which can be eliminated easily and in conventional SVPWM lower order harmonics are dominant.

Table 4.1. Comparison of Total Harmonic Distortion of the Line voltages.

Modulation index / *Technique*	*.2*	*.3*	*.5*	*.6*	*.8*	*.9*	*1*
Conventional SVPWM	232	181	123	104	76	63	51
Symmetric aligned sequence SVPWM	232	181	123	104	77	63	51
Alternate sequence SVPWM	232	181	123	106	78	63	51
3 zone hybrid PWM	259	202	142	123	94	82	72
Basic bus clamping strategy	256	202	143	124	95	83	72
Boundary sampling strategy	263	207	146	126	96	84	73

4.5. Comparison of the maximum fundamental line voltages (volts)

Table 4.2. Comparison of the maximum fundamental line voltages.

Modulation index / *Technique*	*.2*	*.3*	*.5*	*.6*	*.8*	*.9*	*1*
Conventional SVPWM	39	59	99	120	160	180	199
Symmetric aligned sequence SVPWM	39	60	99	120	159	180	200
Alternate sequence SVPWM	40	59	99	119	159	180	200
3 zone hybrid PWM	36	55	91	110	146	164	183
Basic bus clamping strategy	36	54	91	109	146	164	182
Boundary sampling strategy	34	52	88	106	142	161	179

Comparison of all the six PWM techniques is done by total harmonic distortion of line voltage and maximum fundamental voltage as shown in Table 4.1 and Table 4.2. The above table shows comparison of maximum fundamental voltage for liner modulation index range. The same is implemented in hardware and the results are verified in next chapters.

5. CONCLUSION AND FUTURE SCOPE

5.1. Conclusions

From the simulation results we can conclude the following points :

1. The RMS of output line voltage is maximum for BBCS PWM technique and followed by Conventional SVPWM.
2. The higher order harmonics and even order harmonics are eliminated in BBCS and not in Conventional and Alternative switching sequence SVPWM due to half-wave and quarter-wave symmetry of the output waveforms.
3. The total losses (both switching and conduction losses) in switches are minimum for BBC strategy and followed by 3-zone hybrid and conventional SVPWM techniques (the switching losses are calculated for one sample and compared).
4. Therefore we can conclude that the Basic Bus Clamping Strategy is the best PWM method when compared to other three PWM techniques.

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