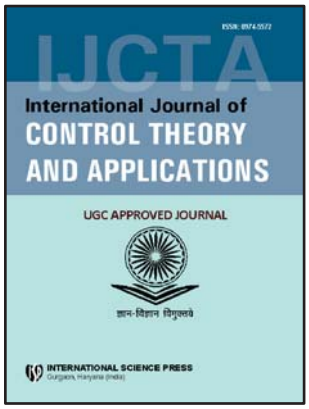

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Design of Cascode Topology Based Doherty Power Amplifier for Wireless Applications

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Abstract : The key role of the Power Amplifier (PA) in RF transmitter is to exhibit high output power. This paper presents design and comparison of cascode topology based Class AB PA and Doherty PA using 180nm CMOS technology. The input and output matching device is designed using Pi type matching network. The result shows that power amplifier achieves output power of 18.298 dBm at 2GHz cut off frequency. Further this amplifier has been combined with a Class C amplifier to produce an amplifier called as Doherty Power Amplifier. The comparison result shows that Doherty Power Amplifier achieves output power of 48.131 dBm. It amplifies signals effectively than Class AB power amplifier. These are implemented using Agilent Advanced Design System (ADS) simulation tool.

Keywords: *Power amplifier, Doherty, Cascode, Efficiency.*

1. INTRODUCTION

Power Amplifier is the most energy consuming block inside the RF transceiver. Therefore performance improvement is a critical point. In CMOS power amplifiers the main non-linearity is due to the non linear gate to source capacitance (Cgs), intrinsic non linear transconductance [1-2].The other non-linearities resulting from drain junction capacitor and output conductance can be neglected. Mostly power amplifiers use common drain and common source topology [3-4]. In this paper cascode topology is used to design a Class AB amplifier. The cascode topology is used as it provides good isolation with respect to the impedance effects at output and input. The supply voltage VDD can be increased to produce higher output power levels by dividing the voltage swing equally between the cascode transistors. This prevents the device from any damage. Also the voltage swing can be unequally divided between common gate and common source transistor. This leads to a higher PAE performance level. Further in this paper cascode structure is used to design a Class C amplifier and these two amplifiers are combined together to produce a system which has enhanced efficiency to about 55-64%. This combined structure using two parallel amplifiers is called as 'Doherty Power Amplifier'. One amplifier is called as Carrier or main amplifier biased in Class AB and the other one is called as peaking or auxiliary amplifier biased in Class C.The two power amplifiers are connected on the DPA structure using a power splitter. The power splitter is implemented with the help of 3dB Coupler. The output of both the amplifiers are combined with the help of impedance inverter which ties main amplifier output to auxiliary amplifier and impedance transformer on the output. The impedance inverter is implemented with the help of microstrip line. Doherty power amplifier is efficient and can achieve very high linearity, so can be used in base station [5-6]. The proposed design is simulated in 180nm CMOS technology using ADS software tool.

2. DESIGN AND ANALYSIS OF CLASS AB POWER AMPLIFIER CIRCUIT

The power amplifier has been designed using cascode topology biased in Class AB. The gate to source voltage is 2.9 and drain voltage is 1.8V. The input and output resistance can be calculated from the following equivalent circuits as shown in Fig.1 and Fig.2 below:

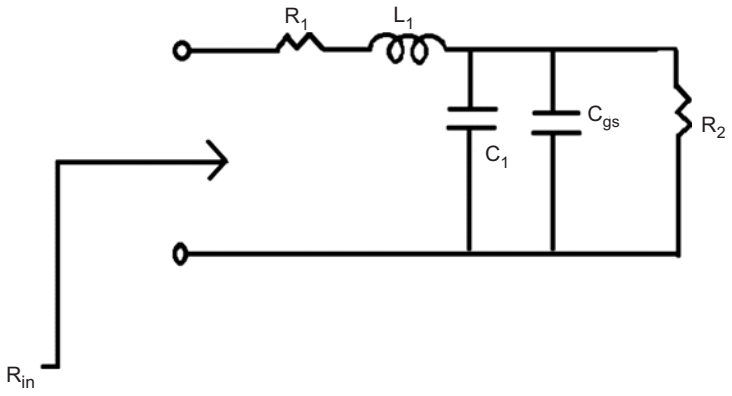

Figure 1: Equivalent circuit (input)

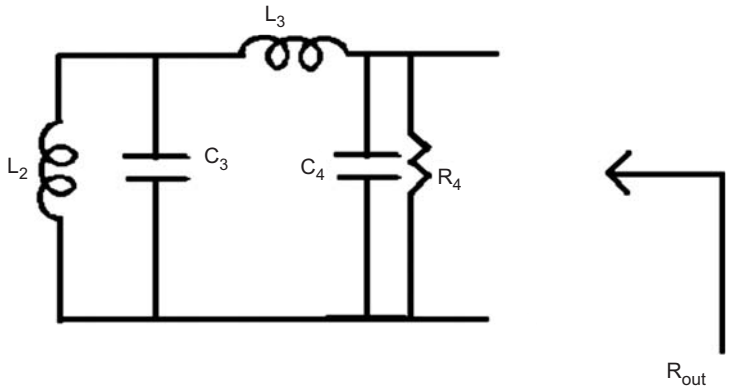

Figure 2: Equivalent circuit (output)

The output resistance of the circuit is described in the following equation

$$R_{out} = \frac{R_4(w^2L_2C_3+1)}{w^2L_2C_3+1} \quad (1)$$

The overall voltage gain of the circuit can be calculated from equation (2)

$$g_m R_{out} \quad (2)$$

The input and output matching network is designed using Pi type matching network as shown in Fig.3:

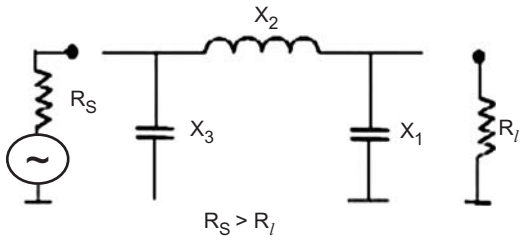

Figure 3: Pi matching network

This circuit can be represented as two L circuits connected together through their shunt component as shown in Fig. 4 below. The imaginary resistor R_x has to be larger than both resistors R_S and R_l.

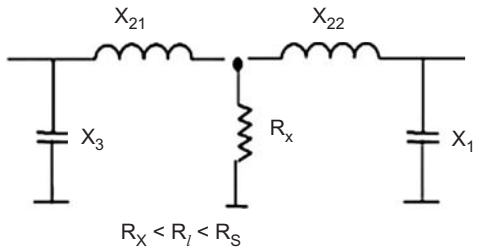

Figure 4: P*i* network with imaginary resistor R_x

Quality factor can be described as

$$Q = \sqrt{\frac{R_S}{R_X} - 1} \tag{3}$$

The values of L and C components can be calculated from the following equations:

$$X_1 = \sqrt{\frac{\frac{R_S}{R_l}}{Q^2 + 1 - \frac{R_S}{R_l}}} \tag{4}$$

$$X_2 = \frac{QR_S - R_l\frac{R_S}{X_1}}{Q^2 + 1} \tag{5}$$

$$X_3 = \frac{-R_S}{Q} \tag{6}$$

The overall voltage gain of the circuit is 9.416dB shown in Fig.5:

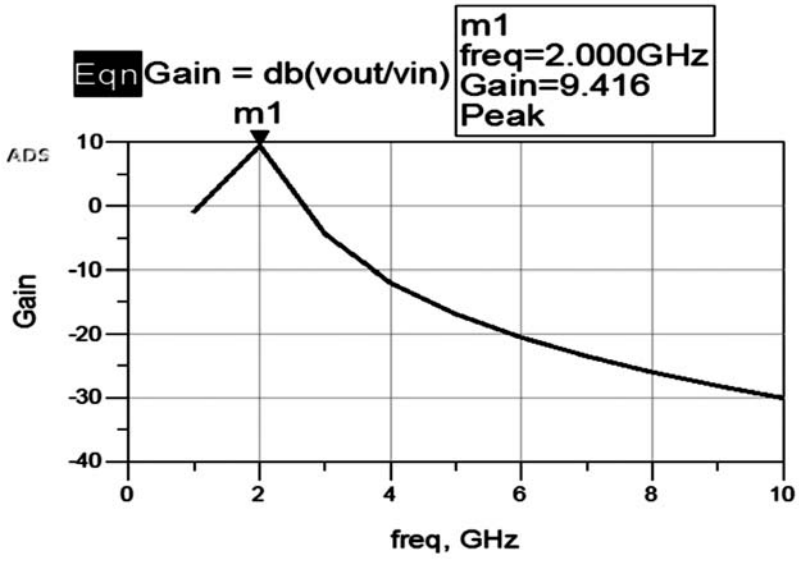

Figure 5: Gain vs. Frequency

The S parameter simulation results are shown below:

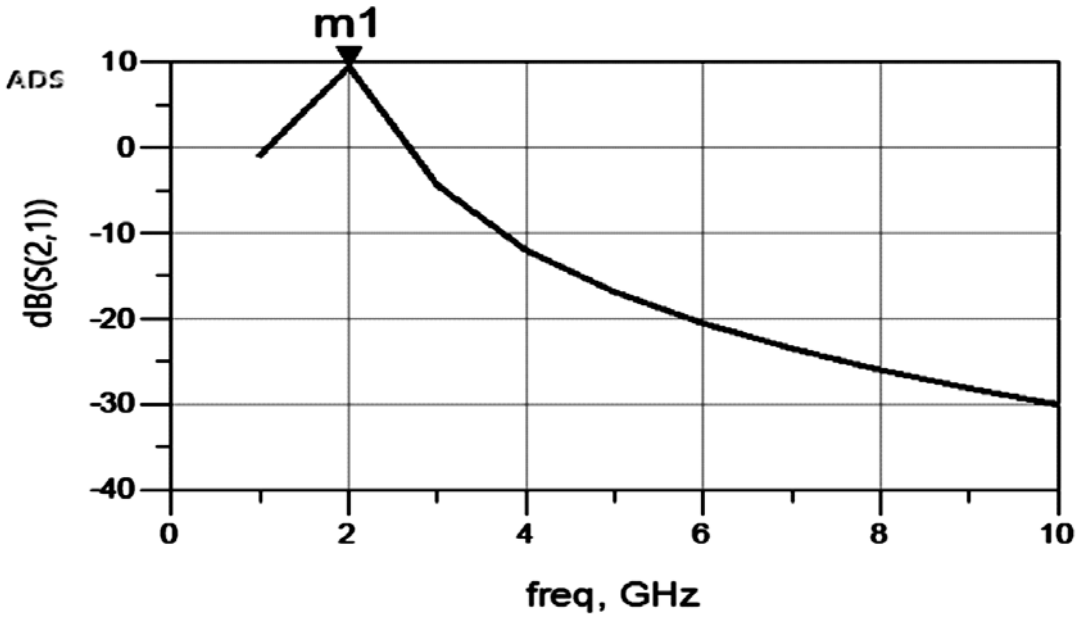

Figure 6: S (2, 1) vs. Frequency

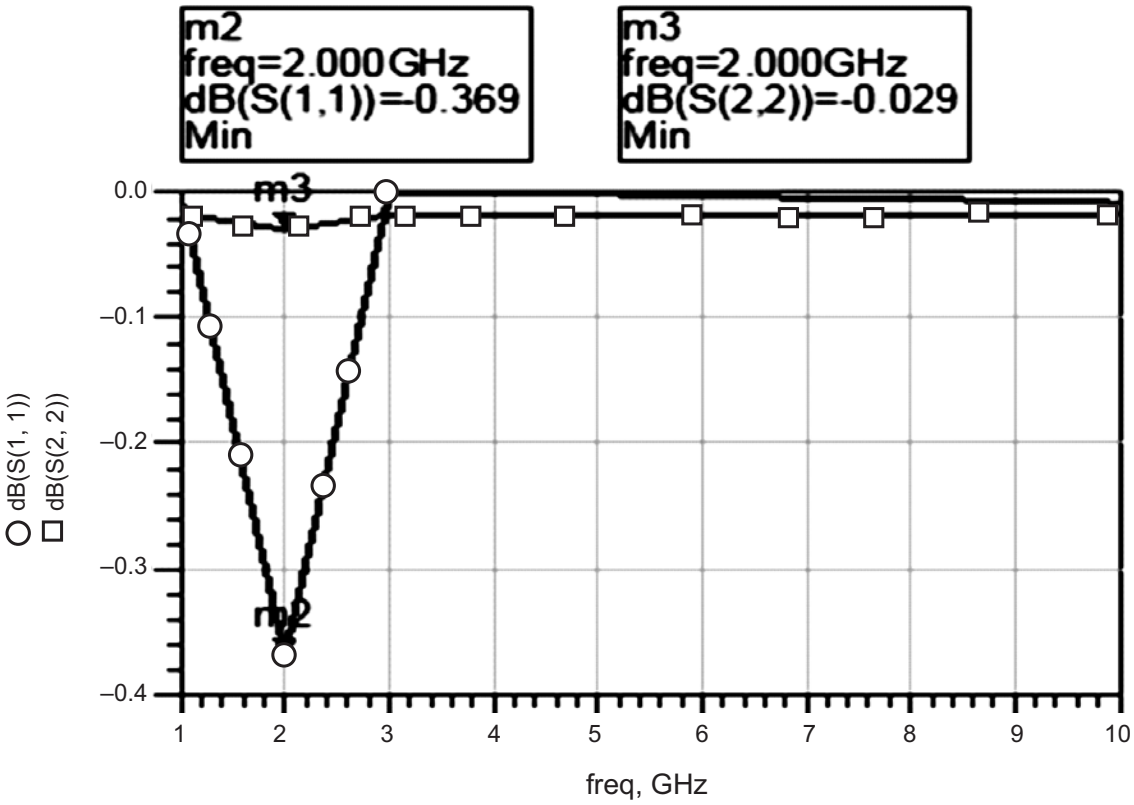

Figure 7: S (1, 1) dB, S (2, 2) dB vs. Frequency

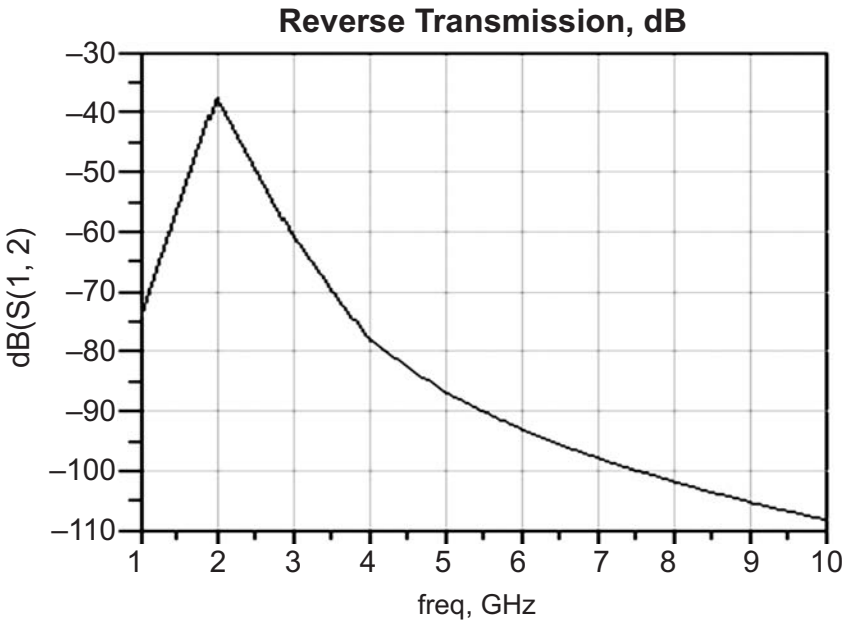

Figure 8: S (1, 2) dB vs Frequency

With the help of S parameter simulation we can obtain forward transmission gain 9.416dB. The input and output transmission coefficient is -0.369dB and -0.029dB respectively.

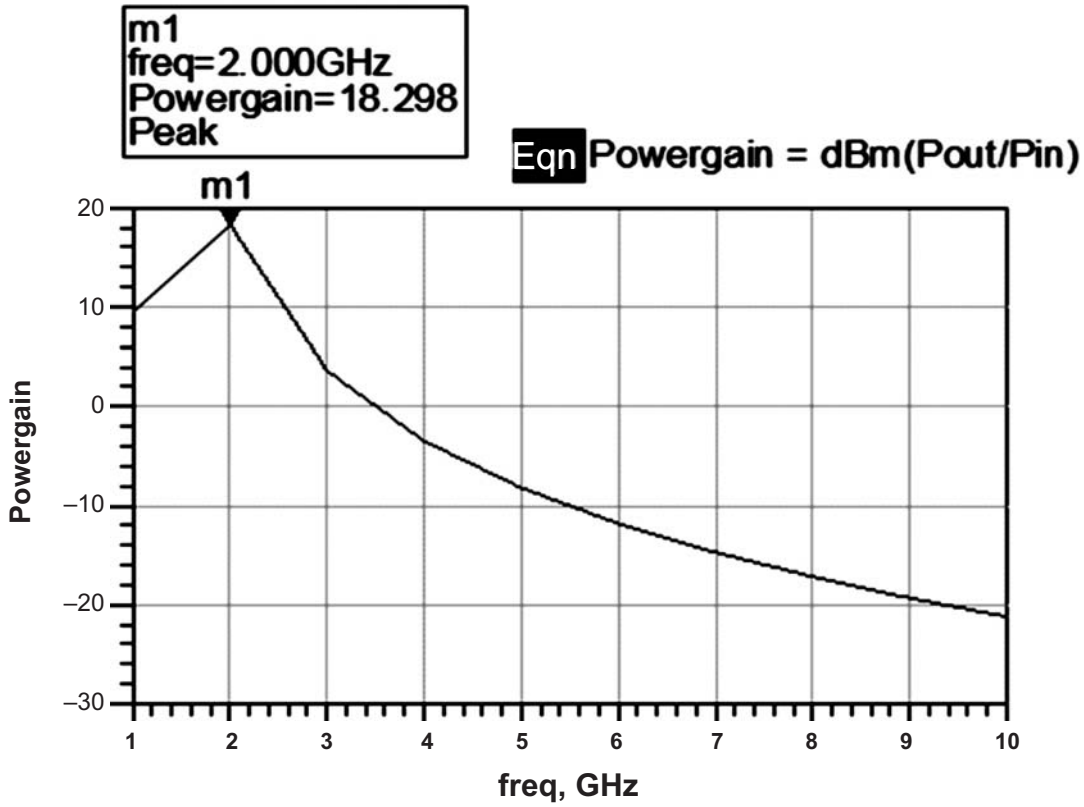

Figure 9: Power gain vs Frequency

The power gain of the circuit obtained is about 18.298dBm as shown above in Fig.9

The complete schematic is shown in Fig.10

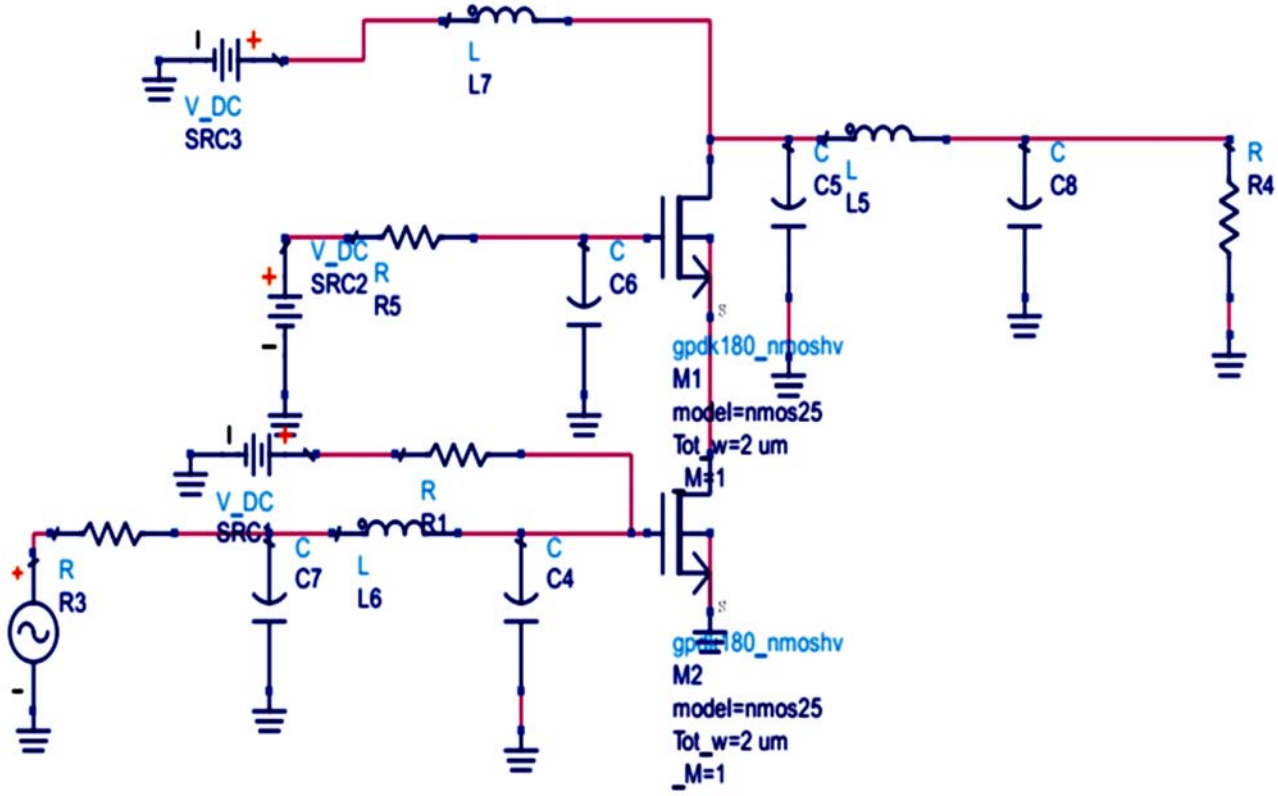

Figure 10: Complete schematic of Class AB power amplifier

3. DESIGN OF DOHERTY POWER AMPLIFIER

The increased use of Doherty power amplifier is due to the need to maintain amplifier efficiency and also due to the increasing peak to average power ratios found in new modulation format. When a signal modulator with an amplitude component is applied to a conventional PA, amplitude distortion occurs. When PAPR ratio increases amplifier has to accommodate the peaks while running at a low average power level. So this situation is overcome in Doherty power amplifier. It is able to accommodate signals with higher PAPR ratios.

In addition to power amplifier it consist of combiner which matches the signals in phase between two halves such that both signals are added together to produce required output. Therefore the overall gain of the circuit is much greater than a conventional power amplifier.

The proposed DPA consists of three parts i.e. design of sub power amplifiers, design of 3db Coupler and the design of combining network. The power splitter is implemented with the help of 3dB Coupler. The power splitter is designed with the objective of dividing input power equally and reducing the losses as maximum as possible. There are two power amplifiers used in the design. The main amplifier is biased in Class AB and the auxiliary amplifier is biased in Class C. The cascode topology is used for the design. The bias voltage of common gate is normally greater than common source amplifier. The drain voltage of main amplifier biased in Class AB and auxiliary amplifier biased in Class C is 20V and 6V respectively. The gate to source voltage is 3V for main amplifier and 0.4V for auxiliary amplifier. The input and output matching device is designed using L type matching network which consist of an inductor and capacitor. It can be designed either by using LC or CL matching network depending on downward and upward transformation.

The output of both the amplifiers are combined with the help of impedance inverter which ties main amplifier output to auxiliary amplifier and impedance transformer on the output. In the proposed design impedance inverter is implemented with the help of microstrip line. The impedance transformer converts 50ohm load to 25ohm on input side. As the main amplifier saturates, its output impedance begins to drop. The impedance inverter converts main amplifier output impedance to a high value, thus allowing auxiliary amplifier to pump power into load. Therefore, impedance inverter in a way transforms saturated main amplifier into a current source. Both the amplifiers behave as two parallel current sources, thus providing power to output network.

The overall schematic and simulation results are shown in Fig.11 below:

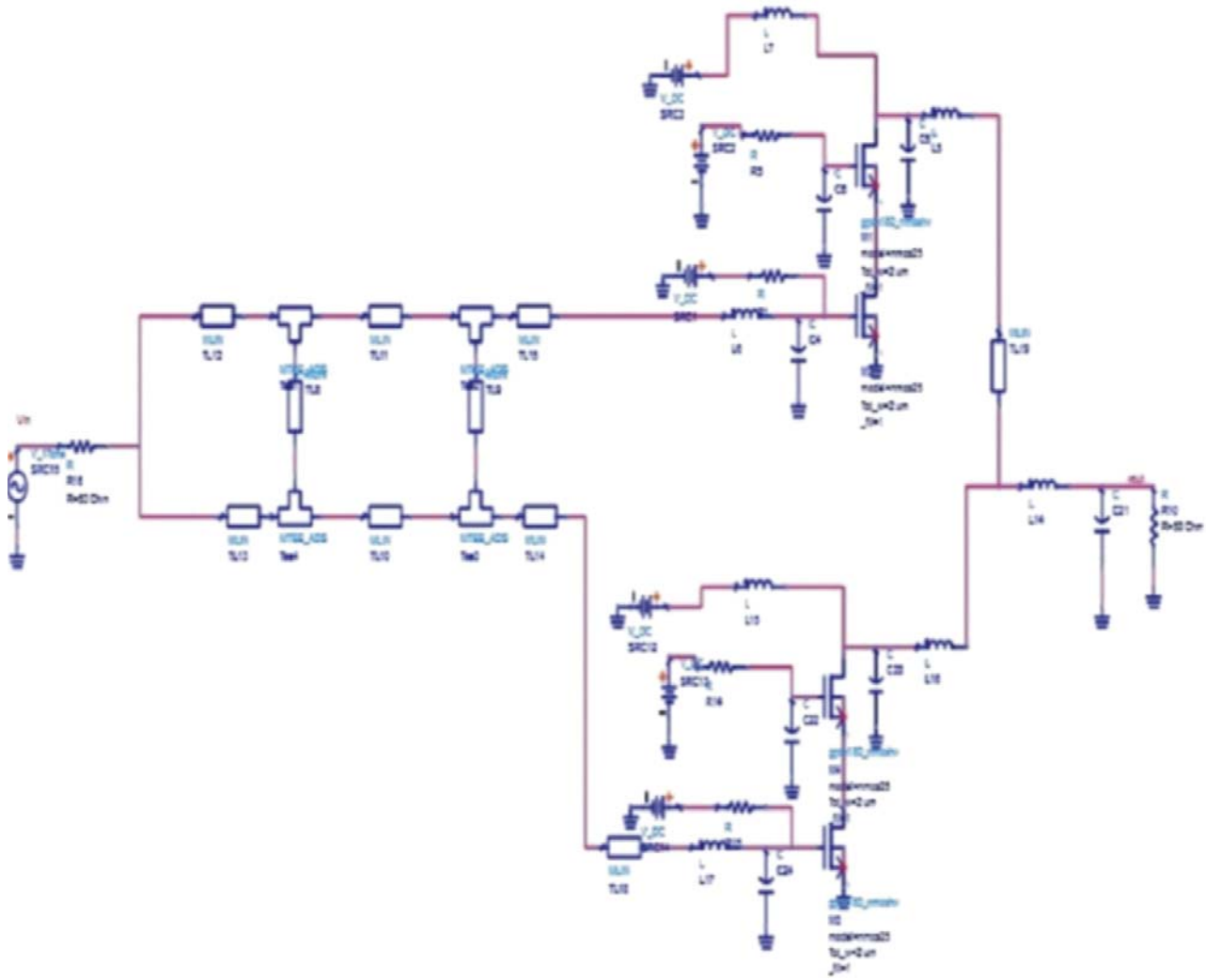

Figure 11: Schematic of proposed Doherty power amplifier

The overall voltage gain of the circuit is 30.343dB shown in Fig. (12).

The measurement result shows that the proposed circuit achieves output power of 20dBm to 48dBm in the frequency range 1.5-2GHz. Fig. (13).

The table shown below describes the comparison between the two types of amplifiers proposed in this paper *i.e*. between Class AB power amplifier and Doherty power amplifier.

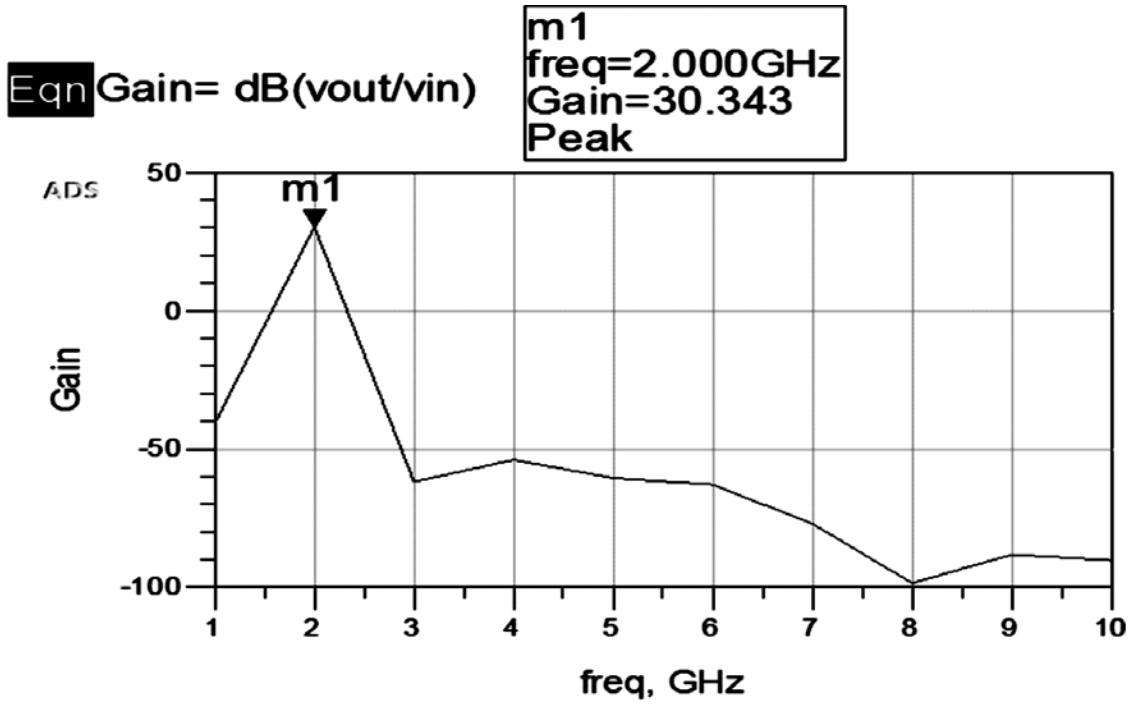

Figure 12: Gain vs. Frequency

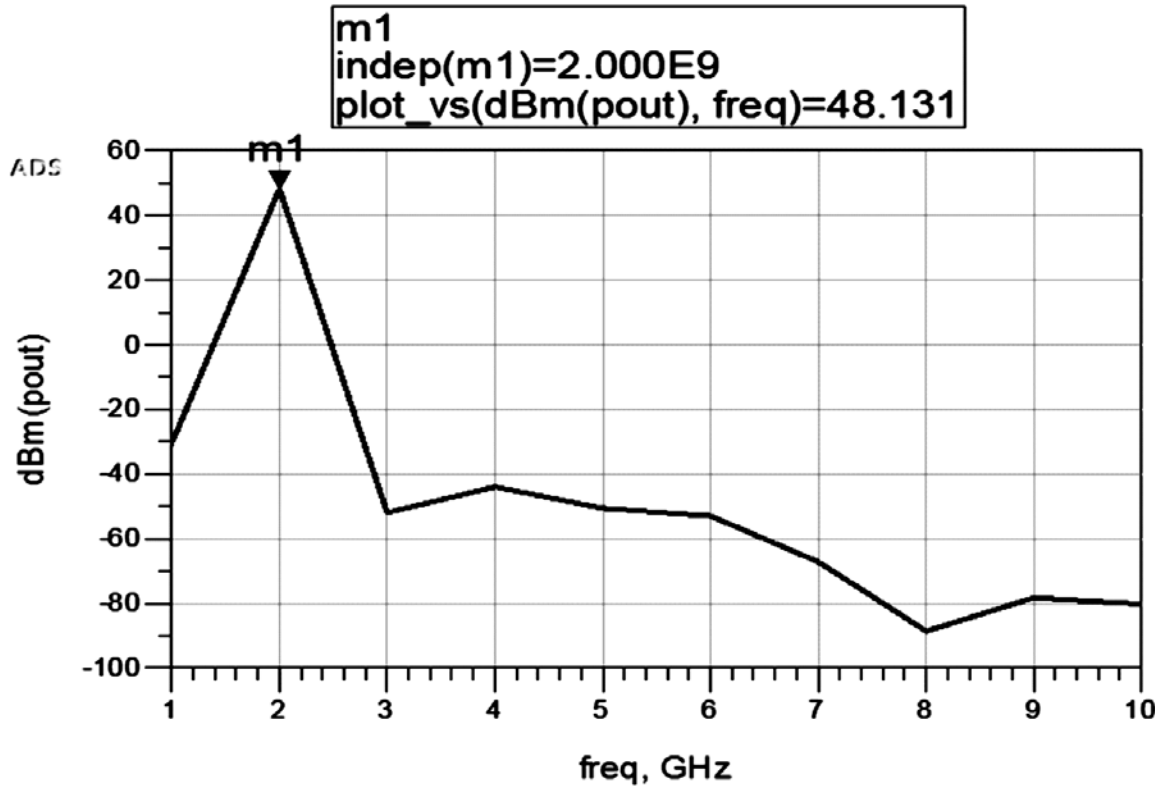

Figure 13: Pout (dBm) vs. Frequency

Table 1
Table of comparison

Type	*Frequency (GHz)*	*Gain (dB)*	*Pout (dBm)*	*Efficiency (%)*
Class AB PA	2	9.416	18.298	40-42
DPA	2	30.343	48.131	55-64

4. CONCLUSION

The result shows that PA achieves output power of 20dBm at 2GHz cut off frequency. The comparison result shows that Doherty Power Amplifier achieves output power of 48.13dBm at cut off frequency. It amplifies signals effectively than a Class AB power amplifier. The efficiency achieved is around 55-64% which is greater than Class AB power amplifier (40-42%). Both the designs have been simulated and implemented in ADS software tool using CMOS technology.

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