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FPGA Based Design and Implementation of Low Cost High Performance Generalised Cascaded Asymmetric Multilevel Inverter

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ABSTRACT

In this work, initially a new topology for sub multilevel inverter is introduced and then series connection of the sub multilevel inverters is developed as a generalized fifteen level multilevel inverter. This multilevel inverter has been analyzed in asymmetric conditions with different values of DC sources. This new multilevel inverter topology has the advantage of reduced number of switches compared to a conventional H bridge multilevel inverter. The required gate pulses for the switches are given by level shifted carrier based Pulse width modulation technique. This highly conventional technique is based on the comparison of a sinusoidal reference with carrier signals. This modulation scheme for generating gate pulses for the switches is implemented using Spartan 6 FPGA processor. The main advantage of this is the ability to generate SPWM waveform in real time using control algorithm in the FPGA processor. This reduces the computational time required to determine the switching times for inverter legs, making the system more suitable for real time implementation for larger drives. It also focuses on getting a more output voltage level with reduced number of switches. The multilevel inverter is simulated using MATLAB/ SIMULINK software for fifteen levels of step voltages with different DC sources and implemented with both R and RL loads and power quality analysis has been done.

Keywords: Pulse Width Modulation, Field Programmable Gate Array, Total Harmonic Distortion, DSO

1. INTRODUCTION

In recent years, industry has demanded for high power equipment's, which today reaches to megawatts. Adjustable ac drives which operate in high power range are usually connected to the medium voltage network. Hence, medium and high voltage ac drive systems have been considered widely [1].

Power electronic converters are becoming more and more popular for various industrial applications. To overcome the limitation of semiconductors current and voltage ratings in high power applications, series and parallel connection of switch is often considered an effective solution [2].In addition, stepped waveform in the output of inverter has better harmonic spectrum than 2-level waveform in low switching frequencies. The switching frequency is restricted by switching losses in high power and high voltage applications, multilevel inverters have found wide acceptance as they can achieve a low harmonic component with low switching frequency [3]. Furthermore, low blocking voltage by switching devices is the other advantage of this type of converters as well as minimum harmonic distortion and switching losses.

Multilevel inverters are mainly utilized to synthesize a desired voltage wave shape from several levels of dc voltages [4]. Their main advantaged are low harmonic distortion of the generated output voltage, low electromagnetic emissions, high efficiency capability to operate at high voltages and modularity [5]. Among

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the different solutions available for multilevel converters, the asymmetric topologies allow to generate more voltage levels with less number of semiconductors and thus increase of output performance and system reliability. For these reasons, this kind of topology has attracted a lot of attention both from the customers and from the manufacturers. Multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium-voltage energy control. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms [6]. By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic distortion. However, a larger number of levels increase the number of devices that must be controlled and the control complexity [2]. The asymmetric multilevel inverters provide a large number of output steps without increasing the number of DC voltage sources and components [5]. Multilevel inverters produce a stepped output phase voltage with a refined harmonic profile when compared to a two-level inverter [6]. The concept of multilevel inverters, introduced to perform power conversion in multiple voltage steps to obtain improved power quality, lower switching losses, better electromagnetic compatibility, and higher voltage capability.

2. LITERATURE SURVEY

Rodriguez et al. [7] (2002) presents the most important topologies like diode-clamped inverter (neutral-point clamped), capacitor-clamped (flying capacitor), and cascaded multi cellular with separate dc sources. Emerging topologies like asymmetric hybrid cells and soft-switched multilevel inverters are also discussed. This paper also presents the most relevant control and modulation methods developed for this family of converters like multilevel sinusoidal pulse width modulation, multilevel selective harmonic elimination, and space-vector modulation. The need of an active front end at the input side for those inverters supplying regenerative loads is also discussed, and the circuit topology options are also presented. This paper has provided a brief summary of multilevel inverter circuit topologies and their control strategies.

Babaei [1] (2008) introduces a new multilevel converter topology that has many steps with fewer power electronic switches. The proposed circuit consists of series-connected sub multilevel converters blocks. The optimal structures of this topology are investigated for various objectives, such as minimum number of switches and capacitors, and minimum standing voltage on switches for producing maximum output voltage steps. A new algorithm for determination of dc voltage sources' magnitudes has also been presented. The proposed topology results in reduction of the number of switches, losses, installation area, and converter cost. The operation and performance of the proposed multilevel converter has been verified by the simulation and experimental results of a single-phase 53-level multilevel converter.

Hinago and Koizumi [3] (2010) describe a multilevel inverter which reduces the number of switching devices by switching the dc voltage sources in series and in parallel. It consists of an H-bridge and an inverter which outputs multilevel voltage by switching the dc voltage sources in series and in parallel. The total harmonic of the output waveform is also reduced. The proposed inverter can reduce the number of switching devices compared with conventional multilevel inverters in the same number of output voltage levels.

Boora et al. [2] (2010) explains the output voltage quality of some of the single-phase multilevel inverters that can be improved when their dc-link voltages and regulated asymmetrically. Symmetrical and asymmetrical multilevel diode-clamped inverters have the problem of dc-link capacitor voltage balancing, especially when power factor of the load is close to unity. In this paper, a new single-inductor multi-output dc/dc converter is proposed that can control the dc-link voltages of a single-phase diode-clamped inverter asymmetrically to achieve voltage quality enhancement. The circuit of the presented converter is explained and equations are developed. A control strategy is proposed and explained in details. To validate the versatility of the proposed combination of the suggested dc–dc converter and the asymmetrical four-level diode-

clamped inverter (ADCI), simulations and experiments have been directed. It is concluded that the proposed combination of introduced multi output dc–dc converter and single-phase ADCI is a good candidate for power conversion in residential photovoltaic (PV) utilization.

Nami et al. [5] (2011) described a novel H-bridge multilevel pulse width modulation converter topology based on a series connection of a high-voltage diode-clamped inverter and a low-voltage conventional inverter. This paper presenting the diode-clamped multilevel H bridge cell cascaded with three-level conventional inverters to increase efficiency of converters with high output voltage resolution. A novel dc link voltage rating is proposed for the multilevel diode-clamped and three-level H-bridge inverters to improve the output voltage and current quality by preserving the adjacent switching vectors between all voltage levels. Here, two different methods for the switching states selection are proposed to minimize either losses or THD of voltage in hybrid converters.

Leon et al. (2011) [4] presented a generalized modulation technique for a converter based on a multidimensional control region. Several possible solutions to develop a specific implementation of the modulation method are addressed in order to show the potential possibilities and the flexibility of the proposed technique. In addition, a feed forward version of this technique is also introduced to determine the switching sequence and the switching times, avoiding low harmonic distortion with unbalanced dc voltages.

Mohammad F K and Ebrahim babaei [6] (2013) initially described a new topology for sub multilevel inverter and then series connection of the sub multilevel inverters is proposed as a generalized multilevel inverter. The proposed multilevel inverter uses reduced number of switching devices. Special attention has been paid to obtain optimal structures regarding different criteria such as number of switches, standing voltage on the switches, number of dc voltage sources, etc. The proposed multilevel inverter has been analysed in both symmetric and asymmetric conditions. The simulation results of a 13-level symmetric topology based on the proposed multilevel inverter have been presented. In the case of asymmetric topology, the simulation and experimental results have been presented for a 31-level inverter based on the proposed optimal structure to validate the ability of the proposed topology in generating of desired output voltage.

3. MODULATION SCHEME

In many industrial applications, the output voltage of inverters should be controlled to overcome input voltage changes and meets the need of voltage/frequency control. It is obvious that output voltage harmonics are depended on the selected modulation technique [3]. A high number of semiconductor devices and switching redundancies bring a higher level of complexity in multilevel topologies compared with a two-level inverter [7]. However, this complexity can be used to improve the modulation technique, such as, reducing the switching frequency, minimizing the common-mode voltage or balancing the dc link voltages. Today, there are many modulation techniques for multilevel applications and they can be classified in two main groups, depending on their switching frequency they are fundamental switching frequency, where each inverter has only one commutation per cycle and High switching frequency, where each inverter has several commutations per cycle [3].

Figure1. (a) Shows a 2-level SPWM fundamental, in this figure a reference signal which is usually a sinusoidal waveform, is compared with a carrier signal which is usually a triangular waveform. There are different methods to generate modulation signals. A reference signal is compared to a carrier signal and output state is selected based on which signal is higher at any moment.

This highly conventional technique is based on the comparison of a sinusoidal reference with carrier signals which are usually selected triangular and modified in phase or vertical positions to reduce the output voltage harmonic content. Multilevel PWM is a generalized form of the 2-level PWM applied to

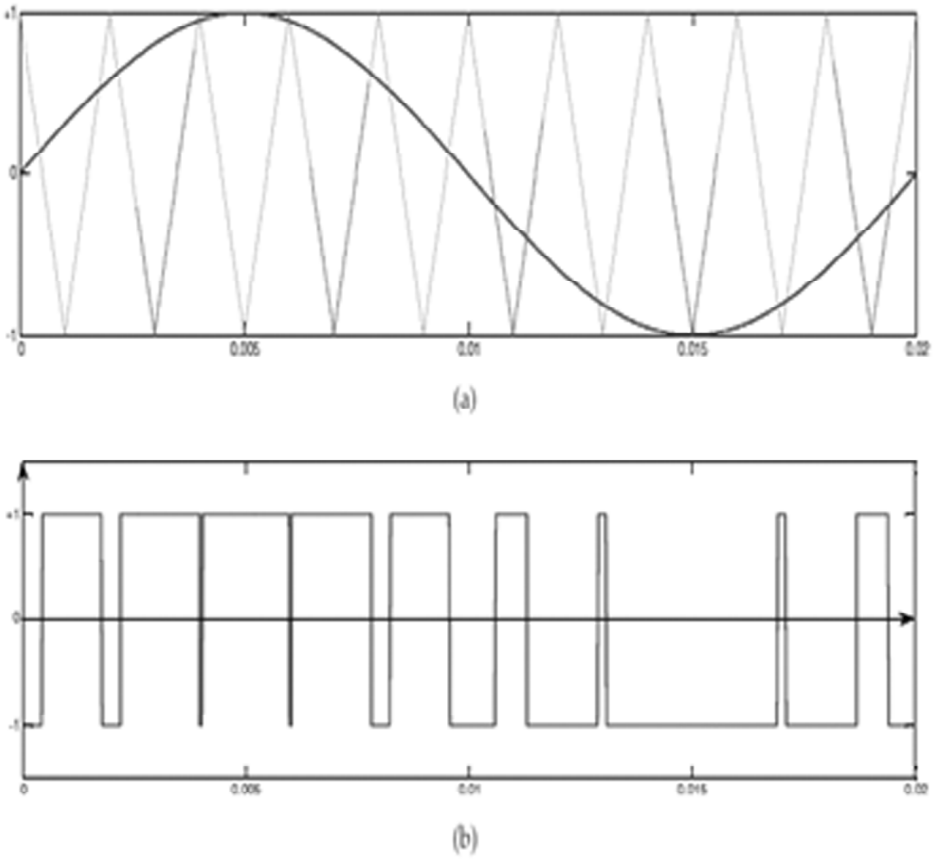

Figure 1: (a) Reference signal and Carrier Signal, (b) Output Voltage

multilevel inverters. Carrier signals in multilevel applications can be in the form of level-shifted to each other or phase-shifted. In level shifted PWM, the carrier signals have the same phase and pick-to-pick amplitude and they are in vertical positions to each other [1]. In phase-shifted PWM the phase of each carrier shifts in a proper angle to reduce the harmonic content of the output voltage. The arrangement that is used generally is triangular waveforms which are level-shifted to each other. The above PWM technique is called Phase Disposition PWM (PD-PWM) [4]. Moreover, the other two modulations are Alternate Phase Opposition Disposition PWM (APOD-PWM) where each carrier signal is out of phase with its neighbor's by 180^0 and the other method is phase opposition Disposition PWM (POD-PWM) where all the carrier signals above zero are in phase and are 180^0 out of phase with those below zero.

IV. PROPOSED DESIGN TOPOLOGY

Multilevel inverters are being used widely in static VAR compensators, active power filters and adjustable speed drives (ASDs) for medium voltage induction motors. Usually the inverters which generate more than two phase potentials are known as multilevel inverters. By increase the voltage levels to infinite value, THD of voltage waveform decreases to zero, since the waveform will be more sinusoidal; but, in practice the accessible voltage level is limited because of voltage unbalancing problems and power losses. In this part, the most important topologies of multilevel inverters and their characteristics will be discussed.

In symmetric topology, the value of the DC voltage sources is equal. However the number of switching devices increases rapidly by increasing the number of output voltage levels. The formula for calculating the number of voltage level (N) in a symmetric multilevel inverter is

$$N = [2(m)\,(n) + 1] \tag{1}$$

Where, m – Number of sub multilevel cells and n– Number of DC sources.

The Figure.2 shows the 13-level inverter based on the symmetric multilevel inverter with Six dc voltage sources each of them 100 V have been used so that the maximum output voltage will be 600 V. Usually in multilevel inverter the number of output voltage levels is odd instead of even. It means that the definition of a zero voltage level in the output of inverter like in 3-level or 5-level inverters makes it more sinusoidal and less harmonics are made. These inverters are known as symmetric multilevel inverters, since their DC link capacitors have the same voltages and all the semiconductor devices should be able to block these voltages in the off state.

Asymmetric multilevel inverters have the same circuit configuration as symmetric ones. The only difference is the voltages. Using different dc link voltages in different power cells and application the appropriate switching methods, the number of output voltage levels increases. Therefore, with less number of H-bridge cells, more output voltage levels can be obtained. It is important to mention that the switches applied in the symmetric inverter have the same off-state voltage, but in the asymmetric inverter, due to different voltage levels of dc link sources, the size of switches can be different.

In asymmetric topology, in order to increase the number of output voltage level, the value of the DC output voltages is selected to be different. The figure 3 shows the asymmetric topology multilevel inverter. The formula for calculating the number of voltage level (N) in an Asymmetric multilevel inverter is

$$N = (2^{n+1} - 1) \tag{2}$$

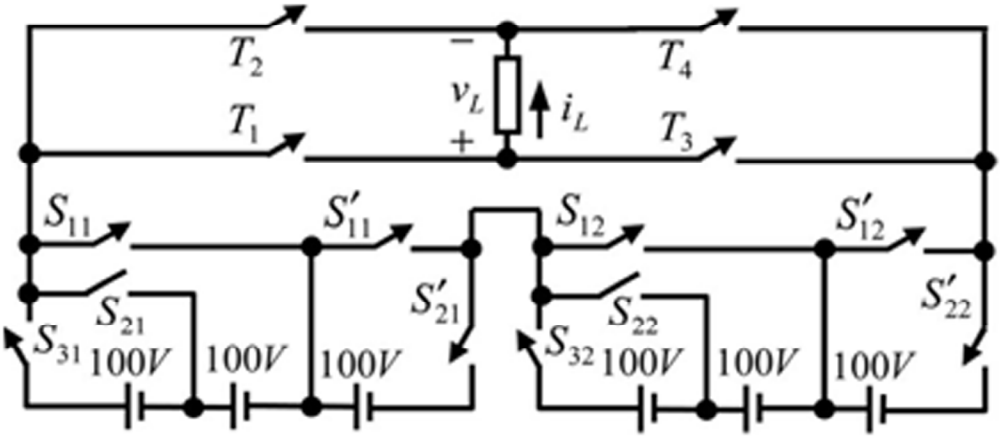

Figure 2: Symmetric topology multilevel inverter

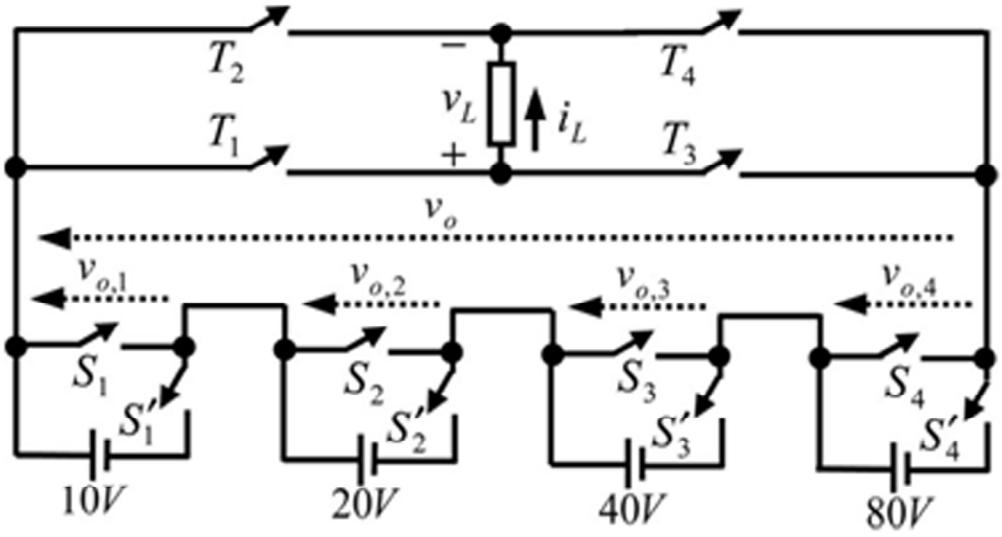

Figure 3: Asymmetric topology multilevel inverter

The advantages of the asymmetric topology are reduced number of dc sources, High speed capability, Low switching loss and High conversion efficiency.

Similarly, the main advantages of cascaded H bridge multi-level inverter are, it requires least number of components to achieve the same number of voltage levels and soft switching techniques can be used to reduce switching losses and device stresses. The cascaded multilevel inverter reaches the higher output voltage and power levels, and the higher reliability due to its modular topology and the simplicity. Among inverter topologies, the cascaded H-bridge multilevel inverters require the least number of total main components. One aspect which sets the cascaded H-bridge apart from other multilevel inverters is the capability of utilizing different DC voltages on the individual H-bridge cells which results in splitting the power conversion and asymmetrical multilevel inverters can be obtained.

To provide a large number of output steps without increasing the number of DC voltage sources, asymmetric multilevel converters can be used. The cascaded H-bridge can operate as symmetric or asymmetric converter. In asymmetric multilevel converters the DC voltage sources are proposed to be chosen as different value according to different methods.

5. SIMULATION OF PROPOSED MULTILEVEL INVERTER

The goal of this work is to design a peak 70-V multilevel inverter with minimum 15 levels of output voltage. The number of cascaded sub multilevel inverters should be 3. Therefore, a 15-level 70-V inverter

Table 1
Comparison of Existing and Proposed Topology

Description	*Comparison of Existing and Proposed Topology*	
	15 Level Cascaded H Bridge Multilevel Inverter	*15 Level Generalized Cascaded Asymmetric Multilevel Inverter*
Number of DC Sources Needed	7	3
Number of MOSFET Switches Used	28	10
Formula for Calculating Number of Levels (N)	$N = (2n + 1)$ (n – number of DC sources)	$N = (2^{n+1} - 1)$ (n – number of DC sources)

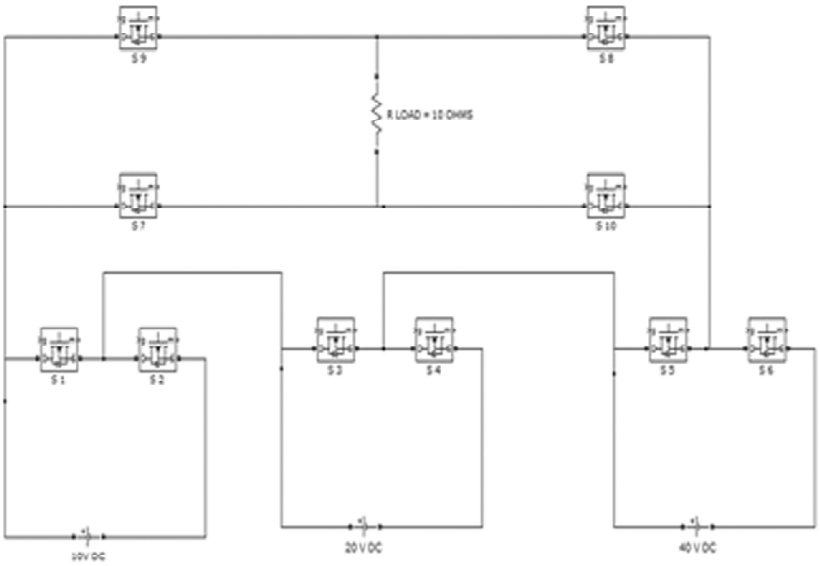

Figure 4: Cascaded multilevel inverter using series connection of sub multi-level inverters

based on the proposed generalized multilevel inverter is designed in which the values of the dc voltage sources are different. The proposed 15-level inverter uses 10 IGBTs. There are three numbers of sub multi-level inverters are used which as a different values of DC sources like 10V, 20V, 40V. Since the values of input DC sources are different, the above topology is called asymmetric cascaded multi-level inverter. Each sub multilevel inverter consists of two switches. The above sub multi-level inverters are connected in series to form a generalized cascaded multi-level inverter.

The proposed sub multilevel inverters can be connected in series to achieve the desired voltage and number of voltage levels. The proposed sub multilevel inverters can be connected in series to achieve the desired voltage and number of voltage levels. The output voltage of the sub multilevel inverters (and series connection of them) is always positive or zero. To operate as an inverter, it is necessary to change the voltage polarity in every half cycle. For this purpose, an H-bridge inverter is added to the output of the series connected sub multilevel inverters. It is important to note that the switches of the H-bridge must withstand higher voltage. This should be considered in the design of the inverter.

However, these switches are turned ON and OFF once during a fundamental cycle. So, these switches would be high-voltage low-frequency switches. The Figure 4. shows the diagram of 15 levels asymmetric cascaded H bridge multilevel inverter. Each sub multilevel inverter has separate DC voltage source. To generate the required gate pulse for this inverter SPWM method is used. In this method a sinusoidal waveform is compared with a carrier wave using a relational operator. This sinusoidal waveform is a fundamental frequency of 50Hz. The carrier based PWM using Level shifted PWM is shown in Figure 5.

In this technique, to generate a 15 level of output, high frequency carrier wave is generated and compared with a single sinusoidal waveform. The Obtained output gate pulses for the various switches like S1, S2, S3, S4, S5, and S6 are shown in figure 7. The product of the compared waveform is added in the summation block and feed in to a compare to constant block which compares the input signal with a constant value. The figure 6. Shows gate pulse generation for the H bridge inverter. The switches are names as S7, S8, S9, S10.

In this Asymmetrical multi-level inverter three different input DC voltage sources are given as 10V, 20V and 40V as shown in Figure 8.

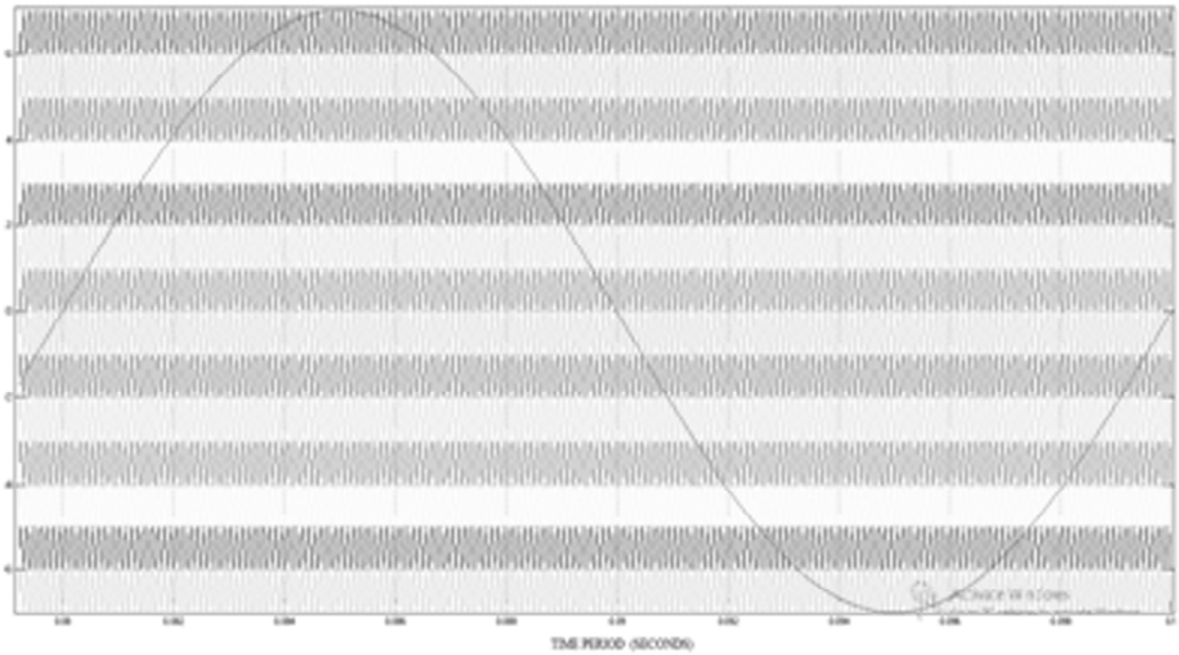

Figure 5: Carrier Based SPWM

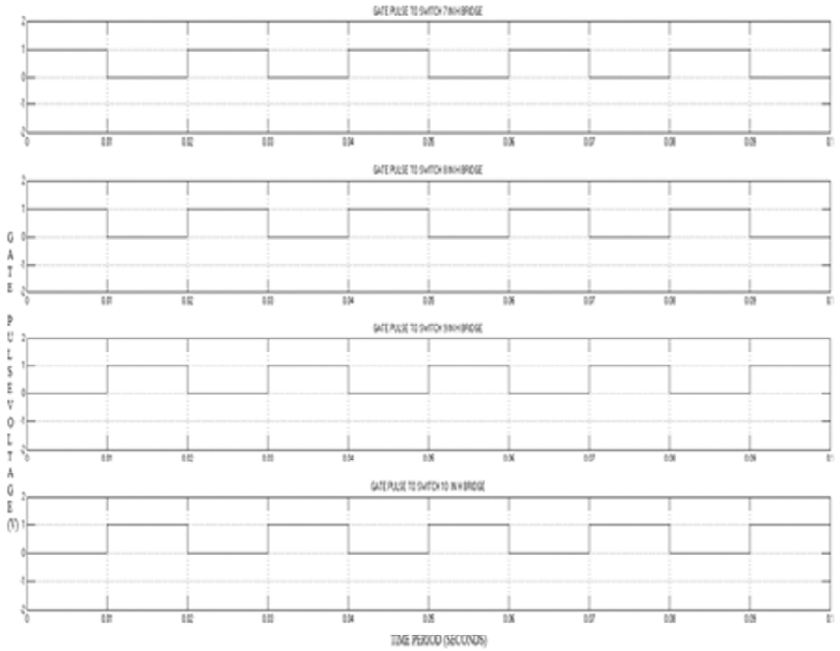

Figure 6: Generated gate Pulse waveform for H Bridge Inverter

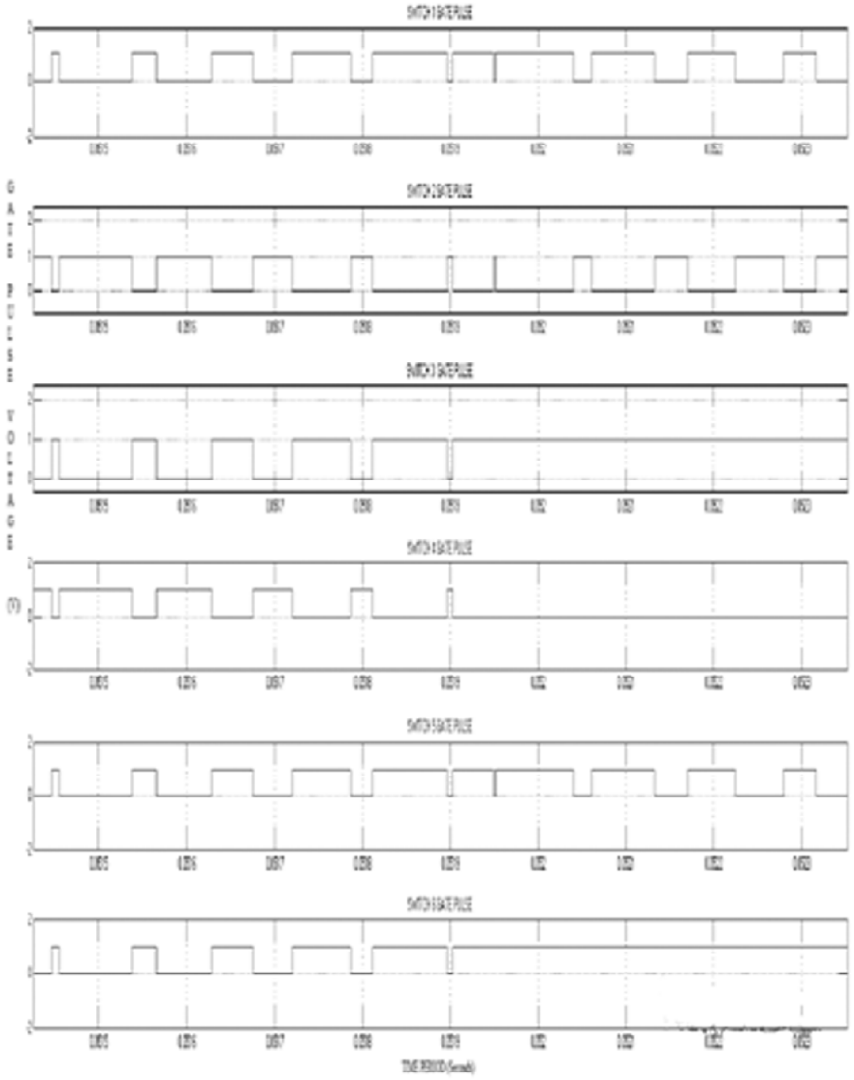

Figure 7: SPWM gate pulse waveform for Switches S1, S2, S3, S4, S5 and S6.

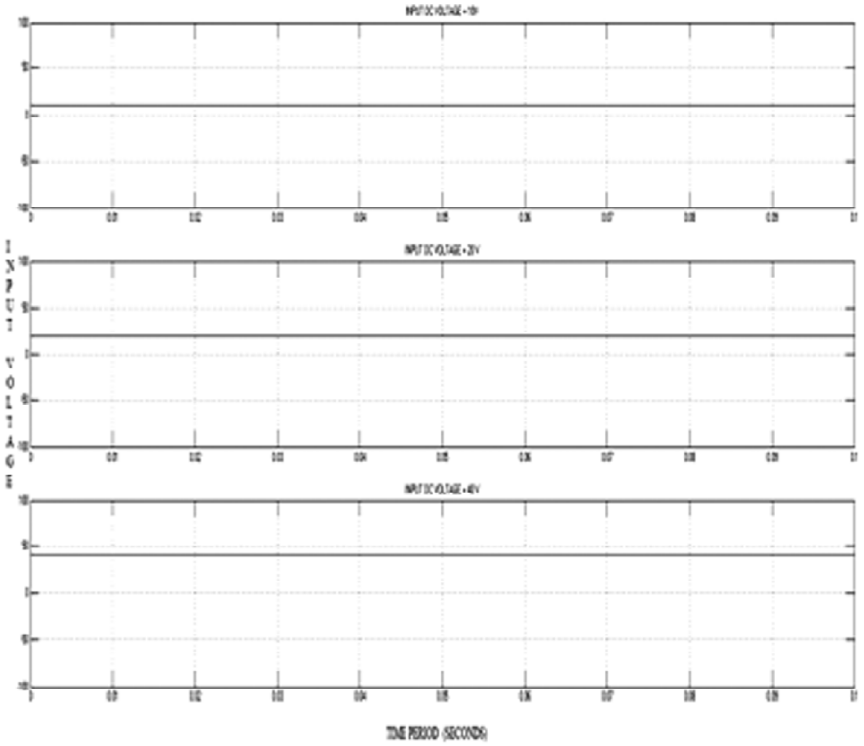

Figure 8: Input DC Voltage Source for multilevel Inverter

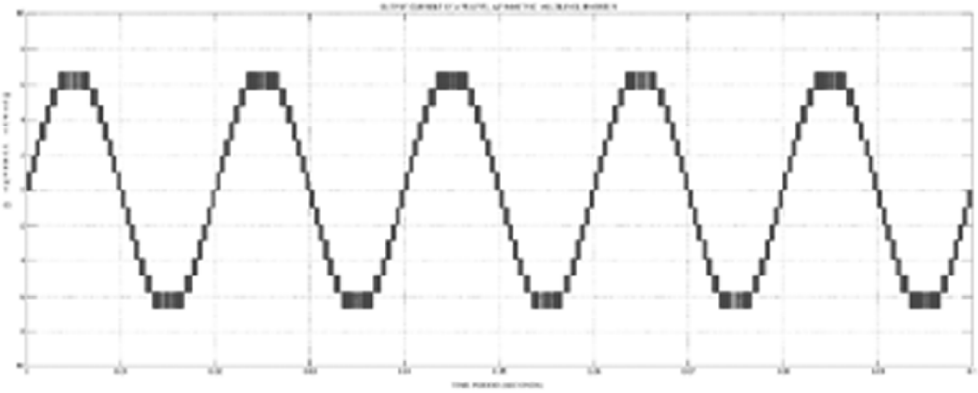

Figure 9: Output Voltage Waveform of a 15 level asymmetric cascaded H bridge multilevel inverter

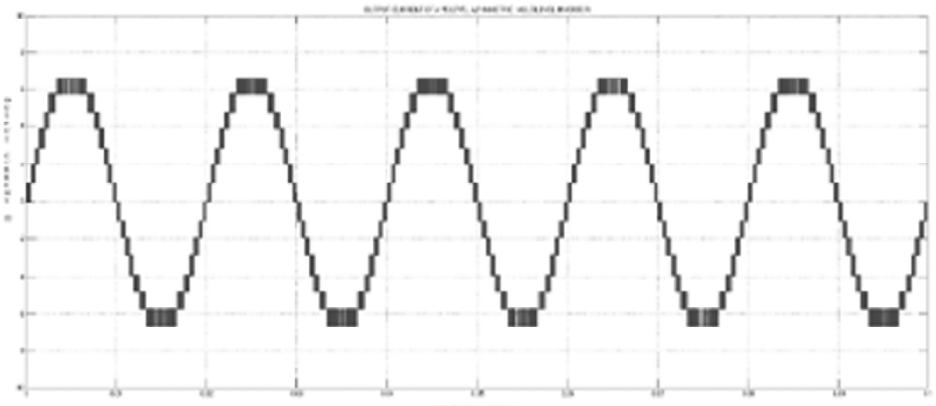

Figure 10: Output Current Waveform of a 15 level asymmetric cascaded H bridge multilevel inverter

The figure 9. shows the output voltage of a 15 level asymmetric cascaded H bridge multilevel inverter. In this simulation work, the magnitude of the output voltage 70V with fifteen levels each 10 level existing

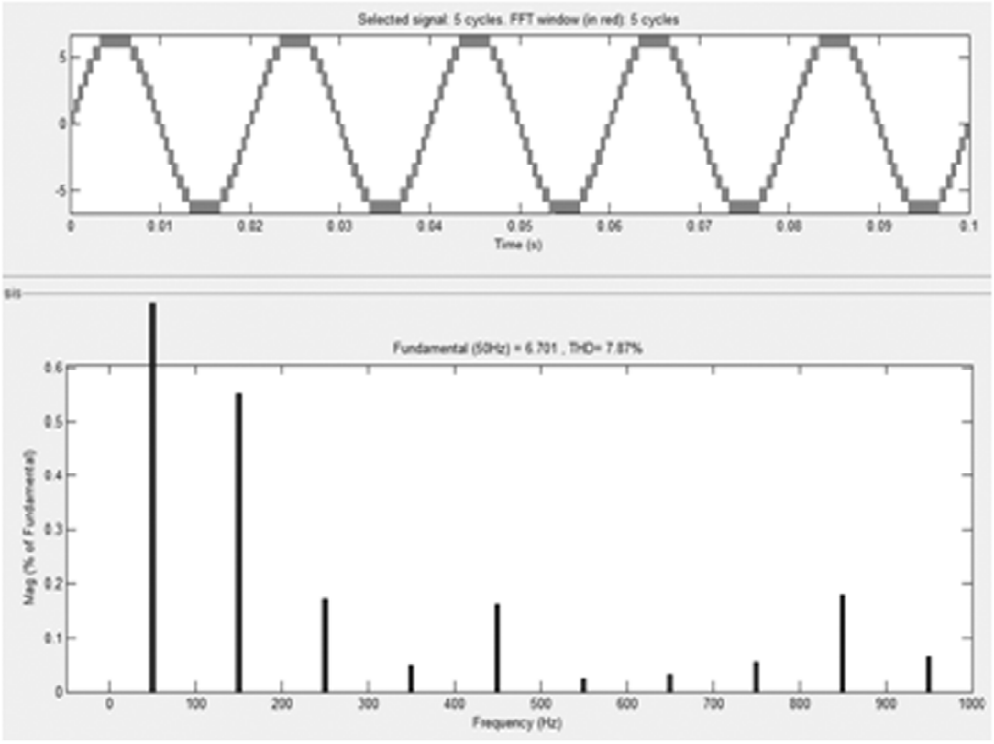

Figure 11: Total Harmonic Distortion Analysis of a 15 level asymmetric cascaded H bridge multilevel inverter

at every 10V. The Figure 10. shows the output current waveform of a 15 level asymmetric cascaded H bridge multilevel inverter. These current and voltage waveforms are obtained using Simulink/MATLAB. The Figure 11 shows the total harmonic distortion analysis of the 15 level cascaded multilevel inverter. The THD value of 7.87% is obtained by doing FFT analysis in MATLAB.

6. IMPLEMENTATION ON FPGA

The proposed 15 level asymmetric cascaded H bridge multilevel inverter is implemented in Spartan 6 FPGA. After executing the programming coding in XILINX software, the required gate pulses for the FPGA processor are generated for all the ten MOSFET switches used in this cascaded fifteen level multilevel inverter.

The above figure 12. shows the required gate pulses generated by FPGA Processor. The figure 13. shows the high frequency carrier wave generated by using XILINX software. There are fifteen carrier frequencies are generated with different magnitudes. These carrier frequencies are compared with a sinusoidal reference frequency of 50Hz.

Figure 14: and 15. depicts the hardware setup for proposed 15 level asymmetric cascaded H bridge multilevel inverter implemented using Xilinx Spartan FPGA Processor.

7. POWER QUALITY ANALYSIS

After implementation of proposed multilevel inverter using FPGA processor to validate its functionality and to analyze the quality of the output produced, the proposed inverter is made subject to the different loads such as resistive, inductive etc. Using Digital Storage oscilloscope, the total harmonic distortion analysis has been performed to observe the quality of the output current and voltage produced by the proposed 15 level asymmetric cascaded generalised H bridge multilevel inverter. From the analysis it is clearly observed that the proposed multilevel inverter outperforms well in all the aspects of output voltage, current and also the total harmonic distortion.

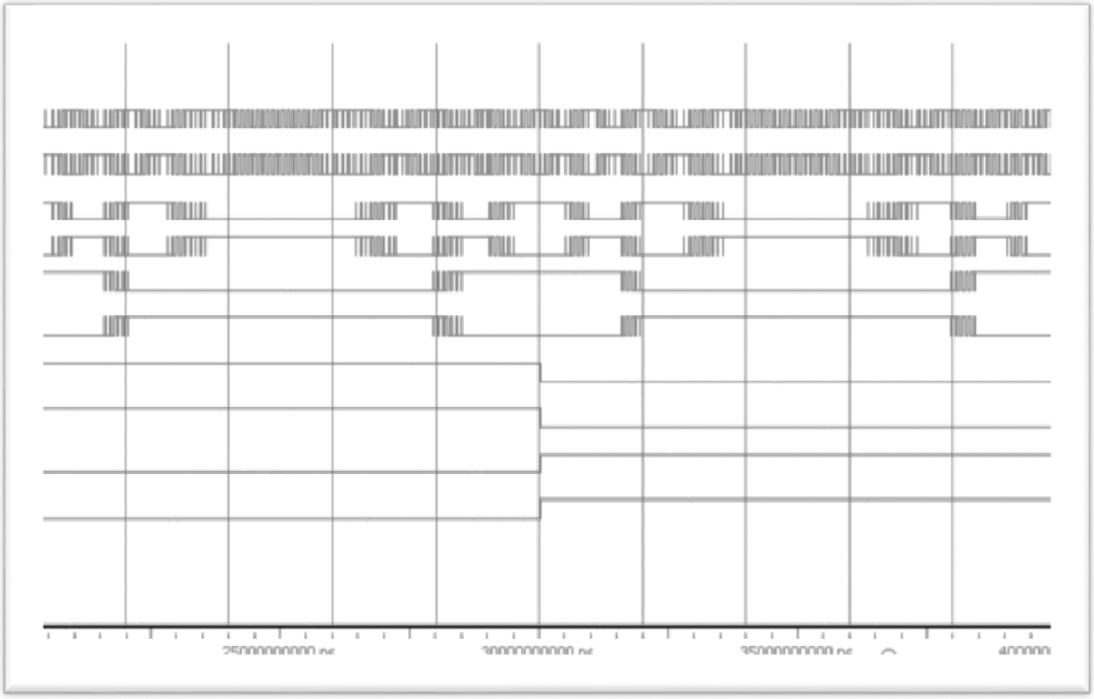

Figure 12: Gate pulses Generated by FPGA Processor

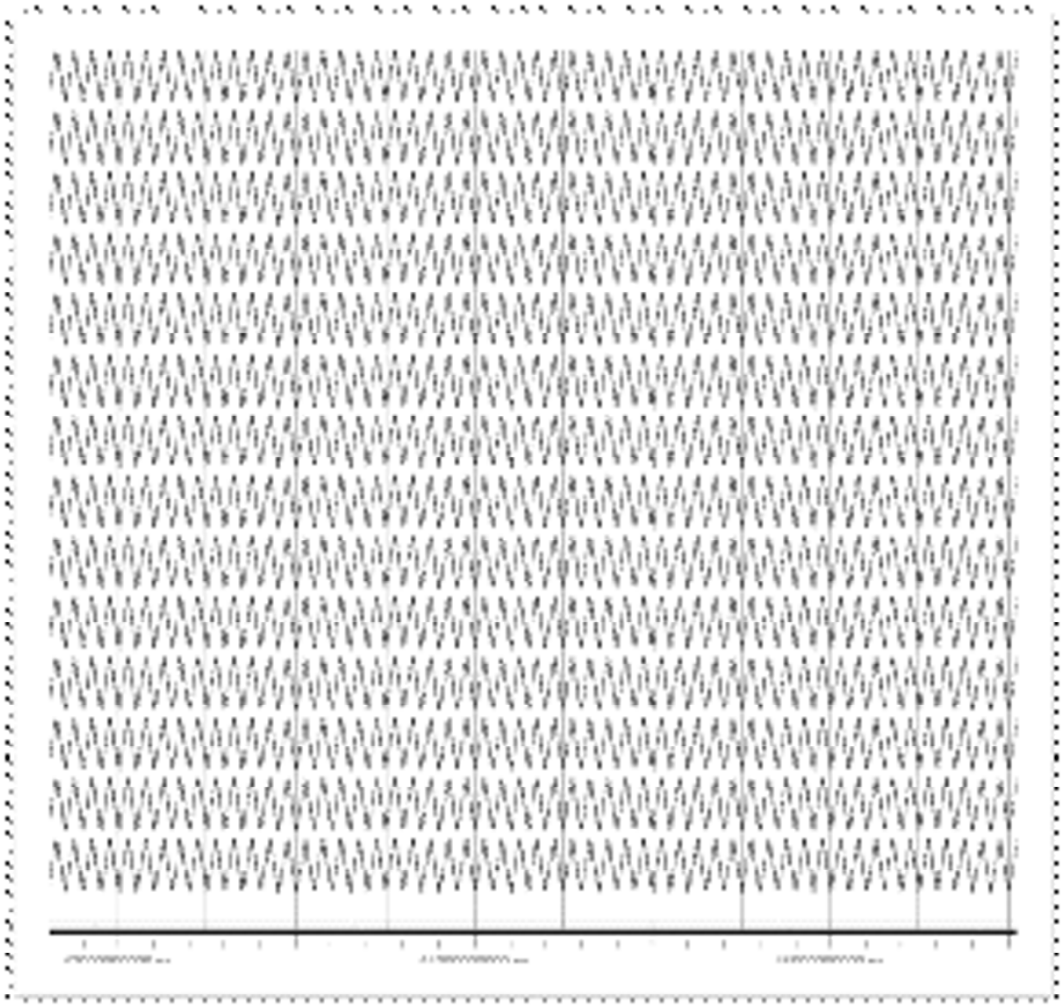

Figure 13: High frequency carrier wave generated by FPGA Processor

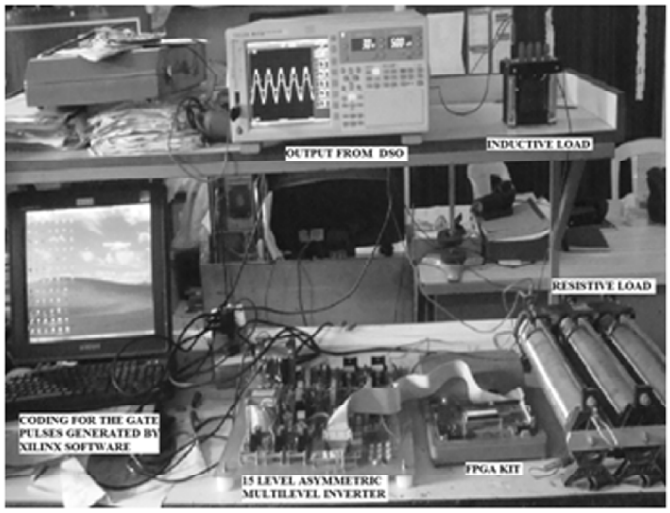

Figure 14: Hardware Setup for Proposed Multilevel Inverter

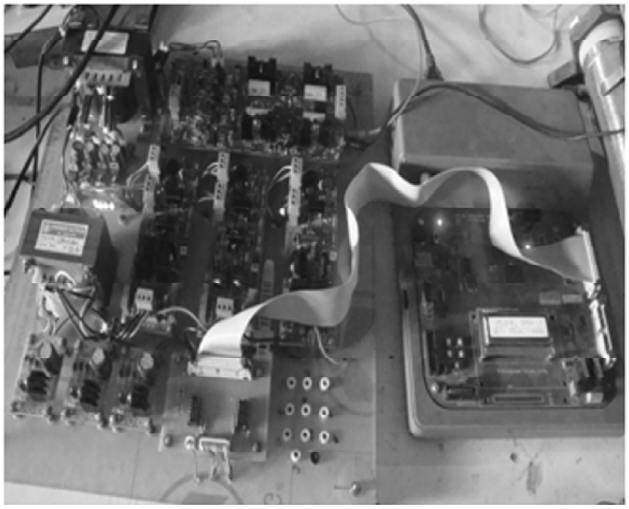

Figure 15: Implementation of Proposed Multilevel Inverter using FPGA Processor

Figure 16. and Figure 17. Shows the output voltage and current produced by the proposed inverter with resistive and inductive load respectively. From the analysis that there is no significant change in voltage and current when it is subjected to different loads but their THD values shows the difference.

As far as total harmonic distortion is concerned, both the Voltage THD (%) and Current THD (%) values are calculated. The below figure 18. shows the total harmonic distortion values of both the current and voltage when the inverter is connected to a resistive load. Here the voltage THD (%) is obtained as 2.988 and the Current THD (%) is obtained as 2.212.

The below figure 18. shows the total harmonic distortion values of both the current and voltage when the inverter is connected to an inductive load. Here the voltage THD (%) is obtained as 2.103 and the Current THD (%) is obtained as 1.568.

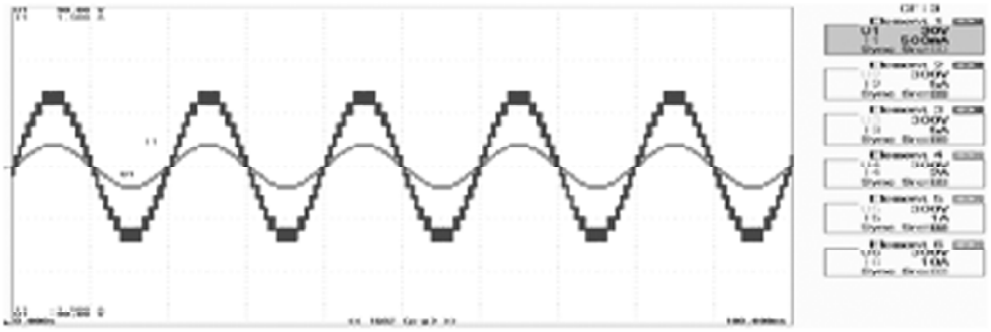

Figure 16: Output Voltage and Current Waveforms with R Load

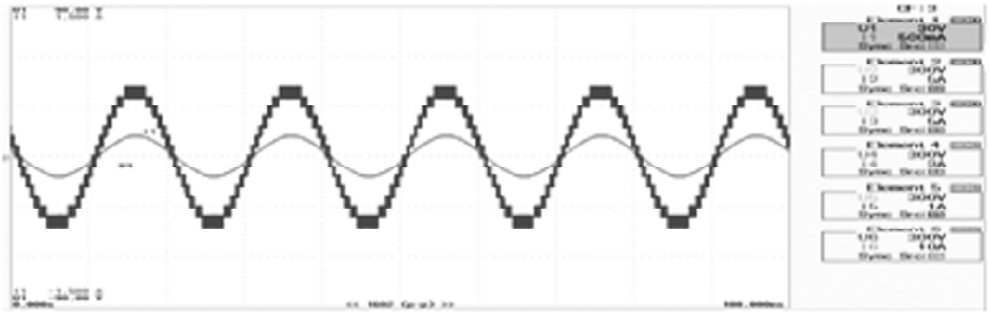

Figure 17: Output Voltage and Current Waveforms with RL Load

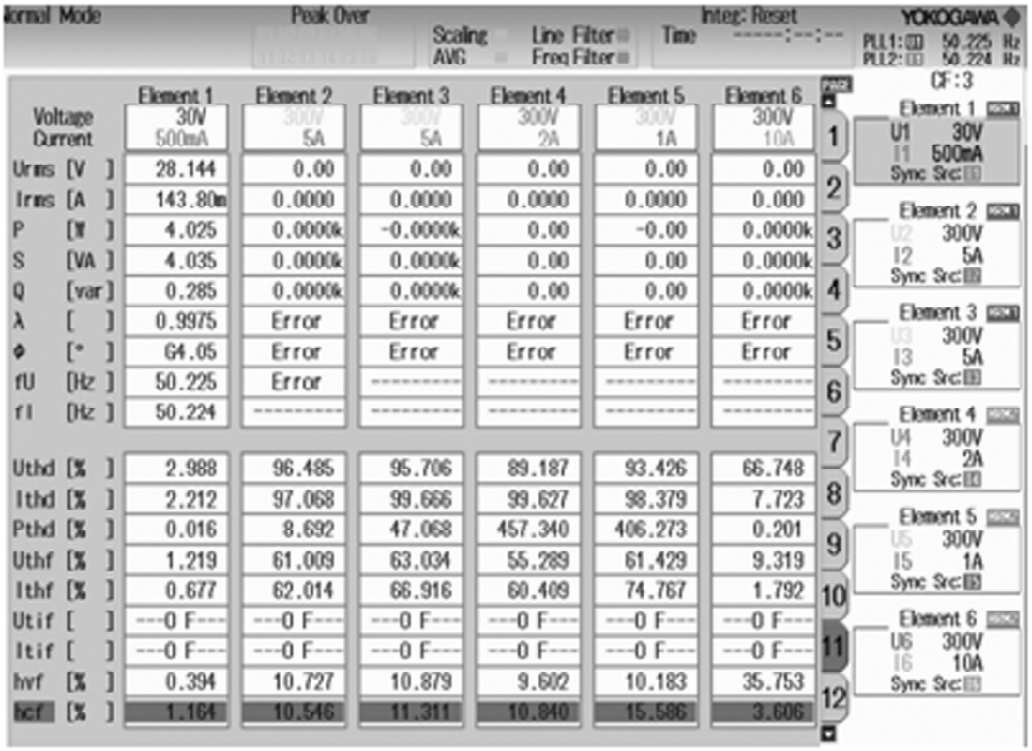

Figure 18: Total Harmonic Distortion due to R Load

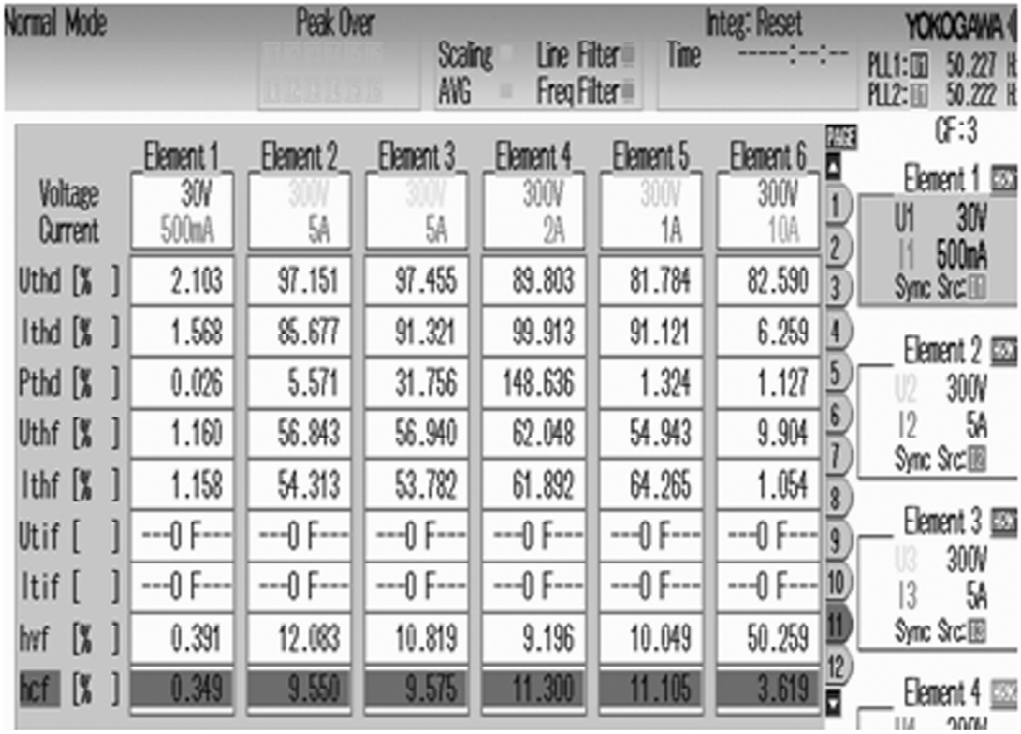

Figure 19: Total Harmonic Distortion due to RL Load

8. CONCLUSION

This work has provided a brief summary of multilevel Inverter in asymmetrical circuit topology and their control using Carrier based PWM technique using MATLAB simulation. In this work initially, a sub multilevel inverter has been proposed and then the cascaded sub multilevel inverters have been considered as a generalized multilevel inverter in asymmetric conditions. It also focuses on getting a more output

voltage level with reduced number of switches. The proposed multilevel inverter was designed considering several factors such as the number of switching devices, number of dc voltage sources, number of output voltage levels. In asymmetric topology, the simulation results have been presented for a 15-level inverter to validate the ability of the proposed topology in generating of desired output voltage by using carrier based PWM technique. Further the proposed design has been implemented using Xilinx Spartan 6 FPGA Processor. The main advantage of this is the ability to generate SPWM waveform in real time using control algorithm in the FPGA processor which reduces the computational time required to determine the switching times for inverter legs, making the system more suitable for real time implementation for larger drives. This FPGA based cascaded multilevel inverter finds wide application where power quality issues are the major considerations. In future, the total harmonic distortions are reduced by using Space vector PWM technique.

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