I J C T A, 10(8), 2017, pp. 33-38 ISSN: 0974-5572

RAM Memory testing based on JTAG

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ABSTRACT

Boundary scan is a method for testing interconnects (wire lines) on printed circuit boards or sub-blocks inside an integrated circuit. JTAG/Boundary Scan is possibly the most resourceful test access technique around. The effect of testing will affect various parameter of device under test. In general the areas concentrated while testing are fault coverage, test coverage, testing time, power reduction, vector compression.

The statistics which should be observed while testing the circuit such as test coverage, testing time, fault coverage, test vectors, testing power, delay. It is difficult to process the testing with all the criteria into the account. In order to make the process easier. The boundary scan based testing for UUT like inter connect test and RAM are performed using trainer kit 1149.1 on board level testing.

Keywords: JTAG, Boundary Scan Testing, Interconnection test, Ram test, Test Coverage.

1. INTRODUCTION

This paper analyse the various tests involved in the processor testing and gives an elaborate testing process including boundary scan testing and memory cluster testing memory cluster testing test the connectivity between boundary scan cells and non-boundary scan points . The complete infrastructure involves inter connection test logic cluster test memory access test etc. The first part of the paper gives the detail on test pattern generation JTAG, TAP controller and CASLAN programme and next part analyze the memory cluster testing and test coverage report for the same.

1.1. JTAG/Boundary Scan Test

Limited access to test points led to the concept of placing the test points within the inter- gated circuit devices themselves. Most CPLDs and FPGAs include boundary scan logic as part of their internal structure independent of the functionality of the logic programmed into the device. These devices are JTAG compliant. A circuit, known as a boundary scan cell, is placed between the programmable logic and each input and output pin of the device, The cells are basically memory cells that store a I or a O. The cells connected to the programmable logic inputs are called input cells, and those connected to the programmable logic outputs are called output cells. Boundary scan testing is based on the ITAG standard (IEEE Std. 1149.1).[23] The four JTAG inputs and outputs- TDI (test data in), TDO (test data out), TCK (test clock), and TMS (test mode select}-are known as the test access ports (TAP). [25][26]

1.2. Tools For Boundary Scan Test

CASCON GALAXY allows implementing boundary scan testing of JTAG-compliant or custom microelectronic integrated circuits when used in conjunction with Goepel's boundary scan physical interface. Designer and Prototype level sub scribers of CMC Microsystems can download the software from the CMC web site and access licenses through the License Management System (LMS).

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The CASCON Galaxy software runs in conjunction with the SCANFLEX Combo (SFX/Combo) hardware controller which Interfaces with an I/O Module. The CASCON Galaxy software must be configured with the appropriate drivers to communicate with the hardware interface.

The main features of the software include:

- Fully integrated software platform
- Graphic project development
- Use of intelligent tools
- Maximum safety for the test vectors
- extended test depth for non-scan able circuitry
- Deep interaction and integration capability for other ATEs
- Maximum modularity and scalability

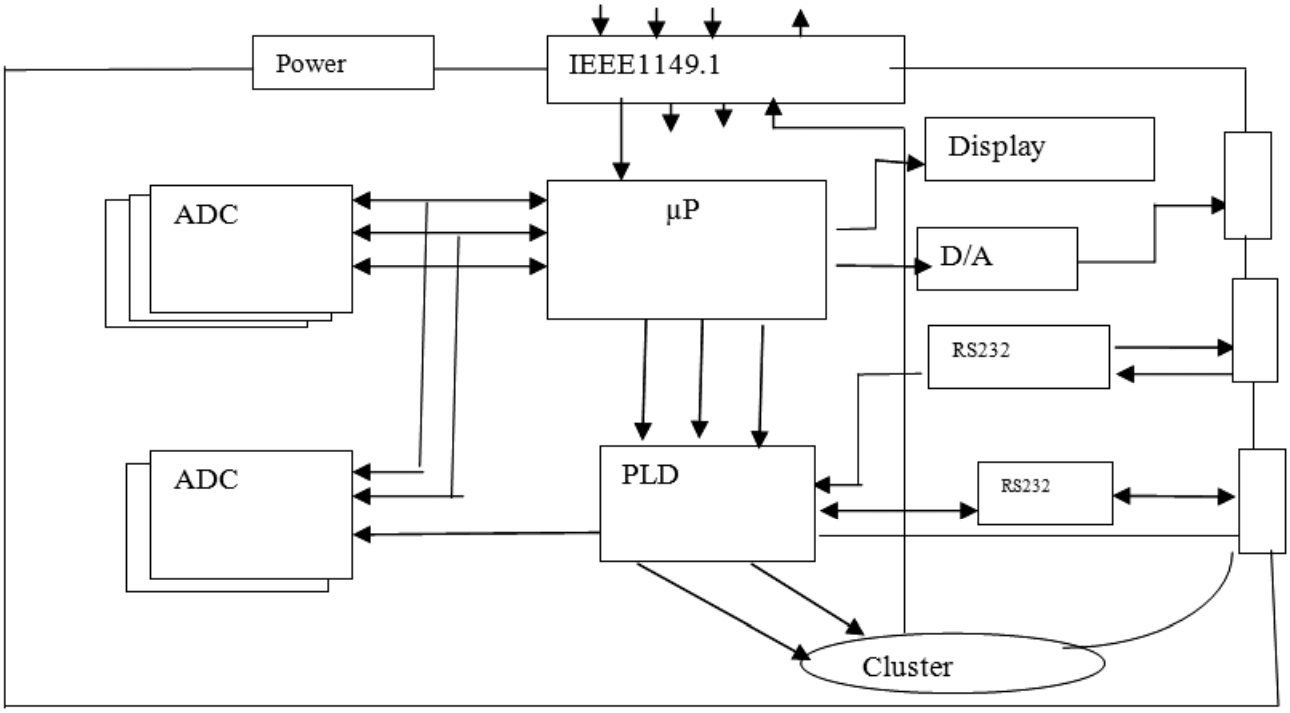

Figure 1: Test Coverage Boundary Scan Stand Alone

Features that Make the Difference to other JTAG/Boundary Scan Software Solutions [32][33].

- Scalable high-performance platform with more than 40 integrated tools, central project data base and intuitive user interface
- Interactive JTAG/Boundary Scan visualisation on layout, schematic and logic level for graphical analysing and debugging
- Support of test and programming strategies for internal and external instrumentations beyond JTAG/ Boundary Scan.
- Extended test coverage and precise fault diagnostic by complete inclusion of non-JTAG/Boundary Scan circuits.
- Simple, fast and goal-oriented project development by intelligent tools and automated system processes

Integrated safety functions avoid hardware damaging scan vectors and guarantee safe test programs

2. INTERCONNECTION TESTING

The interconnection test checks the connections between Boundary Scan pins. This test considers transparent buffers and disables other buses. If possible, it creates test vectors for pull-up/pull-down resistors.[11].

In these test all Boundary Scan nets and BScan pins will be checked for Stuck-At faults in the first part, the stuck-at test.

The independence of the BScan nets will be checked in the second part, the test for shorts [2], [3].

2.1. Stuck-at Test

The stuck-at test consists of two parts, the stuck-at-low and the stuck-at-high test. One or more test steps will be generated for the stuck-at-low test so that

- all BS can nets have a high level in each test step if possible. Thus the stuck-at test is separated from the test for shorts and clear identification of the error types is possible.
- each drivable pin drives a high level at least one time in the stuck-at-low part and each input and bidirectional pin measures a high level at least one time (real stuck-at test).[7].

2.2. Boundary Scan Testing on RAM

Similarly to the interconnection test, this test is automatically generated. Its goal is the connection test between BScan ports and a RAM. For this purpose, the functionality of a RAM is used which is stored in the library.

Usually, RAM devices do not have embedded Boundary Scan resources. Nevertheless, the electrical connection to the board can be verified. Based on the RAM model description, CASCON automatically generates address- and data values, which will be written to and read from the RAM.

Models are currently available for SRAM, SSRAM, DRAM, SDRAM, DDR RAM, DDR2 RAM and others. Support is also provided for Dual Port RAMs and other particular RAM types.

In this context, not the entire RAM is tested. Instead, test data are written to several test addresses and read back.

In case of an error, the defect address- or data line is diagnosed. A precondition is the proper function of all involved control lines. The rest of the board is hold in a conflict-free state.

- The RAM must have a library model with functional description. This description is located in the Device Description block and is marked as RAM. It contains the port description for address- data, and control lines as well as functional descriptions in tabular form.
- All ports described in RAM must have connections to BScan outputs/ -inputs.

  Non-BScan buffers between the BScan pins and the RAM are automatically analyzed.
- All nets used in RAM must be freely movable. The attributes HIGH, LOW, DRIVEN, DRIVE_HIGH, DRIVE_LOW lead to an error during generation.
- A BScan Netlist File (*.CNL) must be provided.

3. TEST COVERAGE ANALYSIS AND REPORT

The analysis of test coverage is an essential instrument for estimating the quality of the generated test programs. It allows conclusions about whether it makes sense to write further test programs or to use Other test procedures when applicable. The Test coverage report contains the test coverage achieved by a given

CASCON Batch File with the included tests or by one individual test. The test coverage analysis is based on the Netlist Table File *.NLT that was created during Parse Net List on the Link to Library page. That means that nets interconnected via serial resistors are regarded as separate nets (and do not form a linked net like they do for the ATG process). [15], [16].

Having created the Test Coverage Report, the coverage can be visualized and analyzed in the Workbench Window. For this purpose, click on the hyperlink in the actions area, displaying the number of tested pins and nets.

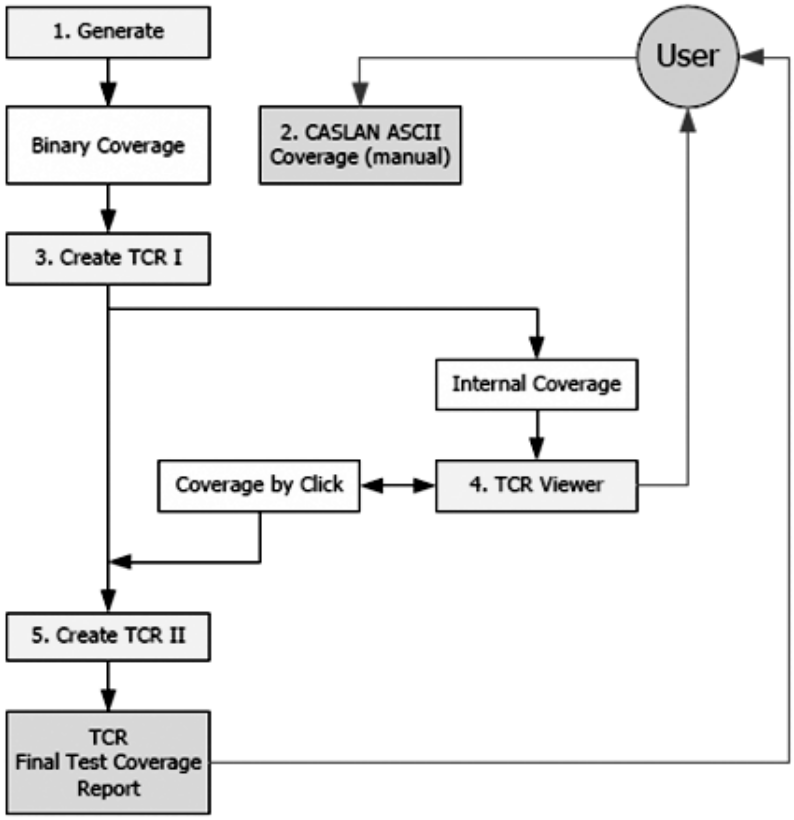

Figure 2: Flow chart Test Coverage Report

4. OUTPUTS/RESULTS

Here the following circuits are tested and its test coverage report analysis shows the number of pins /nets tested are available in fig 1.3 [2], [3]. Fig 1.3 shows the test coverage report of a interconnection .And the

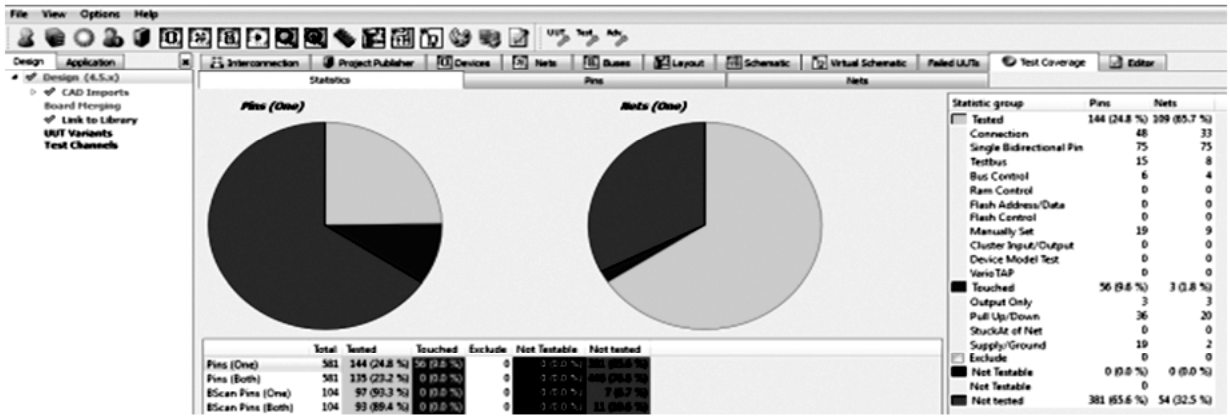

Figure 3: Test coverage report for interconnection test

Table 1
Comparison of test coverage reports for pins of chosen circuits

Circuit Name	*Total Pins*	*Tested*	*Not Tested*	*Touched*
Interconnection	581	144(24.8%)	381(65.5)	56(9.6%)
Interconnection U3	581	165(28.4%)	356(61.3%)	60(10.3%)

Table 2
comparison of test coverage reports for nets of chosen circuits

Circuit Name	*Total Nets*	*Tested*	*Not Tested*	*Touched*
Interconnection	166	109(65.7%)	54(32.5%)	3(1.8%)
Interconnection U3	166	116(69.9%)	43(25.9%)	7(4.2%)

Table 3
Elapsed time taken by the UUT

Name of UUT	*Elapsed time taken by the UUT*			
	Status of power and test bus			
	LL	*LH*	*HL*	*HH*
Interconnection	.090	.067	.087	.085
Interconnection U3	.086	.080	.142	.084
RAM U9	.340	.375	.364	.427

Table 1.1 and Table 1.2 compares the number of pins and nets tested and not tested of various circuits. The sample is taken from boundary scan coach, geopel electronics. The CASCON software is used to generate the test vectors and CASLAN language is used for programming. [32][33]

Table 1.3 gives the elapsed timed difference due to switching of power and testbus in UUT. If the controller's (Production Integration Package) PIP4 is selected for power switching, the active level of these two bits has to be independently defined under PIP4 switch levels. The initialization state of the two bits is tristate. So the extra hardware device has to evaluate this tristate as inactive level (e.g. pullresistors).[1],[2],[3]

5. CONCLUSION

Thus the UUT (Unit under Test) like RAM and interconnection are tested using CASCON software and the program are generated using BSDL and the outputs are presented in the paper. The following points are observed from results of test coverage of the UUT by JTAG. Normally the time taken testing the circuit is the test time which will not equal for all the UUT. Time elapsed will be more for the RAM. These test time can also be varied based on switching level of power & test bus. In case of power when the switch level is high the time taken for testing is more, similarly for test bus when the switch is high time taken is greater

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