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Analysis of Threshold Voltage for Vertical Silicon Nano tube field-effect transistors (Si V-NTFETs)

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ABSTRACT

This paper describes the variation in threshold voltage (VTH) for cylindrical channel vertical nanowire silicon Nano-tube field-effect-transistors (Si-NT FETs). The device performance parameters like Drain Induced Barrier Lowering (DIBL), sub threshold slope (SS) and ION/OFF ratio and other device parameters are verified for scalable channel thickness using three dimensional technology computers aided design TCAD. The results are shown for VTH as function of channel lengths with varying si thickness (tsi) which yields better ON and OFF current characteristics at particular 16 nm technology. The results indicate that's, though the cross-sectional dimensions of these futuristic devices are very small, even then enhanced electrostatic controllability are achieved. The classical and quantum mechanical model results have been verified with simulated data obtained by VLSI Semiconductor device simulation software Genius (version 1.9.0). The unique characteristics of Si-NT FETs make them superior compared to other available MOS structure.

Index Terms: Si-NT FETs, Sub threshold slope (SS), DIBL, Threshold voltage (VTH).

1. INTRODUCTION

The demands for faster smaller and less expensive electronics equipment are basically the driving forces for improving the speed and increasing the packing density of microelectronic components. Down scaling of the device is the principle method to realize these requests [1]. For future miniaturization of CMOS devices, many device structures are being explored [2-3]. Among these the silicon nanowire transistor (SNWT) has attracted broad attention from semiconductor industry in order to enable further scaling and improve the transistor performance. The SNWTs have full compatibility with planar technology [4] in addition to that the gate cylendrical structure control short channel effects (SCEs) [5]. Silicon Nano Tube (SI-NT FETs) are considered to be an ultimate device because of unique structure that helps to achieve ultimate SCFs immunity and exponential increase of static power combination (6-7). Also nanowire channels can be used in advanced electronics high speed memories [8], wireless communication [9-11].

2. DEVICE STRUCTURE AND SIMULATION WORK

In this work we proposed a vertical Si-NT FET. The main emphasis here is to study the physical and electrical transport properties of nanowire transistors with respect to size and its dimensionality especially circular. Simulations have been performed with proportionate device dimension recommended by International Technology Roadmaps for Semiconductors (ITRS) as shown in table (1). In Fig.-1 the simulated 3D model of Si-NT FET structure is shown. This 3D model represent the three axis i.e. X, Y, Z as X & Y represent the radius (r) of the gate and Z axis represent the layout model of (drain, source and gate). In Fig-2 layout design of Si-NTFET is shown. The meshing scale of SiNT has been drawn first and after define

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Table 1
The structure parameter used for simulator of Si-NT FETs

Symbol	*Parameter*	*Value*
Eox	Permittivity of silicon	$3.97 \times 8.85 \times 10^{-14}$ F/cm
εsi	Permittivity of oxide	$11.8 \times 8.85 \times 10^{-14}$ F/cm
tsi	Channel thickness	10 nm
tox	Oxide thickness	3 nm
L	Channel length	40 nm
VT	Thermal voltage	0.0256 V
ϕM	Metal work function	4.7 ev
Na	Acceptor ion concentration	10^{15} cm^{-3}
Nd	Donor ion concentration	10^{20} cm^{-3}
Ni	Intrinsic ion concentration	1.45×10^{10} cm^{-3}

region i.e. filled with materials of particular technology say 16 nm resulting into 3D Model. Si- Nano Tube devises are grown vertically (VNT FET) and covered with SiO2 to prevent the leakage current.

Fig-3 showing 3D structure in Z direction with specific coordinates of each layer. While in Fig-4 shows the net charge density for various doping level i.e acceptor ion concentration, donor ion concentration and channel doping concentration (the gate oxide thickness is fixed 3nm). It uses drift diffusion method with quantum effect and three dimensional (3-D) Poisson equations in cylindrical coordinate has been solved with suitable boundary conditions to find the threshold voltage by varying Si-channel thickness with fixed channel length. These simulation are performed using 3D numerical simulator visual TCAD. [4]

3. SIMULATION RESULT AND DISCUSSION

The VNTFET with Si tube channel (Gate all around) scale give better electrostatic control with using an high ON current. In Fig-5 show the Electric Field density in SiO_2 region which is clear that the more charge carrier are avilable and derive the more current.

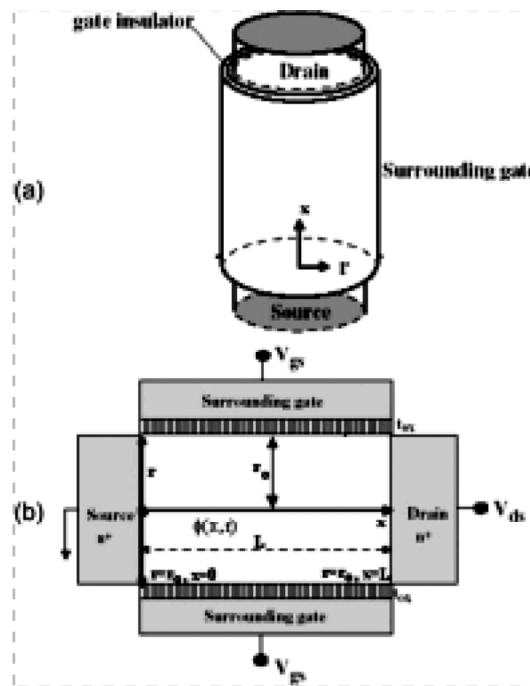

Figure 1: 3D model of Si-NT FET

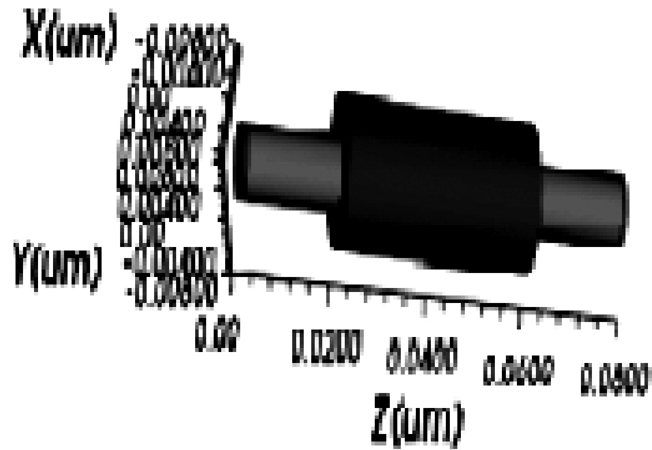

Figure 2: layout design of Si-NTFET

Also it has been reported [6] that diameter of tube is reduced in order achieve high drain current confirmed from Fig-5,6. So SiNT FET (gate thickness (tsi)) 16 mm yield better ON and OFF current beside this better SCE immunity can be maintained. In Fig-6 show the transfer characteristics of VNT FET observed at Vds = 1V (for saturation) with different channel thickness (Tsi) parameter and fixed the gate length. Fig (6) show the transfer characteristics of Si-NT FET observed at Vds = .1V (for Linear) with different channel thickness (tsi) and fixed the gate length

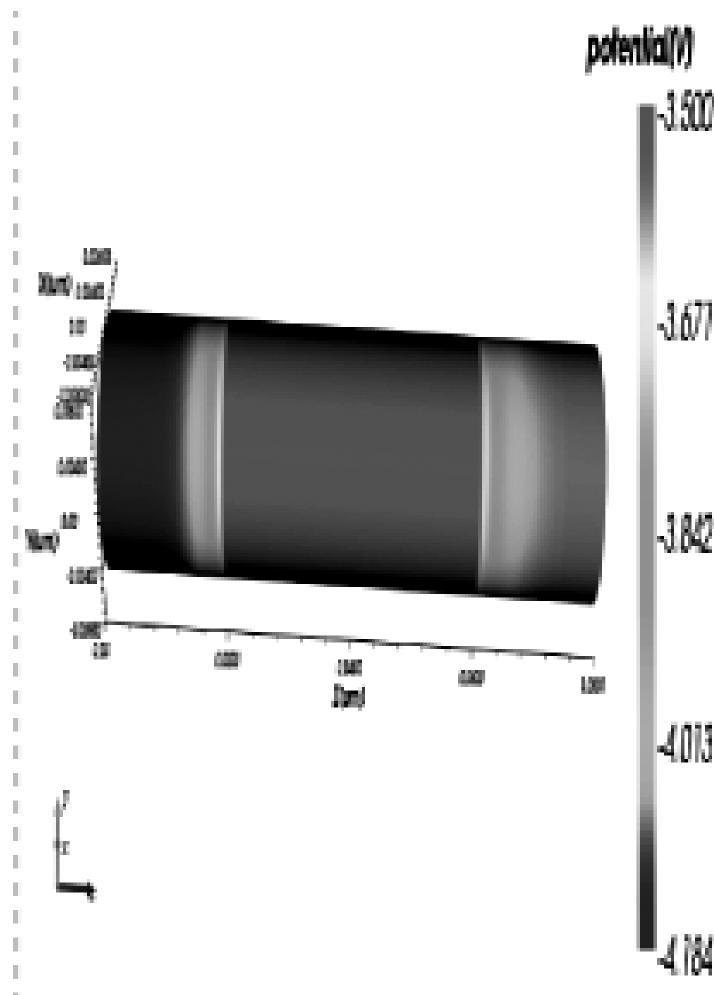

Figure 3: Various doping levels for VNT FET

Table (2) presents the variable threshold voltage with different channel thickness (tsi). The threshold voltage is extracted using constant current method with $I_D = \frac{w}{l} \times 10^{-7} A.$ Where L is channel of the device W is effective width of channel i.e $2\pi r$ (r is radius of Si-NT tube). Simulation results formed decrease the threshold voltage using increase channel thickness from (i.e 8 to 20 nm) and better SCF in a device with thinner tube thickness(i.e. 8nm).

Table-3 indicates that On/Off ratio increase by Si channel thickness (tsi) from 8 to 20 nm. So there is trade off because ION and IOFF & Si channel thickness (tsi). Major short channel effects (SCE) like subthreshold slope (SS), DIBL has been observed and calculated for Si-NTFETs performs best at 16 nm Si channel thickness (tsi).

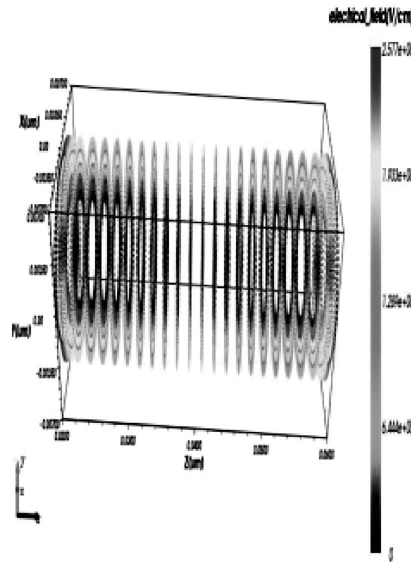

Figure 4: Electrical field in SiO2 region

Table 2
Threshold voltage Vs channel thickness (tsi)

TSi	*8nm*	*10nm*	*15nm*	*20nm*
VTH	0.23	0.23	0.15	0.18

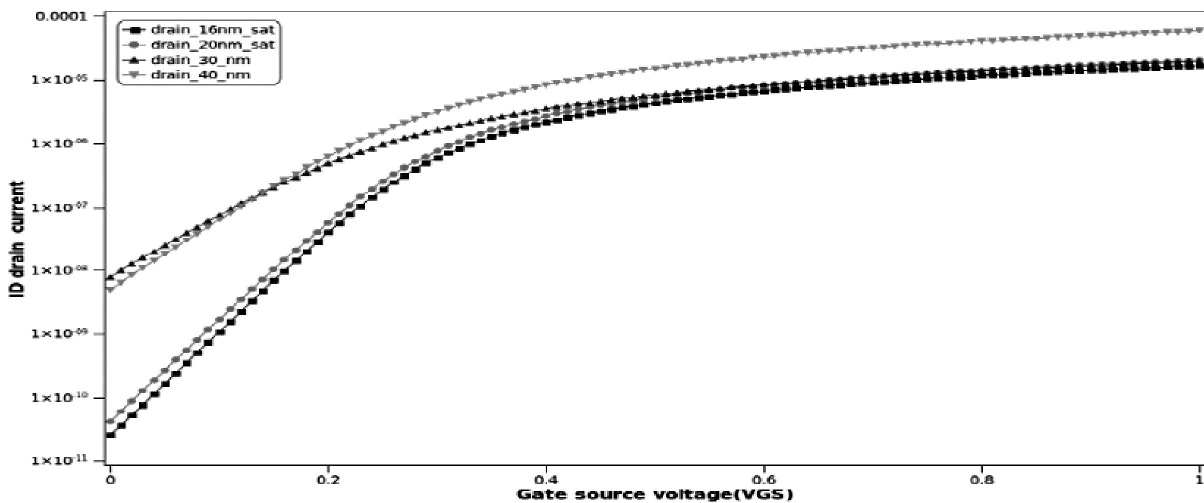

Figure 5: show the transfer characteristics of VNT FET observed at Vds= 1V (for saturation)

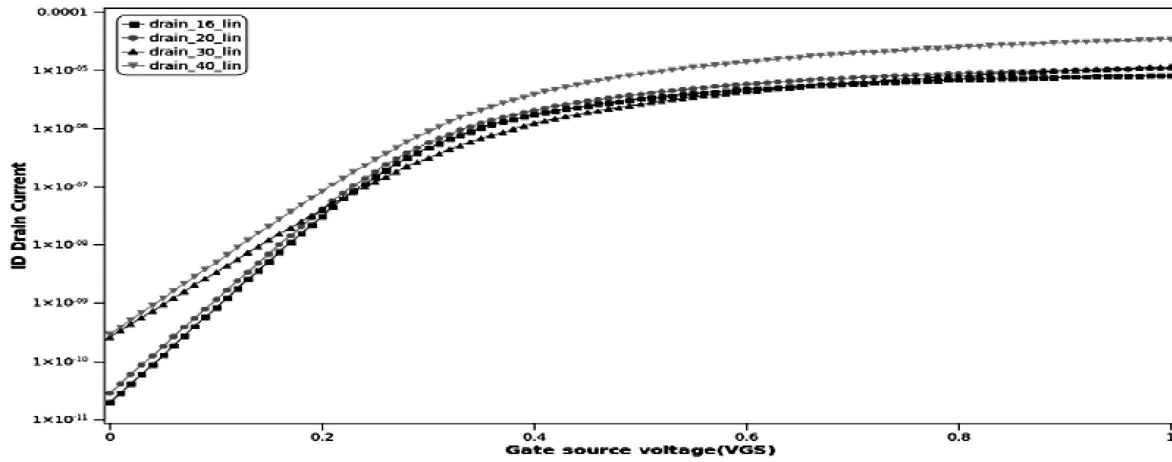

Figure 6: show the threshold voltage (VTH) variable of different Si channel thickness(tsi)

Table 3
Current variation versus tsi thickness

TSi (nm)	*DIBL*	*VTH*	*ION*	*IOFF*
8	0.09	0.23	1.67×10-5	2.505×10-11
10	0.08	0.23	2.62×10-5	4.22×10-11
15	0.04	0.15	1.97×10-5	7.86×10-9
20	0.03	0.18	5.89×10-5	4.95×10-9

Lowest value of DIBL achieved Therefore overall improvement in device parameter is observed at the optimized Si channel thickness (tsi).

4. FABRICATION PROCESS

Proposed Si-NTFET device can be fabricated using the Top Down Approach. [4]

1. Silicon wafer orientation <111>
2. Thermal oxidation growth at 900°C
3. Source and drain formation using electron beam lithography or ion implantation curve done to create S/D regions.
4. Nano were formed using vapor phase liquid epitaxial
5. Reactive ion etching (RIE) and collective ion etching used to create gate regions.
6. SiO_2 oxide deposited by atomic layer deposition with thickness 3nm.
7. Gate material polysilicon deposition using radio frequency sputtering technique.
8. Electrode formation for source, drain and gate annealing at 420°C in presence of nitrogen for obtaining ohmic contact at source, drain and gate regions.

5. CONCLUSION

Vertical surround gate transistors of various diameters ranging from 16 to 40 nm are characterized. Fig. 5, 6 shows the typical characteristic from devices with diameter 16 nm. Also it has observed that Si-NTFETs is scalable up to 8 nm Si channel thickness (tsi). Device display very good performance with fast turn-on (subthreshold slope (SS) 55–80 mV/sec. The threshold voltage roll-off can be reduced with control short channel effects like DIBL, SS and provde better performance when reduce the thickness.

Hence SiNT FET provides faster switching speed, better turn on capacitor, and higher integrated circuits in nanowire circuits.

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