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Analysis and Implementation of DSP based Single-Carrier Thirteen-Level SPWM

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Abstract : In this paper a proposed strategy of thirteen -level single-carrier and multi wave Sinusoidal pulse width modulation (SCMM-SPWM) techniques used. During positive and negative half cycle of modulation waves (MWs), dc offset related to the amplitude of the carrier are set on the three MWs, respectively, to apply the same as well comparison logics of the MWs and carrier and also generating the zero-crossing voltage pulse disturbance (ZCVPD) is analyzed. Thus, it is implemented with only one digital signal processor chip without any other attached logical circuit or controller and verified by experimental results. The spectral characters of the conventional multi-MW-based SPWM are originally derived and compared with each other by simulation in detail. The theoretical analysis, simulation, and experimental results represented that the output characters of the proposed strategy and significantly reducing the cost with the way of implementation.

Keywords : Multi-modulation-wave (MW) sinusoidal pulse width modulation (SPWM), thirteen level, spectral character, zero-crossing disturbance.

1. INTRODUCTION

The multilevel inverters become more and more attractive and have obtained expansive foreground not only in the field of the high-voltage and huge-power system but also in a the low- voltage and small-power system, in such as the photovoltaic generation system [1]–[3].Variousmultilevel topologies have been proposed over the recent years [4]–[9]. Common ones are cascaded H-bridge [4], a flying capacitor [5], and diode-clamped [6]. Furthermore, asymmetrical topologies the a consisted of two kinds of half-bridge legs a with different level numbers are presented [7]–[9].Compared with the symmetrical line topologies, the asymmetrical ones the of significantly reduce the number of the power switches on the premise of obtaining the as same level number of the output voltages. The reduction of the amount of power the switches means that the overall loss, cost, and bulk can be further reduced.

However, multilevel pulse width modulation (PWM) strategies such as the multicarrier-basedmultilevel sinusoidal PWM (SPWM), the selective harmonic elimination PWM, and the voltagespace-vector PWM [10]–[14] are difficult to be implemented only with a digital signal processor (DSP). In [15] and [16], the multilevel SPWMs are implemented with the DSP + complex programmable logic device or DSP + field- programmable gate array (FPGA) platforms. The attached controller increases the cost and decreases the reliability as well. A single-carrier andmulti-modulation-wave (MW)-based multi- level SPWM (SCMM-SPWM) strategy is proposed in [17] and [18]. However, this kind of SPWM uses the same waveforms in the positive and negative half cycles of the MWs; in the negative half cycle, the compare logics between the MWs and the carrier need to be inversed against the positive ones to implement overall multilevel output PWM waveforms. The DSP can only implement the same comparelogic in the positive half cycle and theNegative one; thus, the attached digital logic circuits and dead-time generation circuit

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2. BLOCK DIAGRAM

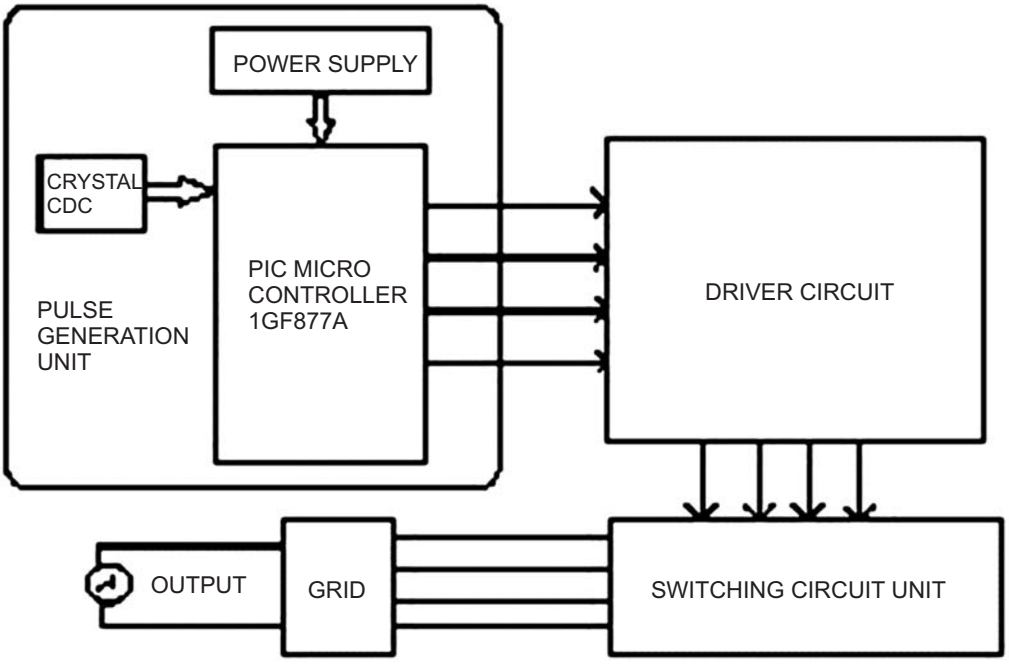

Figure 1

3. DISTURBANCE ELIMINATION AND SPECTRUM ANALYSIS OF SINGLE CARRIER THIRTEEN-LEVEL SPWM

Multilevel inverters against the two-level ones applied in the field of the low-voltage and small- power system is further enhanced.controllers are still needed to switch the control signals of various power switches.

In the low-voltage and small-power system, *e.g.*, in the photovoltaic grid-connected generation system, some control algorithms, including the grid current close-loop control, the maximum power point tracking control of the photovoltaic cells, and the dc link voltage close-loop control, are all needed to be performed. If some kind of multilevel PWM strategy suit- able for being implemented with a DSP is developed, all of the former control algorithms and the multilevel

PWM strategies can be performed with only one DSP chip; thus, the FPGA or the logic circuit is no longer indispensable. Unfortunately, none of the presented multilevel PWM strategies can be implemented only with a DSP if without any modification.

This paper proposed a seven-level SCMM-SPWM strategy based on MW reversed during negative half cycle. Further- more, the reason for generating the zero-crossing voltage pulse disturbance (ZCVPD) that a SCMM-SPWM is analyzed, and the spectrum of elimination is proposed. Finally, the spectral characters of the single-carrier and multi-MW-based multilevel SPWM, including the conventional and proposed ones, are originally derived and are compared with each other by simulation. The proposed SCMM-SPWM has the following advantages. The cancelation of the attached logic circuit or controller makes the implementation platform more concise and cheaper and also indirectly improves reliability.

4. PRINCIPLE OF THE PROPOSED SCMM-SPWM:

The schematic of the single-phase seven-level asymmetrical diode-clamped inverter is shown in Fig. 1. The left bridge arm is a four-level diode-clamped half bridge, and the right bridge arm is atwo-level half bridge. The dead zone is set between the pairs of the complementary switches, *i.e.*, V1 and V4, V2 and V5, V3 and V6, and V7 and V8.

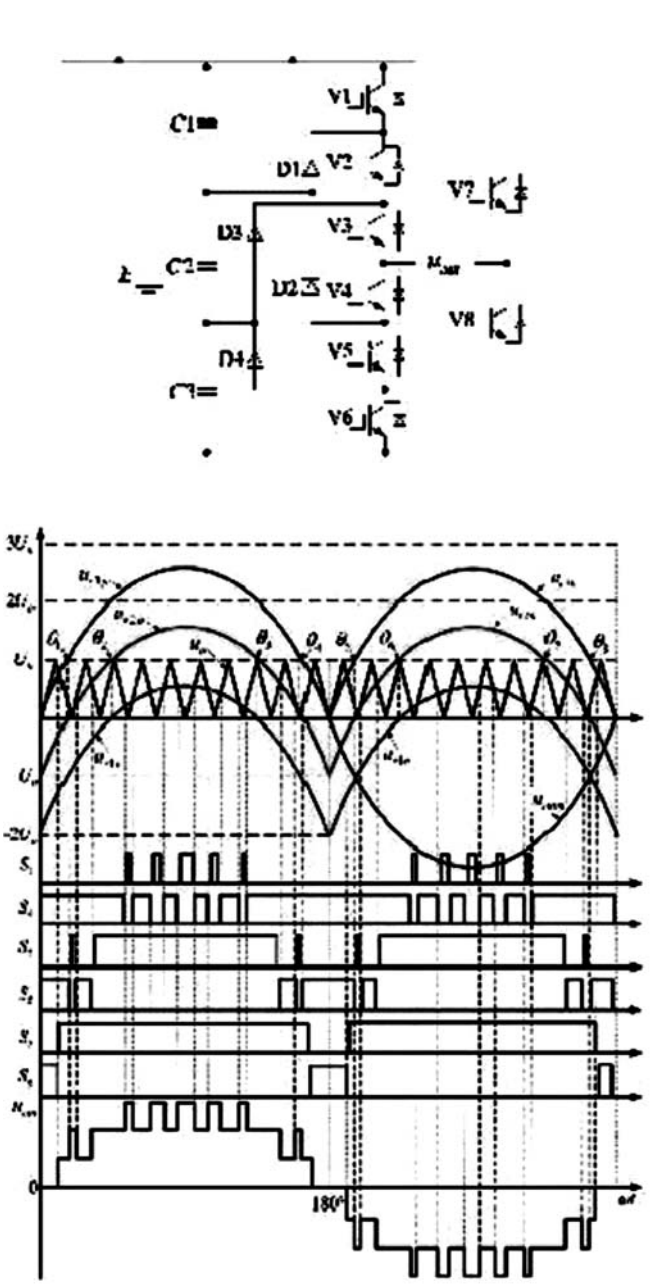

Figure 2: Schematic of the fourteent-switch seven-level inverter

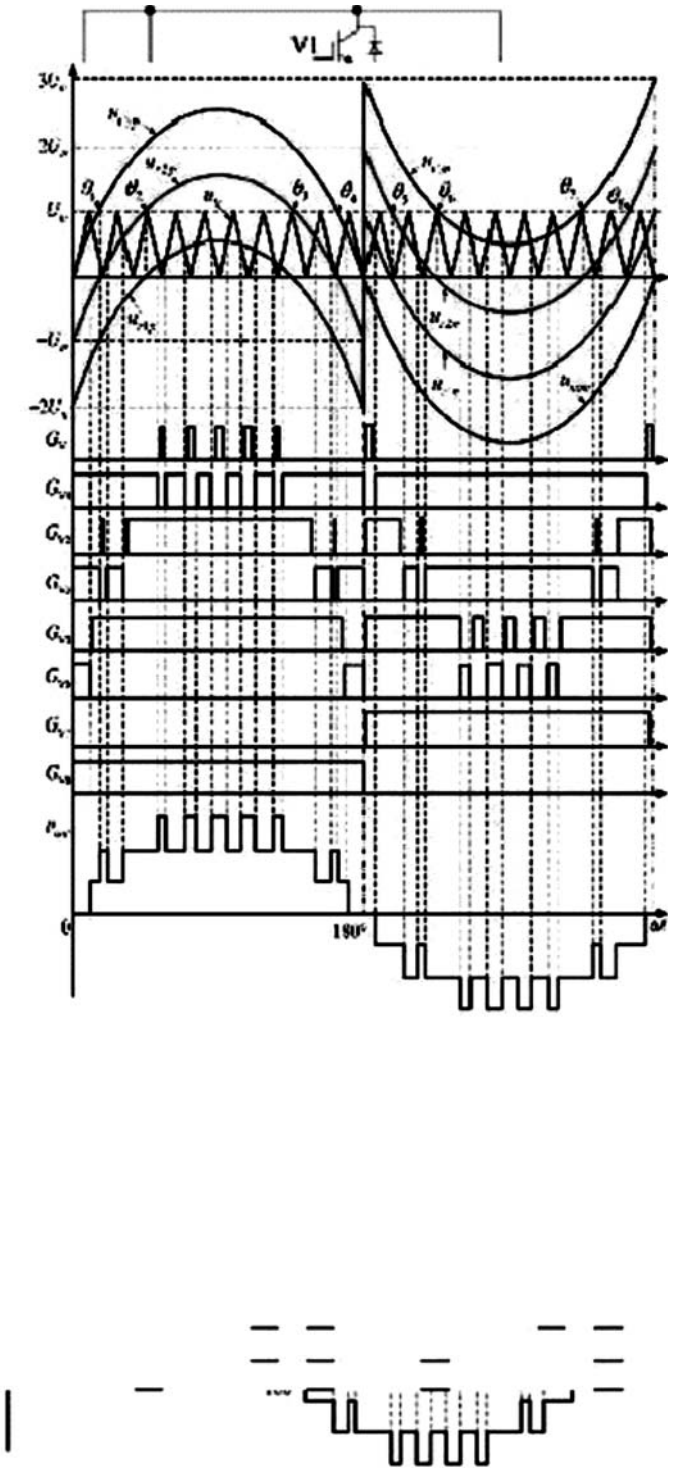

Figure 3: Schematic of the conventional thirteen-level SPWM

The multilevel SPWM strategy in [18], which is called the "conventional seven-level SPWM" in this paper, is analyzed first. The sketch of the conventional seven-level SPWM is shown in Fig. 2. Three MWs are compared with the same carrier to generate seven-level output voltage waveform. In the positive half cycle of the MWs, the comparison results of the MWs and the carrier are directly used as the control signals of various power switches. However, in the negative half cycle of the MWs, the comparison results cannot be directly used to control the various power switches; the comparison results must be reconfigured. The logics between the actual control signals (GV 1−GV 6) and the comparison results (S1−S6) are

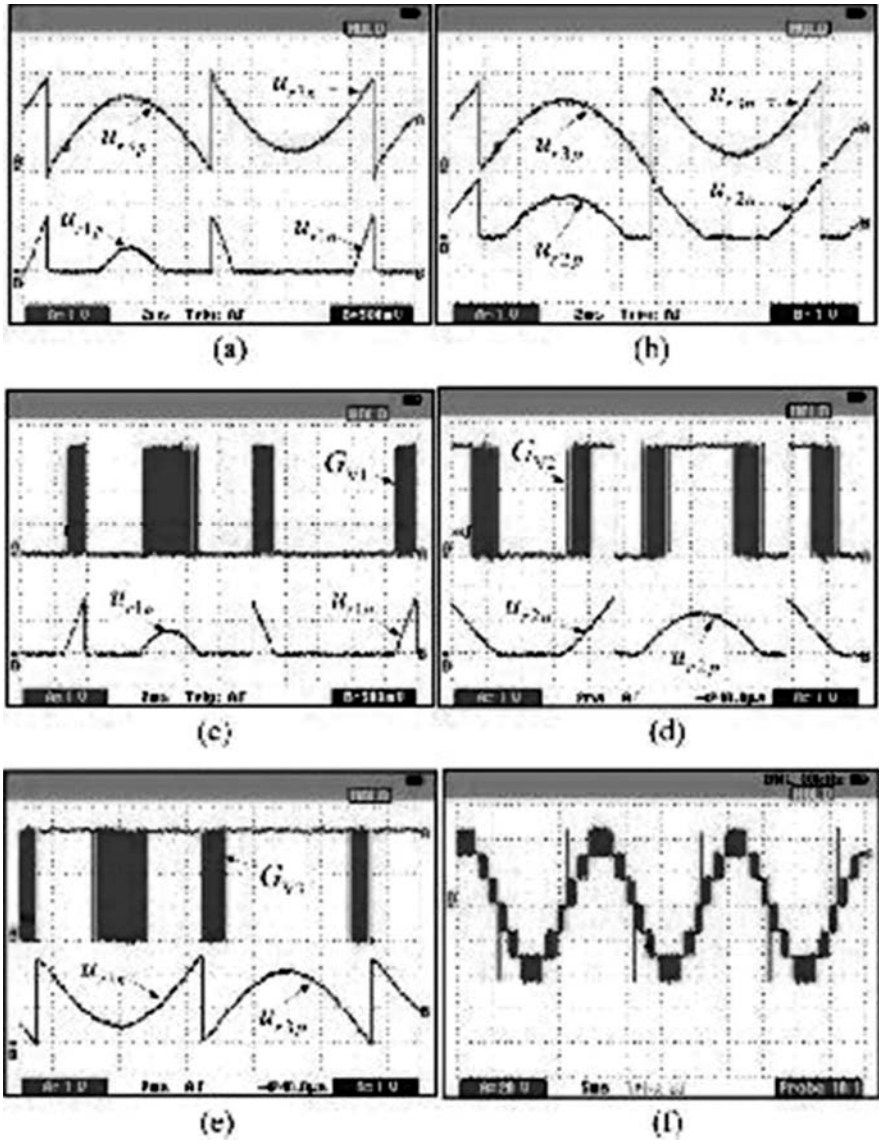

Figure 4: Schematic of the proposed seven-level SCMM-SPWM

GV 1 = S1 & S4 + S3 & S4, GV 2 = S2 & S4 + S2 & S4

GV 3 = S3 & S4 + S1 & S4, GV 4 = S1 & S4 + S3 & S4 (1)

GV 5 = S2 & S4 + S2 & S4, GV 6 = S3 & S4 + S1 & S4.

Because the logic operation depicted in (1) cannot be per- formed with a DSP, the attached logic circuit and dead-time generation circuit or FPGA chip should be added to implement this PWM strategy.

To solve the former problems, a novel the SCMM-SPWM strategy is proposed and the principle is shown in Fig. 3. To obtain seven-level SPWM waveform and without inverting the compare logic, three MWs in their negative half cycles are all inverted and biased with(2)different dc voltage are values (related to the voltage amplitude of the carrier). The functions of the three MWs are derived as follows. Define the amplitude of the carrier as Utr and the normal sine MW asunom = Unom sin(ωst)

whereUnom and ωs are the amplitude and the angular frequency of the normal MW, respectively. The function of the positive half cycle (denoted as ur3p) of ur3 has the same format with the normal one. The function of the positive half cycle of ur1 is

$$ur1p = Unomsin(\omega st) - 2Utr. \quad (3)$$

The function of the negative half cycle of ur1 is

$$ur1n = Utr + Unomsin(\omega st). \quad (4)$$

The function of the positive half cycle of ur2 is

$$ur2p = Unomsin(\omega st) - Utr. \quad (5)$$

The function of the negative half cycle of ur2 is

$$ur2n = 2Utr + Unomsin(\omega st). \quad (6)$$

The function of the negative half cycle of ur3 is

$$ur3n = 3Utr + Unomsin(\omega st). \quad (7)$$

The amplitude modulation ratio of the proposed SCMM- SPWM strategy is

$$M = Unom. \quad (8)$$

3Utr

It can be known in Fig. 3 that, within the overall period of the MW, the exchange of the comparison logic of the carrier and MWs is not needed at all. The PWM signals of the various power switches are obtained directly according to the comparison results of the are carrier and MWs. It means that are also proposed strategy can be implemented only with a DSP, and any other attached logic circuit or FPGA essential for the topology conventional one is not needed at all.

The laboratory experimental prototype of a seven-level inverter shown in Fig. 1 with aresistance–capacitor low-pass filter and DSP chip TMS30F2812 is designed. DC voltage E is 45

V, the frequency of the carrier is 10 kHz, and the frequency of the MWs is 50 Hz. Timer T1 in DSP is used to generate the carrier. To obtain eight PWM signals, all the three compare registers(CMPR1–3) in DSP are used, and the IO ports, GPIOA6 and GPIOA7, are used to output the control signals of V7 and V8.

The experimental results with M = 0.8 are shown in Fig. 4. The actual three MWs have the same shapes with the waves shown in Fig. 3; the output voltage waveform uout is seven level. However, the voltage pulse and disturbances with the ampli- tude equal to E arise at the twozero-crossing points, are which will increase the harmonics, loss and acoustic noise.

5. ELIMINATION OF ZCVPD IN SCMM-SPWM

The reason for generating the ZCVPD is analyzed, and the corresponding elimination is proposed. As known from Fig. 3 that, when the phase angle is close to zero, before 0° angle, V1, V2, V3, and

V7 are on and the other switches are off, *i.e*., uout = 0. If the states of the left and right arms are the switched synchronously, *i.e*., after the 0◦ angle, V1.

(*a*) ur1 and ur3. (*b*) ur2 and ur3. (*c*) GV 1 and ur1. (*d*) GV 2 and ur2. (*e*) GV 3 and ur3. (*f*) uout.V2, V3, and V7 are turned off and V4, V5, V6, and V8 are turned on; uout is still equal to zero. The voltage pulse distur- bance will not occur. However, the control signals of the left arm are generated by the PWM generation module in the DSP; the control signals of the right arm are generated by the software program. The essential parts nonsynchronous phenomenon inevitably occurs between the former two control voltage are signals. As- suming that the right arm changes its output voltage in advance, *i.e*., V7 is turned off and V8 is turned on first. Before the control signals of the left arm are refreshed, V1, V2, V3, and V8 are on, and the output voltage uout = +E. After the control signals of the left arm are refreshed, V4, V5, V6, and V8 are on, the output voltage uout = 0, and the output voltage is back to normal. The action of uout = + E is regarded as the voltage pulse distur- bance. The duration of uout = +E is equal to the delay time for refreshing the switching states between the left and right arms.

Further more, the dead zones between the complementary switch pairs will deteriorate the non synchronous phenomenon. Assume that the inverter drives a resistive–inductive load and the flowing direction of the output current is from B to A (as signed in Fig. 4). At 0◦, during the exchanging process of the switching state of V7 and V8, the dead zone is set; during the dead time, V7 and V8 are both off. Because the output current holds its direction during the dead zone of V7 and V8, at the same time, V1,

V2, and V3 are on, and the output current will flow through the antiparallel diodes of V1, V2, V3, and V8 to the dc source; the output voltage uout = +E also appears as the voltage pulse disturbance. When the duration of the dead zone of V7 and V8 is over, V4, V5, V6, and V8 are on, uout = 0, and the voltage pulse disturbance disappears. In the case of 180◦ angle, the reason is similar to the one of 0◦ angle; the amplitude of the output voltage pulse disturbance is equal to −E.

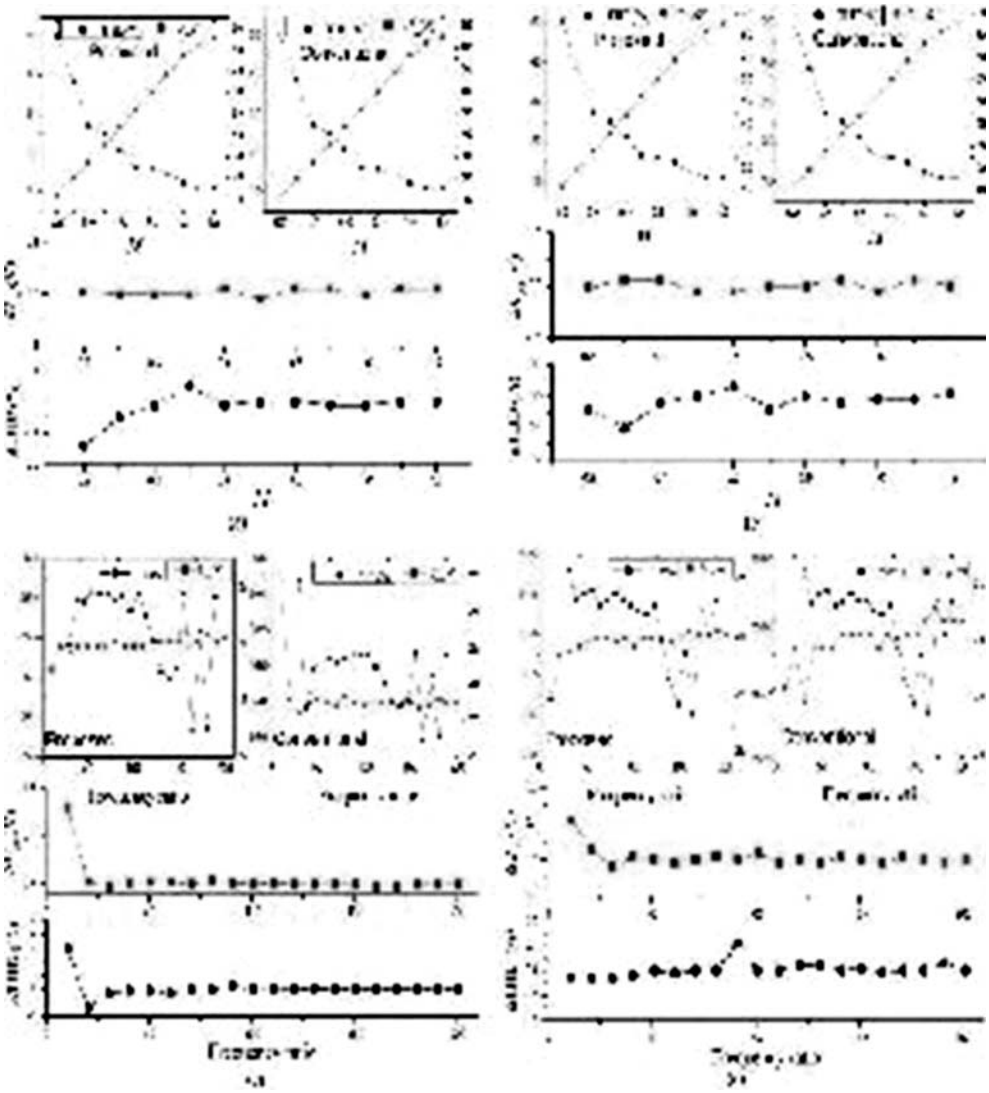

Figure 5: Experimental waveforms of the proposed seven-level SPWMstrategy

The corresponding solution is proposed and depicted as fol- lows. Through forcibly changing the switching states of various power switches around the two zero-crossing points, the output voltage can be clamped at some one special level; thus, the voltage pulse disturbance can be eliminated.

At 0°, before V7 and V8 are both turned off, set V3, V4, and V5 to turn on first. Followed by this operation, all the other power switches are turned off. The corresponding current flowing route is shown in Fig. 5(a). In this case, uout = E/3. Then, turning V8 on after the delay of dead time, if the output current is not equal to zero at the moment of V8 turning on, the flowing direction of the output current will not change, then the current flowing route remains unchanged until the current decays to zero. If the output current has been equal to zero, after V8 is turned on, the flowing route of the output current is switched to the case shown in Fig. 5(*b*); in this case, uout = E/3. At this moment, if setting V4, V5, and V6 to turn on, the output voltage is equal to zero, and the voltage pulse shown in Fig. 5 is eliminated.

In the case of 180°, V2, V3, and V4 are turned on first, and all the other switches are turned off; the corresponding current flowing route is shown in Fig. 6(*a*), and in this case, uout = −E/3. After the duration

of the dead zone, setting V7 to turn on, the current flowing route in the case of the output current equal to zero is shown in Fig. 6(*b*); in this case, uout = −E/3. The voltage pulse disturbance is eliminated at 180◦ in the similar manner.

The experimental results after eliminating the ZCVPD are shown in with the amplitude modulation ratio M = 0.3, 0.5, 0.8, and 1.1, which are corresponding to the cases of three-level,five-level, seven-level, and over modulated output voltage waveforms, respectively. It is shown in these figures that the output voltages within the overall range of the amplitude modulation ratios are all implemented correctly. The waveforms of the low-pass filtered output voltage u1LPF are sinusoidal. The ZCVPDs are eliminated under various amplitude modulation ratios. Thus, the single-phase seven-level

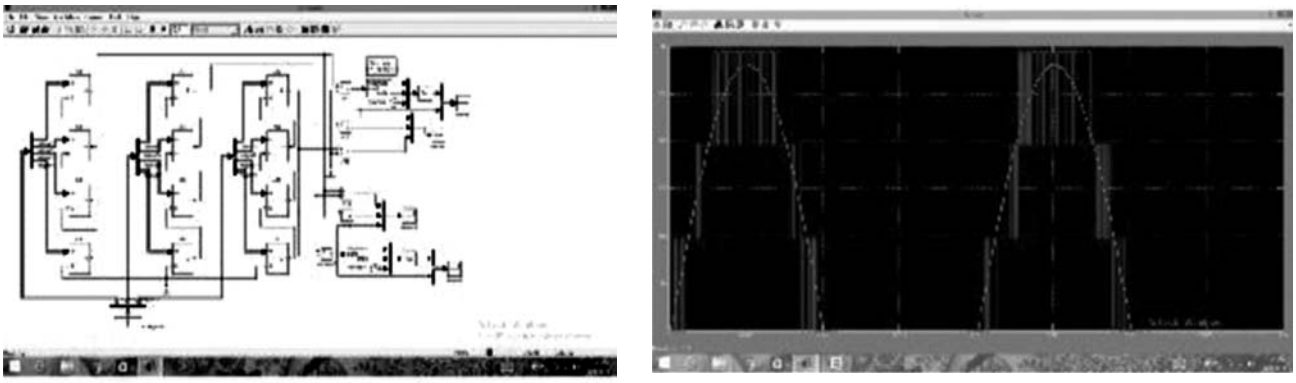

Figure 6: Experimental waveforms of the output voltage and its low-pass filtered voltage under different amplitude modulation ratios. (*a*) M = 0.3. (*b*) M = 0.5. (*c*) M = 0.8. (*d*) M = 1.1

Asymmetrical diode-clamped inverter is correctly driven with a simple multilevel SPWM.

It must be pointed out that, since the voltage pulse disturbances are caused by the non synchronous update of the control signals, this kind of disturbance is not the inherent character of the proposed PWM strategy. From this point of view, the proposed elimination of the disturbance can be also used in other PWM strategies for asymmetrical inverters.

It can be known from (21)–(25) that the spectral characters of the two strategies are different. There exist no harmonics at the carrier frequency and its multiples in the conventional one. No sideband harmonics exist when m and n are both odd or are both even synchronously in the proposed one.

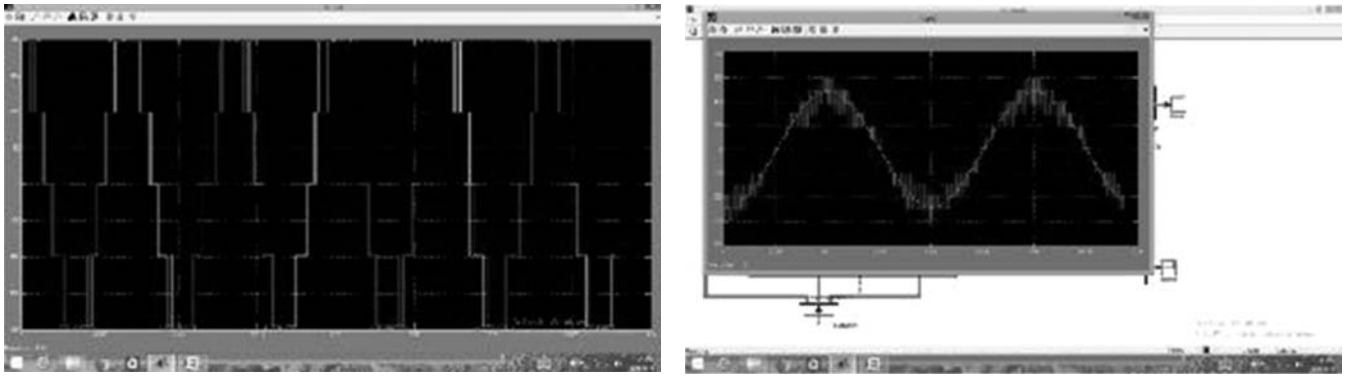

Figure 7: Fast Fourier transforms of output voltages with M = 0.8 and p = 20. (*a*) Conventional. (*b*) Proposed

Since the differences of the spectral characters of the two strategies are not distinct from the theoretical results, the total harmonic distortions (THDs) of the two strategies are compared in the simulation. First, the spectrum with lower frequency ratio (p = 20) and M = 0.8 is simulated, and the results are shown in. The distributions of the spectrum of the two strategies are different, but the THDs are almost the same.

Furthermore, the THDs, the fundamental amplitudes of the output voltage Uout, and their differences with different amplitude modulation ratios and frequency ratios (even ratio and odd ratio) of the two strategies are simulated and shown in.

Uout denotes the differences of the fundamental amplitudes of the output voltages, and THD denotes the differences of the THDs of the output voltages.

Shows the curves with different Ms and the odd frequency ratio $p = 199$. It is shown that, when the frequency ratio is odd, the distribution curves of the THD and the foundational amplitude of the output voltage are alike. The difference of the THDs of the two strategies reaches its maximum (0.05%) when M = 0.5. The difference of the amplitudes of the two strategies is very small during the overall range of M. Fig. 10(b) shows the curves corresponding to M with even frequency ratio ($p = 200$). It is shown that, when the frequency ratio is even, the distribution curves of the THD and the foundational amplitude of the output voltage are also alike. The difference of the THDs of the two strategies reaches its maximum (0.1%) when M = 0.3.

The difference of the amplitudes of the two strategies is very small during the overall range of M. Shows the curves with different odd frequency ratios and M = 0.8. It is shown that, when the frequency ratio is very small (less than 29), there is a bit difference in the changing trend Therefore,intheactualsystem,theperformanceofthe proposed strategy is as good as the conventional one; it means that the proposed strategy can entirely replace the conventional one. The complexity of the system is reduced, and the reliability, as well as the capacity, of resisting disturbance is enhanced. Shows the curves with different even frequency ratios and M = 0.8. It is shown that, within the overall range of the frequency ratio, the two THD curves are very close. Just at the point of $p = 90$, the difference reaches its maximum (0.15%). The shapes of the two amplitude curves are somewhat different. The maximum arises at the point of $p = 10$, which is equal to 0.1.

The frequency ratio of two curves becomes smaller and gradually increases, the difference of the curves, and the maximums are 3% and 0.8, respectively When When the frequency ratio is higher, the differences of THDs of the two strategies have been already very tiny and almost can be ignored. Therefore, in the actual system, the performance of the proposed strategy is as good as the conventional one; it means that the proposed strategy can entirely replace the conventional one. The complexity of the system is reduced, and the reliability, as well as the capacity, of resisting disturbance is enhance.

6. SIMULATION DIAGRAM

In this we are using 6 MOSFET. In which input is given as an AC supply which is connected to the grid. It is also used to improve the voltage stability with the help of the driver circuit. Here we are using step down transformer to step down the voltage and with the help of the switching circuit we obtain the output which can we practically verified with the help with the help of the single phase motor (or) CRO.

7. SIMULATION RESULT

This is the 13th level pulse generation output. The output range varies from 0.1 to 0.8.In this output range varies from 1.0 to 1.8. This is 13th multilevel inverter voltage waveform.This waveform is voltage fluctuation amplitude voltage waveform. The voltage range varies from 0.001 to 0.2 will be produced on the output waveform.

8. CONCLUSION

The proposed SCMM-SPWM strategy suitable for control- ling the single-phase seven-levelasymmetrical diode-clamped inverter has been implemented with only one DSP chip without any other attached logical circuit or controller. The elimination of zero-crossing disturbance in the former asymmetrical inverter is proposed as well. The experimental results verify its accuracy and feasibility. The theoretical and are also simulated comparison results of the also spectral characters between the proposed and the conventional one indicate that the also SCMM-SPWMhas the similar performance with the conventional one. The proposed strategy can entirely replace the non-conventional one to drive multilevel inverter.

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