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High Density Asynchronous Lut Based on Nonvolatile RRAM

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ABSTRACT

Emerging non-volatile memories (NVMs), such as MRAM, PRAM, and RRAM have been widely investigated to replace SRAM and the configuration bits in field-programmable gate arrays (FPGAs) for high security and instant power ON. However, the variations inherent in NVMs and advanced logic process bring reliability issue to FPGAs. A single-stage sense amplifier with voltage clamp is employed to reduce the power and area without impairing the reliability. Matched reference path is proposed to reduce the parasitic RC mismatch for reliable sensing. RRAM is adopted as the configuration bit and the reference resistor to provide large sense margin, thus all eviating the effects of memory and logic process variations. By evaluation, remarkable improvements in power, delay, area, and reliability can be obtained.

Keywords: low power, high speed, RRAM, FPGA- (Field Programmable Gate Array), non-volatile SRAM (nvSRAM).

1. INTRODUCTION

Basic NVMs, such as MRAM, PRAM, and RRAM, have been verified with better scalability and logic compatibility. Based on the logic-in-memory concept, lookup table, which is the core building block in FPGAs, has been introduced with non-volatility. First, various nonvolatile SRAM (nvSRAM) structures with MRAM and RRAM were proposed to directly replace SRAM in the traditional lookup table to acquire non-volatility. However, the size of nvSRAM cell is remarkably larger than that of SRAM, and the write disturbance is also difficult to avoid for half-select RRAM cells. Look Up Table combined with NVM method has been proposed. Various NVSRAM with MRAM and RRAM replaces SRAM. But the drawback is that the area requirement is more in the approach. It has been proposed that a 2 input Nonvolatile memory Look Up Table for run-time reconfiguration. Third type is a hybrid-LUT for MRAM. Drawback -Roff/Ron for MRAM <PRAM or RRAM> which results in less sense margin and larger area. It has larger Roff/Ron ratio 1T1RAM cell has been used as the configuration bit and a reference resistor has been used to provide sufficient sense margin. Single-stage amplifier with voltage clamp is employed to reduce power and area. MRP has been devised to reduce parasitic RC mismatch between selected path in MUX and reference path for reliable sensing against logic variation, lowpower, high area efficiency, and low leakage at the same time.

1.1. Resitive Random Access Memory (RRAM)

This prototype consists of a traditional island-style FPGA (Field Programmable Gate Array)- fabricated in 90nm CMOS technology, on top of which the programmable resistors are integrated. Apart from the configuration memory, all other parts are constructed purely with CMOS transistors. The memory array is interleaved with the CMOS logic throughout the tile. Write drivers, row and columns decoders and sense

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amplifiers are shared by the FPGA tiles. Memory cells are constructed using a 1T2R topology, in which two programmable resistances (or PRs) behave as a voltage divider, pulling the bit line – connected to the cell through the access transistor – up or down. RRAM PRs are small when compared to the CMOS feature size, allowing for an optimized cell surface of only 24 F2.

1.2. FPGAs

An FPGA (Field Programmable Gate Array) is a reprogrammable chip which contains hundreds of thousands of logic gates that internally connects together to build complex digital circuitry. There are few steps given below. It is primarily a semiconductor device that can be configured by the user (customer or designer) after the manufacturing process has been completed. The term "field-programmable" means the device is programmed by the customer, not the manufacturer. It offers partial re-configuration of a portion of design.

2. SINGLE STAGE SENSE VOLTAGE AMPLIFIER

It has less power dissipation and offset in comparison of basic differential voltage sense amplifier. The simultaneous switching of load devices is fundamental advantage of differential voltage sense amplifier in obtaining fast sensing operation. SSAVC converts the resistance state of RRAM in to rail-to-rail logic voltage. when clock is low out and outb are precharge to vdd when clock is high it sense the output. The charges are discharged to a capacitor or ground when CLK is high, resulting in considerable power waste. The voltage clamp may incur reduced currents into the sense amplifier, large *R*OFF/*R*ON of RRAM still helps to preserve the sense margin without impairing the reliability. Compared with the previous two-stage sense amplifier, the single-stage realization occupies less die area. Applying a proper clamp voltage *V*bias, which is lower than *V*DD, on the gates of M7 and M8, the inner nodes of the selected path in TMUX and MRP can only be precarged to (*V* bias-*V*th).

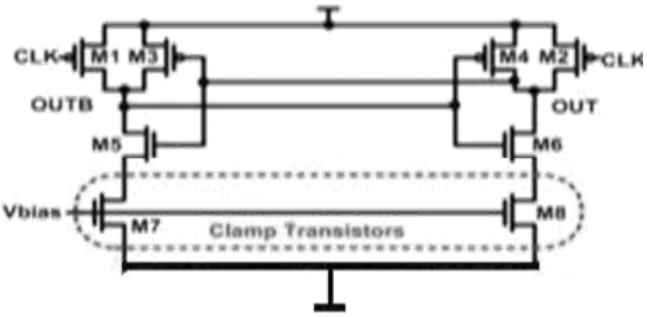


Figure 1: Single-Stage Sense Amplifier with Voltage Clamp

DESIGN OF SINGLE STAGE SENSE AMPLIFIER WITH VOLTAGE CLAMP

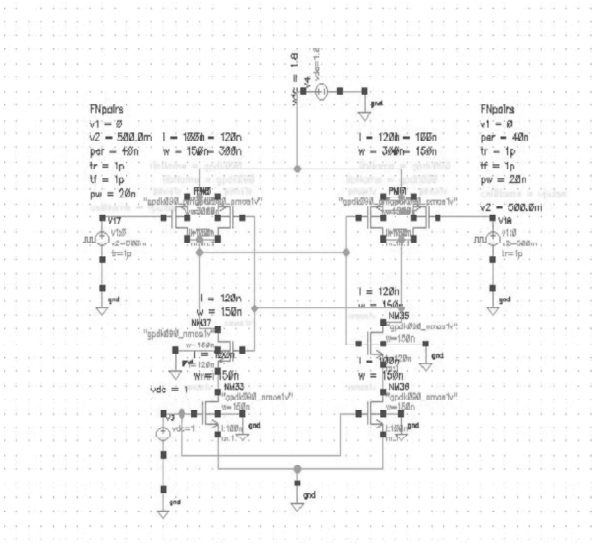


Figure 1.1: Schematic of single-stage sense amplifier with voltage clamp

Waveform

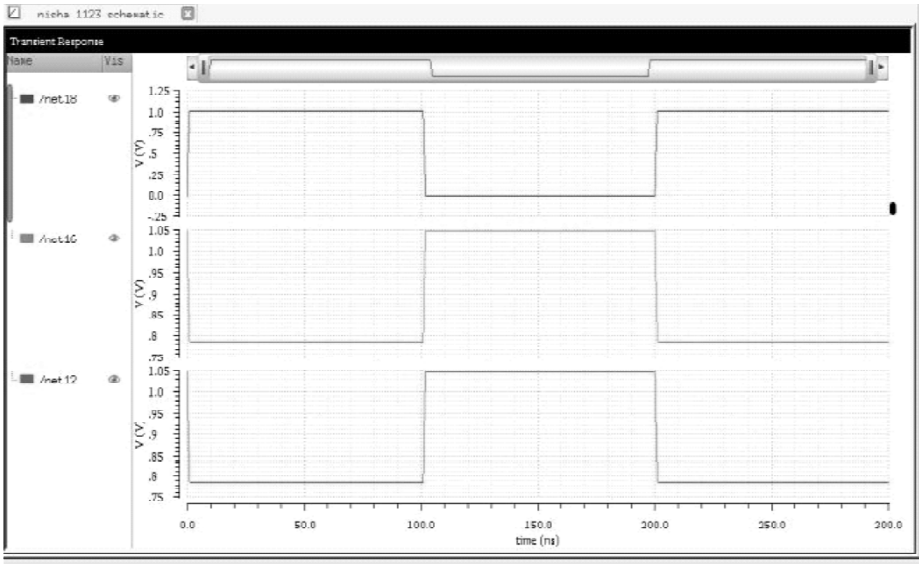


Figure 1.2: Transient Response of single-stage sense amplifier with voltage clamp

3. TERMINAL MULTIPLEXER

TMUX is a multiplexer with select line in0 and in1 which are used to select the corresponding rram . Its working principle is similar to nor operation.

IN0	*IN1*	*OUT*
0	0	R0
0	1	R1
1	0	R2
1	1	R3

4. PROPOSED LOW POWER VARIATION TOLERANT NVLUT

To illustrate design, a two-input nvLUT is presented, as shown in Fig. 3 The input count can also be easily extended to six, which is prevailing in current main-stream FPGA products. The overall architecture of nvLUT consists of an SSAVC, a tree multiplexer (TMUX), an MRP, a RRAM slice, and a footer transistor. The RRAM slice constitutes of four 1T1R RRAM cells at the left for configuration and a dummy RRAM

Table
Specifications of Proposed Design

Module	*Device*	*W/L*
SSAVC	M1,M2	150nm/100nm
	M3,M4	300nm/120nm
	M5,M6	150nm/120nm
	M7,M8	150nm/100nm
TMUX	MP1 to MP6	300nm/100nm
MRP	MP7 to MP10	300nm/100nm
RRAM	MA0,MA1,MA3,MAref	300nm/100nm
Footer	MF	500nm/100nm

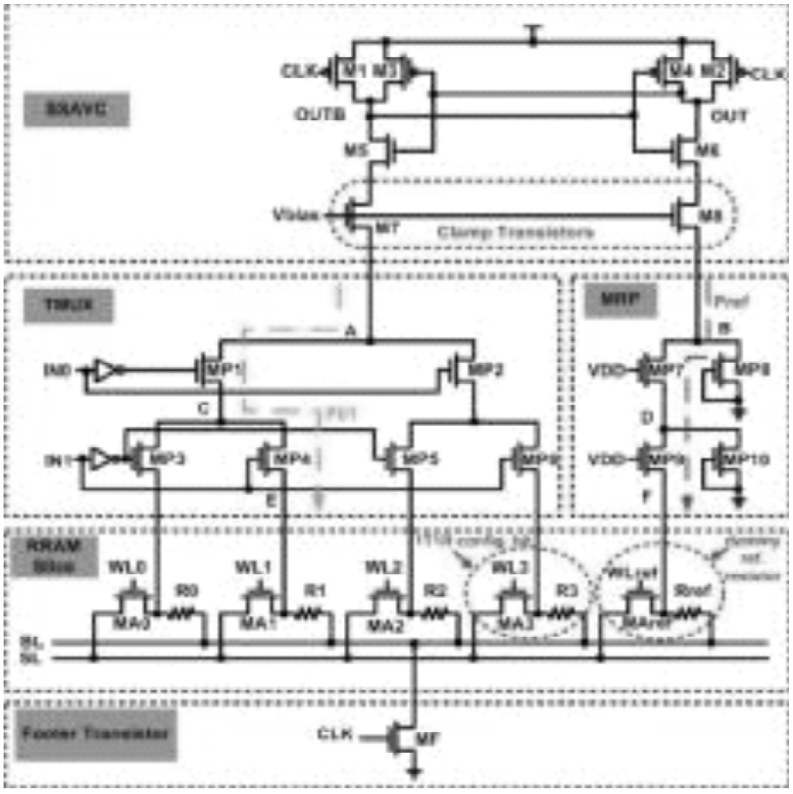


Figure 3: Low- power variation-tolerant nvLUT based on RRAM

cell at the right-most as a reference resistor. The truth table is stored in the RRAM slice in the form of resistance state, *R*OFF or *R*ON, which is different from the logic voltage in SRAM. For example, in order to program the nvLUT as a NOR gate, R0 should be programmed as *R*ON denoting 1, while R1, R2, and R3 should be programmed as *R*OFF denoting 0. The inputs IN0 and IN1 select the corresponding RRAM cell through TMUX.

The excessive parasitic *RC* in RRT may slow down the discharging of the reference path, making the sense amplifier prone to output 1 when the resistance margin between the configuration bit and the reference resistor is subtle due to memory variation.

DESIGN OF LOW-POWER VARIATION-TOLERANT NVLUT FOR RRAM

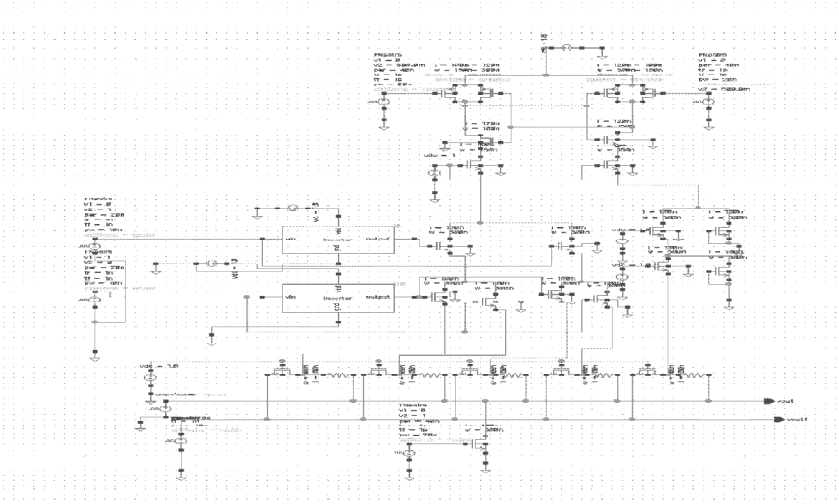


Figure 3.1: Schematic of Low-power Variation-Tolerant nvLUT

Waveform

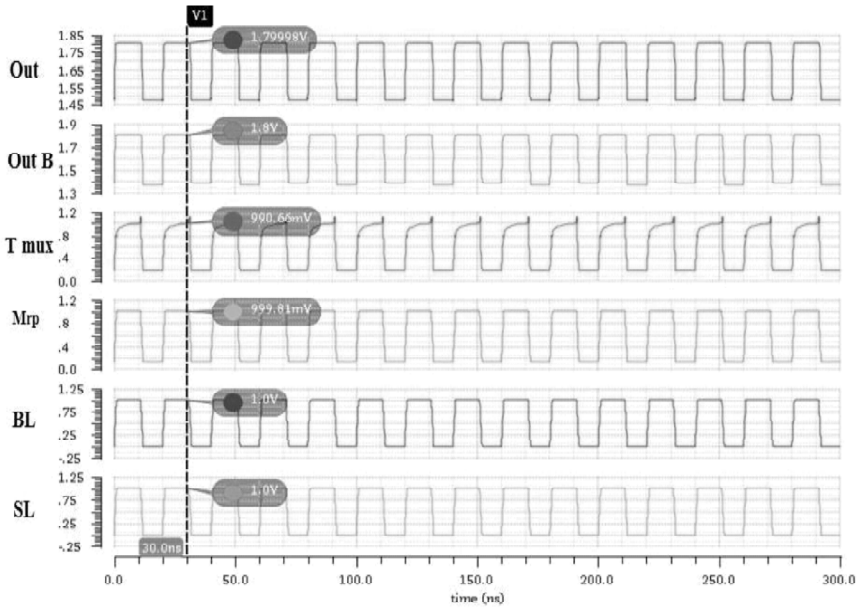


Figure 3.2: Transient Response of Low-power Variation-Tolerant nvLUT

WAVEFORM FOR DELAY CALCULATION

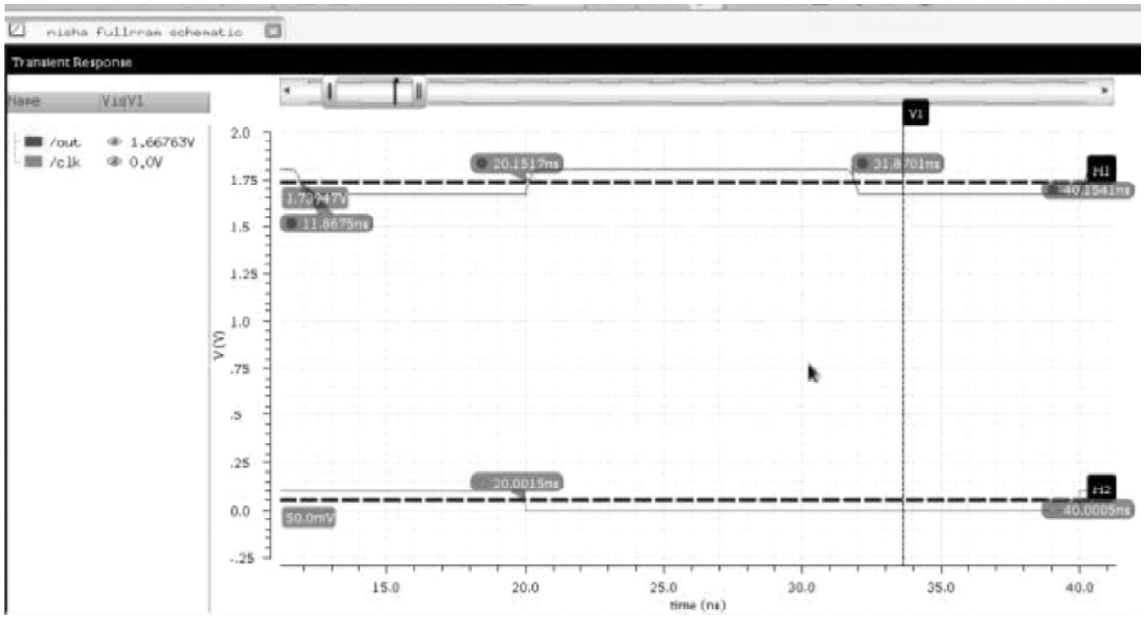


Figure 3.3: Transient Response of Delay calculation

Table 1
Delay Calculation for Rref-20K

Vbias (v)	*Clock*	*Out*	*Delay(ps)*
0.6	152.10621ns	151.86024ns	345ps
0.7	100.001ns	100.1706ns	198ps
0.8	100.0015ns	100.2005ns	164ps
1	100.0015	100.2165	150ps

Table 2
Delay Calculation for Rref-50K

Vbias (v)	*Clock*	*Out*	*Delay(ps)*
0.6	152.10621ns	151.8024ns	360ps
0.7	40.24771ns	40.00063ns	247ps
0.8	40.2285ns	40.0005ns	228ps
1	60.0014ns	60.1779ns	176ps

Table 3
Delay Calculation for Rref-100K

Vbias(v)	*Clock*	*Out*	*Delay(ps)*
0.6	20.00015ns	20.4727ns	400ps
0.7	40.0004ns	40.2699ns	269ps
0.8	40.00058ns	40.23375ns	233ps
1	60.0012ns	60.2086ns	206ps

DELAY VS VBIAS

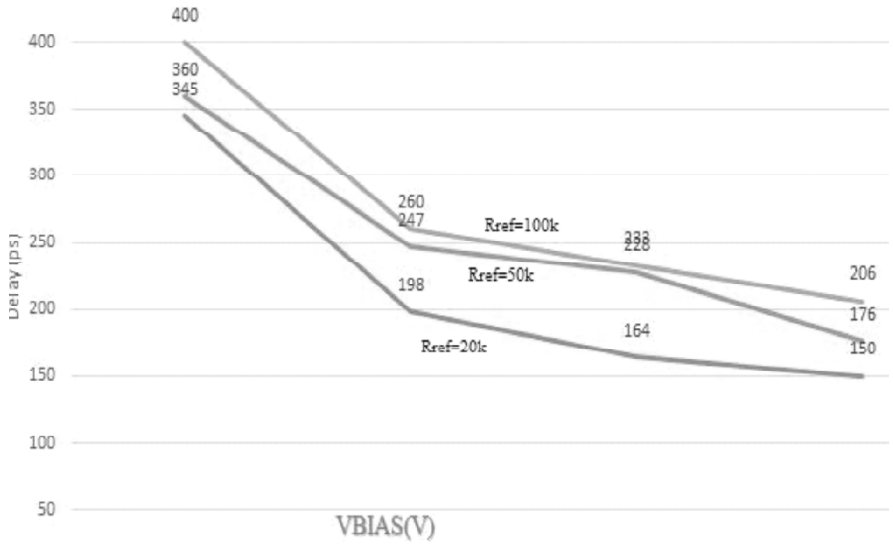


Figure 3.4: Delay of Low Power Variation Tolerant nv LUT with Vbias for different Rref value

POWER CALCULATION

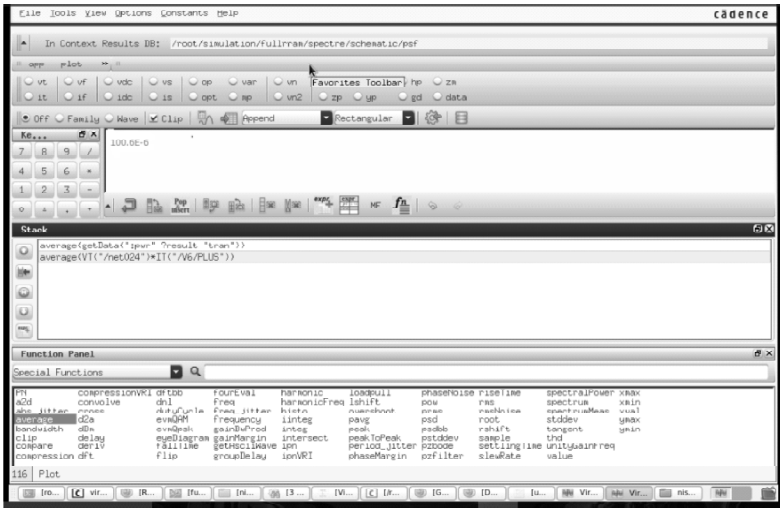


Table 4
Power Calculation

Vbias (v)	*Rref=20K*	*Rref=50K*	*Rref=100K*
	Power	*Power*	*Power*
0.5	100.6E-6	100.5E-6	100.5E-6
0.6	100.8E-6	100.7E-6	100.7E-6
0.7	101.1E-6	101.0E-6	100.9E-6
0.9	101.3E-6	101.4E-6	101.3E-6
1	101.5E-6	101.6E-6	101.6E-6

POWER VS VBIAS

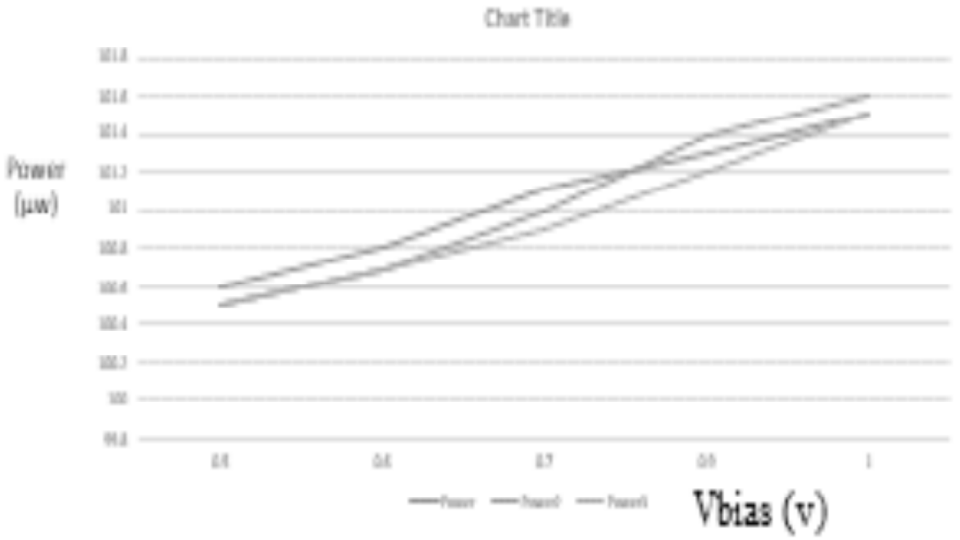


Figure 3.5: Power of Low Power Variation Tolerant nvLUT with Vbias for different Rref value

Table 5
Product Calculation for Rref-20K

Vbias (v)	*Delay(ps)*	*Power (µW)*	*Product (ps*µW)*
0.6	345	100.8E-6	34.776E-15
0.7	198	101.1E-6	20.017E-15
0.8	164	101.3E-6	16.613E-15
1	150	101.5E-6	15.225E-15

Table 6
Product Calculation for Rref-50K

Vbias (v)	*Delay(ps)*	*Power (µW)*	*Product (ps*µW)*
0.6	360	100.7E-6	36.525E-15
0.7	247	101.0E-6	20.017E-15
0.8	228	101.4E-6	23.119E-15
1	176	101.6E-6	17.881E-15

Table 7
Product Calculation for Rref-100K

Vbias (v)	*Delay(ps)*	*Power (μW)*	*Product(ps*μW)*
0.6	360	100.7E-6	36.525E-15
0.7	269	100.9E-6	27.142E-15
0.8	233	101.3E-6	23.602E-15
1	206	101.6E-6	20.929E-15

PRODUCT VS VBIAS

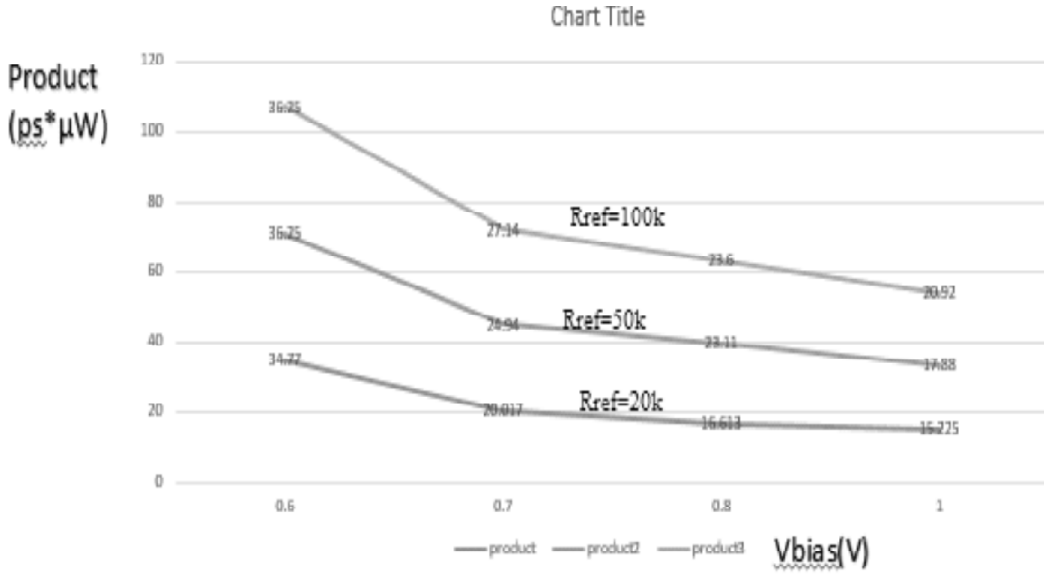
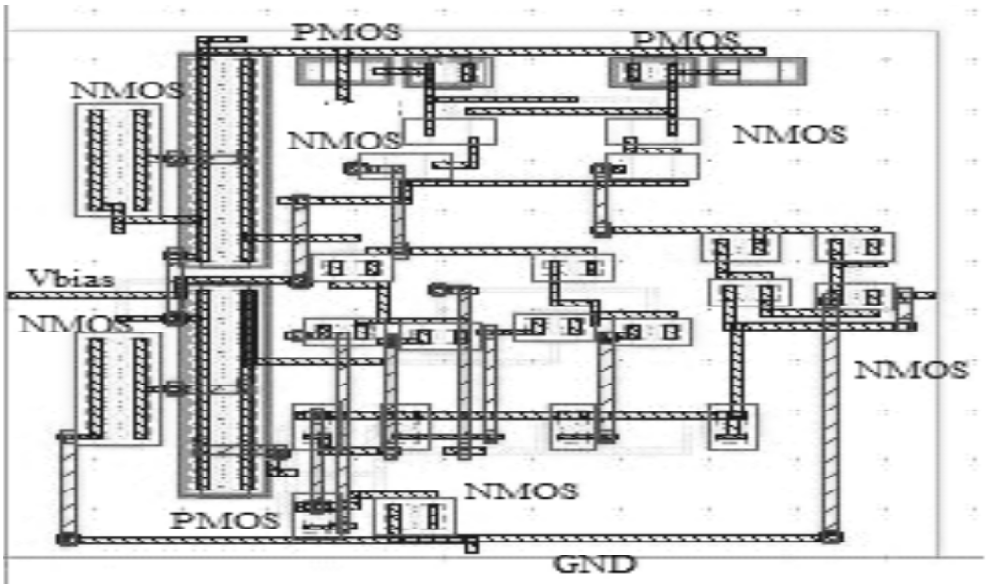


Figure 3.6: Product of Low Power Variation Tolerant nvLUT with Vbias for different Rref value

Layout OF LOW-POWER VARIATION-TOLERANT nvLUT FOR RRAM



Blue=Metal 1, Red=metal 2, yellow=polysilicon
X axis - 10.5000μm, Y axis – 10.4000μm
Area of LUT based on RRAM = 109.2 μm^2

CONCLUSION

The design techniques of high density asynchronous look up table based on RRAM is described. RRAM is adopted as the configuration bit and the reference resistor to provide large sense margin, thus alleviating the effects of memory and logic process variations. Because of the high *R*OFF/*R*ON of RRAM, SSAVC helps to reduce the power and area without impairing the reliability. The MRP is also devised to reduce the parasitic *RC* mismatch between the selected path in the multiplexer and the reference path for reliable operation. The layout of proposed design for high density asynchronous LUT based on Nonvolatile RRAM is implemented using cadence design environment and calculated area of layout is about 109.2 μm^2.

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