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Harmonic Reduction in a Neutral Point Clamped Multilevel Inverter

Murali Venkata Sai* Meenakshi Jayaraman and Sreedevi V.T.*****

Abstract : Multilevel inverters are gaining popularity in renewable energy applications today. This paper presents the configuration of a three level and five level Neutral Point Clamped inverter. Phase Disposition Sinusoidal Pulse Width Modulation strategy is employed to generate switching pulses for both the multilevel inverters. Using the modulation technique, the output voltage, output current and harmonic spectrum of both the inverters are obtained. Further, this work presents the design of a passive LC filter to reduce harmonic distortions from the multilevel inverter output. The performance of the designed filter is studied by analyzing the output waveforms and the harmonic spectrum obtained after connecting the designed filter to the inverter output. All the simulations are carried out in MATLAB-Simulink simulation platform. It is found that the designed filter keeps the output harmonics within IEEE standards.

Keywords : Neutral Point Clamped (NPC), Total Harmonic Distortion (THD), Harmonics, Phase Disposition Pulse Width Modulation (PDPWM).

1. INTRODUCTION

The requirement for high power converters which are able to produce better quality waveforms while using low voltage devices and operating at lower switching frequencies has paved way to the development of multilevel inverters [1]-[3]. Multilevel inverters include a series of semiconductor devices and voltage sources to develop a stepped output voltage waveform. Striking features of multilevel inverters include good power quality, better electromagnetic compatibility, smaller ripple current, lesser losses in the semiconductor switches, and capability to generate high voltages. Multilevel inverters find applications ranging from low voltage ratings to high voltages such as renewable energy systems, motor drives, FACTS devices etc. Various multilevel inverter circuits have been developed in the literature [4]-[7]. The basic multilevel inverter circuits are the diode clamped inverter topology, flying capacitor topology and cascaded H-bridge inverter topology. A Cascaded H-bridge inverter [3] consists of a series connection of single phase inverters. This inverter configuration is simple when compared to other inverters, though they carry more devices as the levels increase. The flying capacitor inverters [4] use balancing capacitors instead of diodes and produce a multilevel output clamped by the capacitors. Higher level inverters require more capacitors which increases balancing issues in the system. Diode clamped inverters also known as Neural Point Clamped (NPC) inverters [8],[9] use clamping diodes in their structure. They possess less number of DC voltage sources when compared to the conventional cascaded inverters. These inverters have high efficiency at fundamental frequency switching. To generate pulses for these multilevel inverters, various Pulse Width Modulation (PWM) strategies are employed such as Sinusoidal PWM [10],[11], Space Vector

* M.Tech. Power Electronics and Drives, School of Electrical Engineering, VIT University, Chennai, India, 600127

** Assistant Professor, School of Electrical Engineering, VIT University, Chennai, India, 600127 Email: jayaraman.meenakshi@gmail.com

*** Professor, School of Electrical Engineering, VIT University, Chennai, India, 600127.

PWM [12], Selective Harmonic Elimination [13] etc. In sinusoidal PWM strategy, which is considered the simplest modulation method, a comparison between a reference sine wave and a triangular carrier wave is done to produce switching pulses for the multilevel inverter. Carrier based SPWM techniques have been developed in which the number of levels of the inverter output decides the number of carrier triangular waves. The variants in multicarrier modulation strategies are the Phase Shifted PWM, Level Shifted PWM, Phase Opposition Disposition (POD) PWM and Alternate APOD PWM [10]. Though the output from multilevel inverters with a well-designed modulation strategy shows improved output waveforms when compared to conventional voltage source inverters, yet the output waveforms carry an appreciable amount of harmonic distortion which is not permitted as per IEEE standards [14]. In order to achieve less harmonic distortion content on the output waveforms, filters are employed with multilevel inverters. Generally, a lower order LC filter is connected with a voltage source inverter to reduce the harmonics [15]-[18]. At resonance, as impedance of the inductor and capacitor branches become equal in a LC filter, the circuit provides less impedance path thereby high amount of current flows in the circuit resulting in losses and creates damping oscillations. To avoid this problem, a resistor is connected in series with the capacitor to reduce resonant damping.

In this paper, the configuration of a three level and five level NPC inverter is presented. Multicarrier PDPWM technique is employed to generate gating pulses the inverter switches. The waveforms obtained on the output of both the inverters along with their harmonic spectrum are analysed and a performance comparison is established. Further a passive LC filter is designed for the NPC inverter in order to reduce the harmonic content on its output waveforms. The filter parameters are chosen based on the value of the resonant frequency and the filter effectiveness is analysed using different inductor values and cut off frequency values. The output voltage, output current and harmonic spectra of the output voltage and current waveforms is obtained for the NPC inverter with the designed passive filter. As the LC filter is a second order filter, it attenuates the harmonics at a rate of -40 dB/decade which reduces the harmonic distortions on the inverter output significantly which satisfies IEEE standards.

This work is presented as below: Section 2 represents the operation of a three level and five level NPC inverter. Section 3 briefs on the PDPWM technique, Section 4 provide the filter design. Section 5 shows the simulation results. Section 6 gives the conclusion.

2. NEUTRAL POINT CLAMPED (NPC) MULTILEVEL INVERTER

(*a*) Three level NPC inverter configuration

A three level inverter NPC inverter is shown in Fig. 1. It consists of four semiconductor switches, Q1 to Q4 with two diodes, D1 and D2. Two capacitors, C1 and C2 are connected across the DC source which splits the input DC voltage equally.

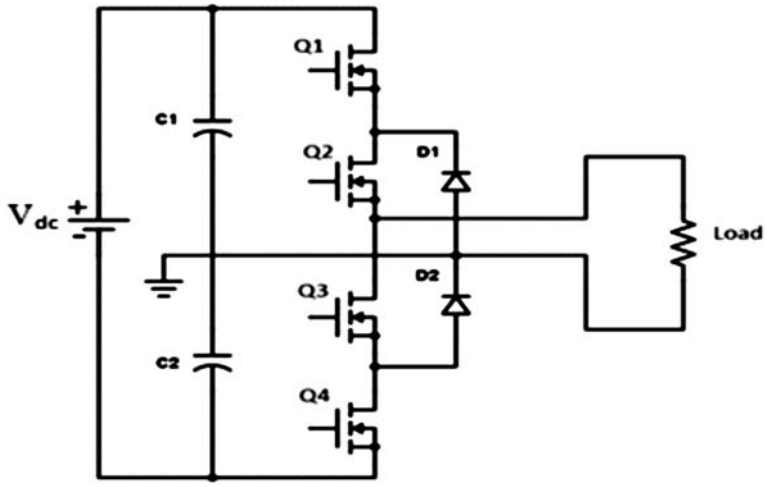

Fig. 1. Three level NPC inverter.

Table 1. Switching pattern for three level NPC inverter.

Switches	$V_{dc}/2$	*0*	$-V_{dc}/2$
Q1	High	Low	Low
Q2	High	High	Low
Q3	Low	High	High
Q4	Low	Low	High

The midpoint of the two capacitors is connected to the neutral. The capacitors connected across the supply are charged to $V_{dc}/2$. When Q1 and Q2 are ON, $V_{dc}/2$ level is obtained. When Q2 and Q3 are ON, zero output voltage is obtained. When Q3 and Q4 are ON, $-V_{dc}/2$ is obtained. The switching pattern for the three level NPC inverter is shown in Table 1.

(*b*) Five level NPC inverter configuration

In a five level NPC inverter, eight semiconductor switches SW1-SW8 and four diodes D1-D4 are used to realize a five level output. The purpose of the four diodes is to clamp the output voltage. The midpoint of the two diodes in each leg is connected to the neutral point. The neutral point is connected to the midpoint of the two capacitors C1 and C3. Fig. 2 shows a five level NPC inverter. When switches SW1, SW3, SW6 and SW4 are ON then V_{dc} is obtained on the output voltage. When switches SW1, SW3, SW6 and SW8 are ON, the output voltage is $V_{dc}/2$. When switches SW5, SW7, SW6 and SW8 are ON, 0 V is obtained at the output. When switches SW5, SW7, SW6 and SW4 are ON, $-V_{dc}/2$ level voltage is obtained. When switches SW6, SW5, SW7 and SW4 are ON $-V_{dc}$ is obtained. The switching pattern for the five level NPC inverter is shown in Table 2.

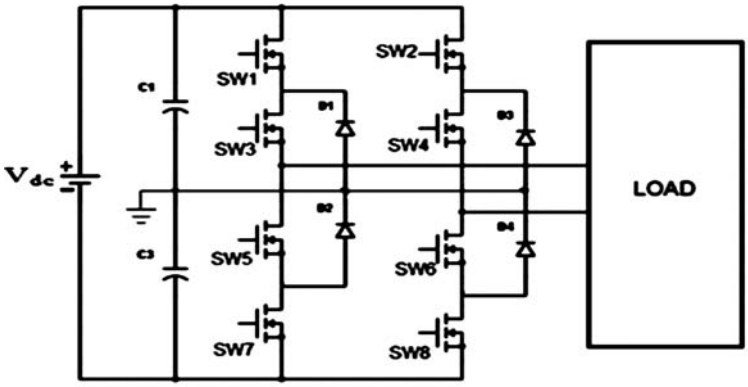

Fig. 2. Five level NPC inverter configuration.

Table 2. Switching pattern for the switches of five level NPC inverter.

Output level (V)	*SW1 SW5*	*SW7 SW3*	*SW2 SW6*	*SW8 SW4*
V_{dc}	High	Low	Low	High
$V_{dc}/2$	High	Low	Low	High
0	Low	High	Low	High
$-V_{dc}/2$	Low	High	Low	Low
$-V_{dc}$	Low	High	High	Low

3. PHASE DISPOSITION PULSE WIDTH MODULATION

In this paper, PDPWM strategy is used to obtain switching pulses for the switches of the three level and five level NPC inverter. The principle of PDPWM is based on the comparison of a sine signal with triangular carrier wave signals. '*b*-1' carriers are used to generate '*b*' levels on the output. The carriers are arranged in continuous bands around the reference zero. They have the same amplitude and frequency equal to the designed switching frequency. The comparison output is 'High' if the sine signal is lower than the triangular signal and 'Low' otherwise. The addition of the comparator outputs gives the output of the modulator which represents inverter output voltage level. This strategy is shown in the Fig. 3.

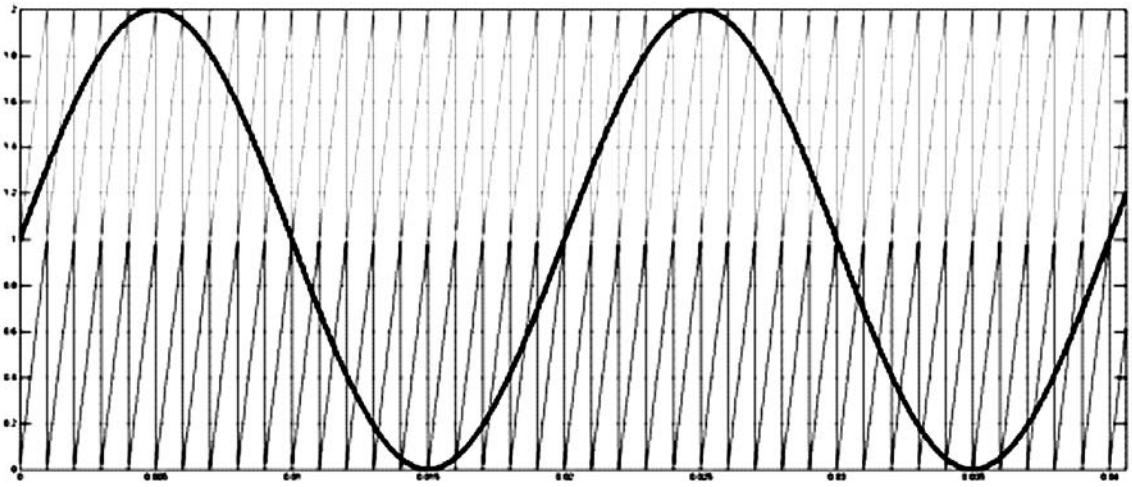

Fig. 3. PDPWM technique for three level NPC inverter.

4. DESIGN OF LCR FILTER FOR NPC INVERTER

To improve the waveform quality of the NPC inverter output and to reduce the harmonic distortion on the output waveforms, a LCR filter is designed in this work. Fig. 4 shows the LCR filter that is connected to the output of the five level NPC inverter where L_1 is the filter inductor, C_1 is the filter capacitor and R_d is the damping resistor.

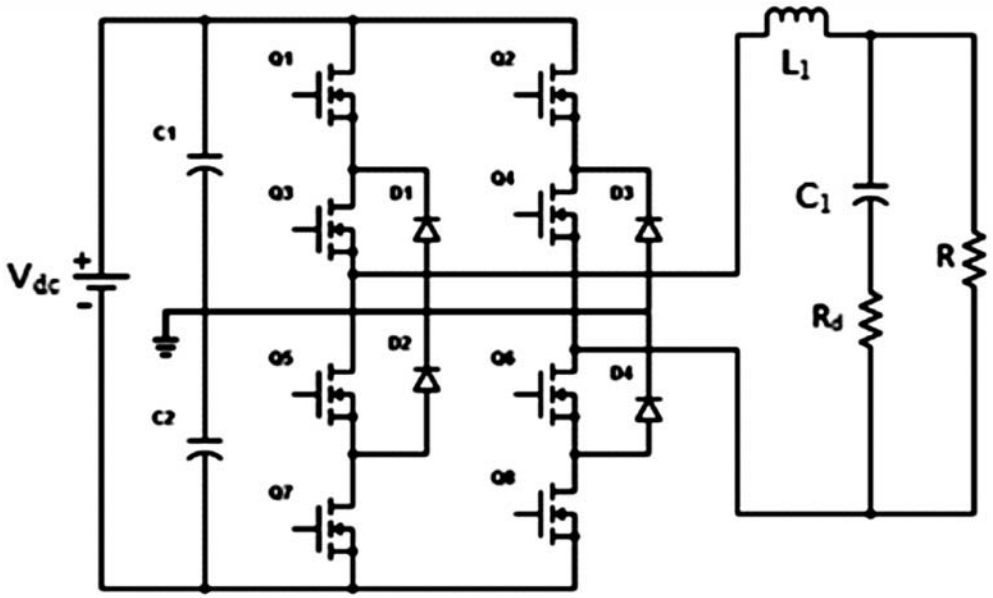

Fig. 4. Five level NPC inverter with LCR filter.

The transfer function of the LCR filter system is given by Eq. (1).

$$\frac{V_0}{V_i} = \frac{S\frac{R_d}{L_1} + \frac{1}{L_1C_1}}{S^2 + S\frac{R_d}{L_1} + \frac{1}{L_1C_1}} \quad (1)$$

where V_o is the output across the load resistance R and V_i is the inverter output which can be rewritten as Eq. (2).

$$\frac{V_0}{V_i} = \frac{2\xi\omega_0 + \omega_0^2}{2^2 + 2\xi\omega_0 + \omega_0^2} \quad (2)$$

where $\omega_0 = \frac{1}{\sqrt{L_1C_1}}$ is the cut-off frequency and $\xi = \frac{R_d}{2\sqrt{\frac{L_1}{C_1}}}$ is the damping ratio.

If the damping ratio is more than one, at low frequency the attenuation is constant. Hence the damping ratio is chosen be less than unity. The LCR filter cut-off frequency is to be sufficiently low value to get the required attenuation ratio. The filter system is designed such that at fundamental frequency, the voltage drop across the filter inductor L_1 is less than 5% of the rated output voltage [14],[14]. The filter capacitor C_1current is designed such that it does not exceed 10% of rated system current. To minimize damping, larger values of the damping resistance value is chosen.

In this paper, the inductor impedance of the LCR filter is selected to be lower than 5% of the total load impedance to attain better harmonic reduction and reduced filter size [14]. The output load resistance is chosen as 50 Ω. Accordingly, the filter inductor (L_1) reactance is $X_L = 50 \times 5\% = 2.5\ \Omega$ which gives $L_1 = \frac{2.5}{2 \times \pi \times 50} = 8$ mH. If the cut-off frequency is taken as 800 Hz (usually chosen to be between five times the fundamental frequency and half the switching frequency), then the LCR output filter capacitor is taken as $\omega_0 = \frac{1}{\sqrt{L_1C_1}}$ which gives the filter capacitor values as $C_1 = \frac{1}{\omega_0^2 L_1} = \frac{1}{(2 \times \pi \times 800)^2 \times 8 \times 10^{-3}} = 5\ \mu$F. If damping ratio is taken as 0.2, then R_d is selected as $R_d = 0.2 \times 2\pi \times \sqrt{\frac{L_1}{C_1}} = 0.2 \times 2\pi \times \sqrt{\frac{8 \times 10^{-3}}{5 \times 10^{-6}}} = 50\ \Omega$.

5. RESULTS AND ANALYSIS

The three level and five level inverter configurations are simulated in MATLAB-Simulink environment. The parameters used for the design and simulation are shown in Table 3.

Table 3. Design Specifications

Parameter	*Value*
Input DC voltage	110 V
Switching frequency	5 kHz
Rated output power	200 W

(*a*) Results with three level NPC inverter

The simulation model of a three level NPC inverter is shown in the Fig. 5.

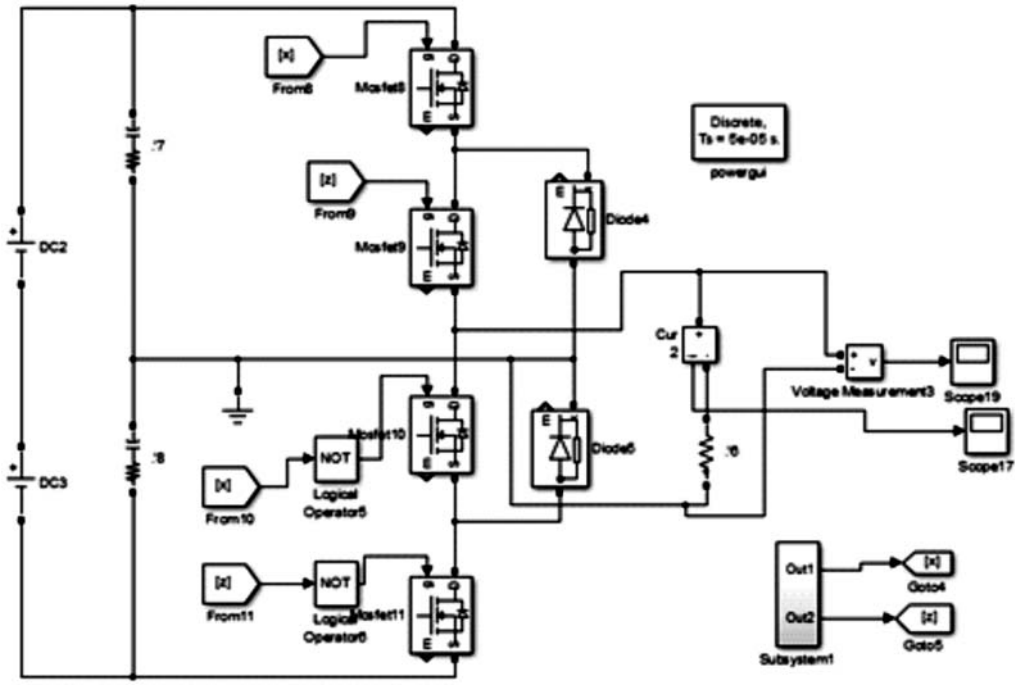

Fig. 5. Simulation model of three level NPC inverter.

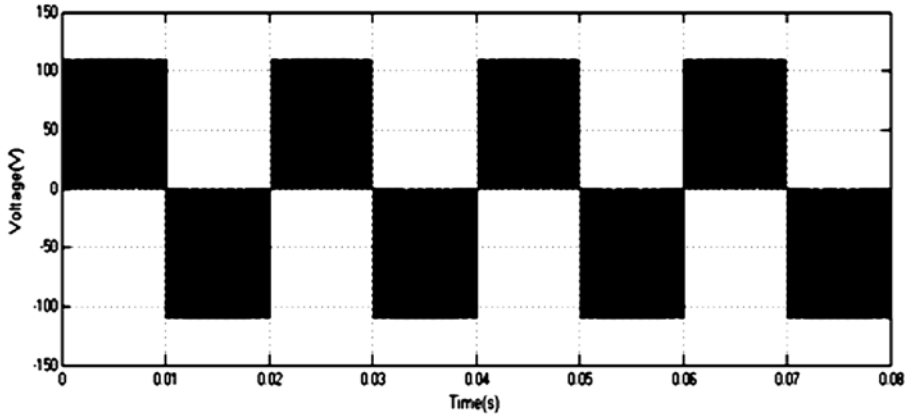

Fig. 6. Output voltage of three level NPC inverter.

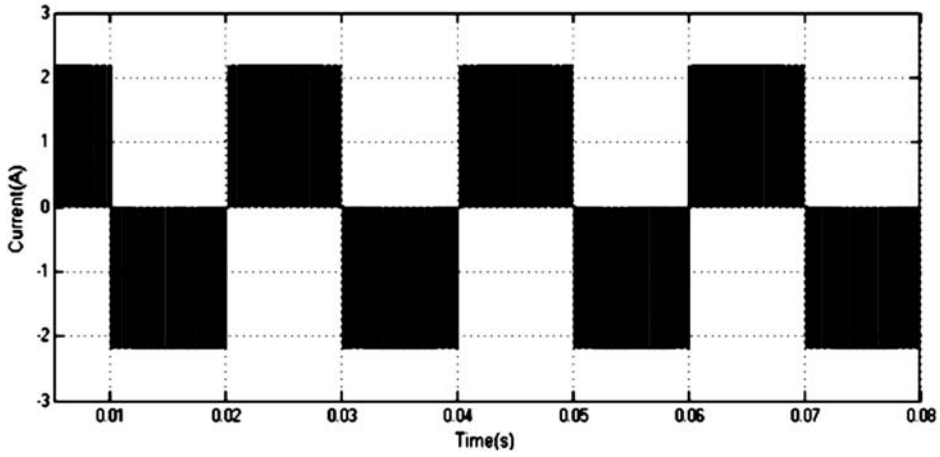

Fig. 7. Output current of three level NPC inverter.

The output waveforms obtained from the three level NPC inverter are shown in Fig. 6 and Fig. 7. It can be seen from the waveforms that the output voltage has three levels on the output and the current waveforms follow the voltage waveforms. The harmonic spectrum obtained for the output voltage waveform is shown in Fig. 8. The THD on the output waveforms of the three level NPC inverter for a modulation index of unity is observed to be 77.17%.

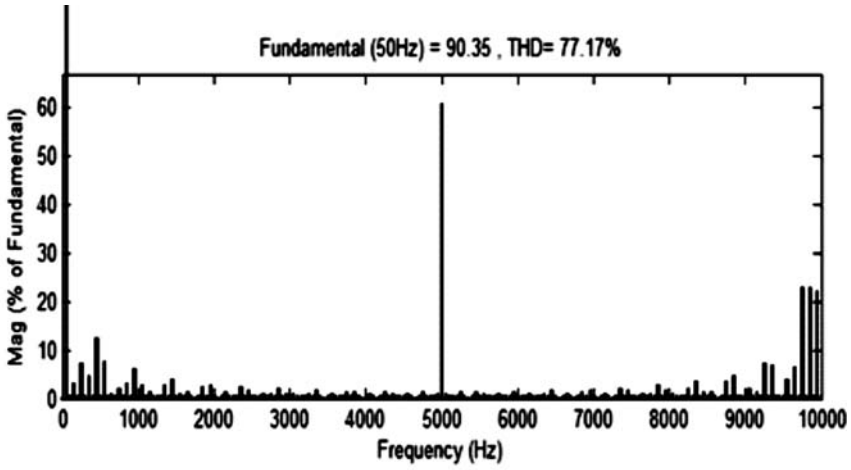

Fig. 8. Harmonic spectrum of three level NPC inverter.

(*b*) Results with five level NPC inverter

The output waveforms obtained from the five level NPC inverter are shown in Fig. 9 and Fig. 10 respectively. The output voltage has five levels on the output and the current waveforms follow the voltage waveforms as seen from Figs. 9 and 10. The harmonic spectrum for the output voltage waveform is shown in Fig. 11. The THD on the output waveforms is observed to be 26.83%.

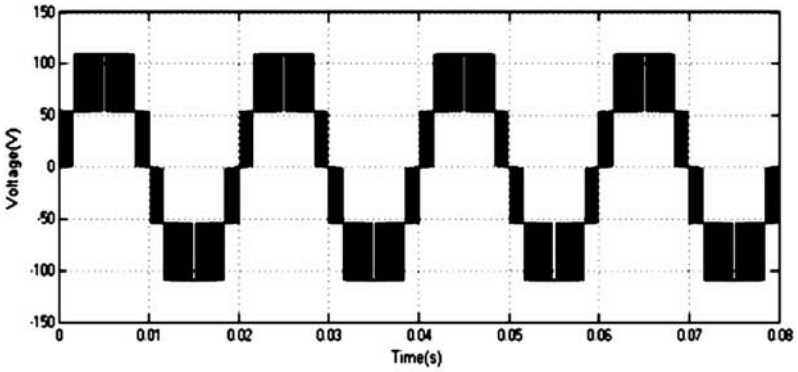

Fig. 9. Output voltage of the five level NPC inverter.

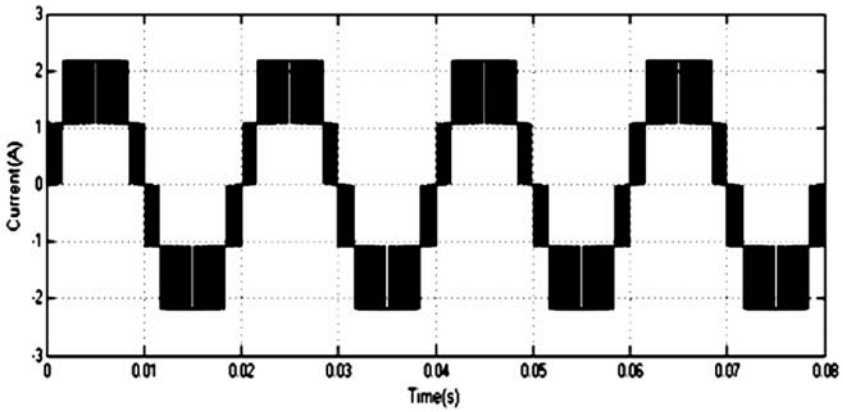

Fig. 10. Output current of the five level NPC inverter.

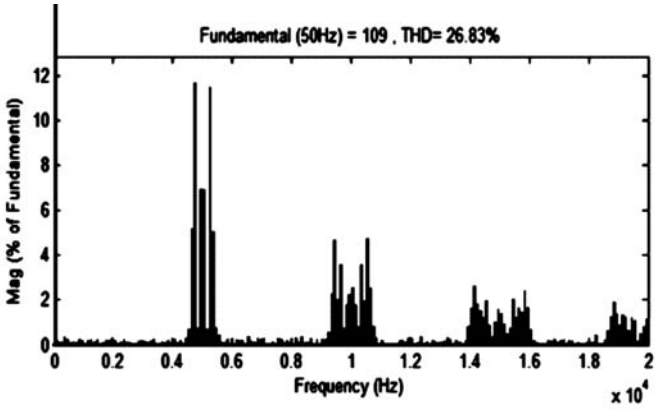

Fig. 11. Harmonic spectrum of the five level NPC inverter.

Table 4. THD content on three level and five level NPC inverter

Inverter	*THD*
Three-level NPC	77.17%
Five-level NPC	26.83%

Table 4 shows the THD on the output waveforms of the three level and five level inverter. It can be seen that the five level inverter produces lesser THD on the output waveforms compared to the three level inverter.

(*c*) Five level NPC inverter with LCR filter

The parameters used for the filter simulation is shown in Table 5. The parameters are designed as per the steps mentioned in Section 4.

Table 5. Filter system parameters.

Parameter	*Value*
Filter Inductance Value	8 mH
Filter Capacitance value	5 μF
Filter Damping Resistance	50 Ω
Cut-off Frequency	800 Hz

The output waveforms of the NPC inverter with the LCR filter are shown in Fig. 12 and Fig. 13 respectively. It can be observed that the output waveforms have become more towards sinusoidal. The harmonic spectrum for the output voltagewaveform is shown in Fig. 14. The THD on the output waveforms is observed to be 2.87% with the designed filter.

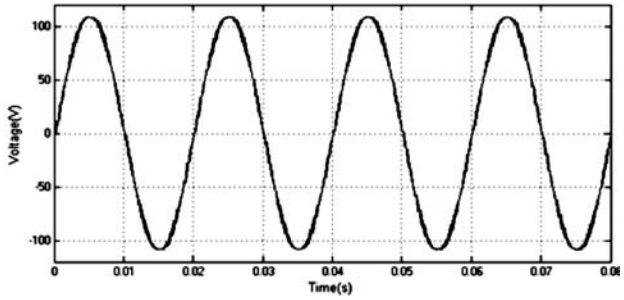

Fig. 12. Output voltage of NPC inverter with LCR filter.

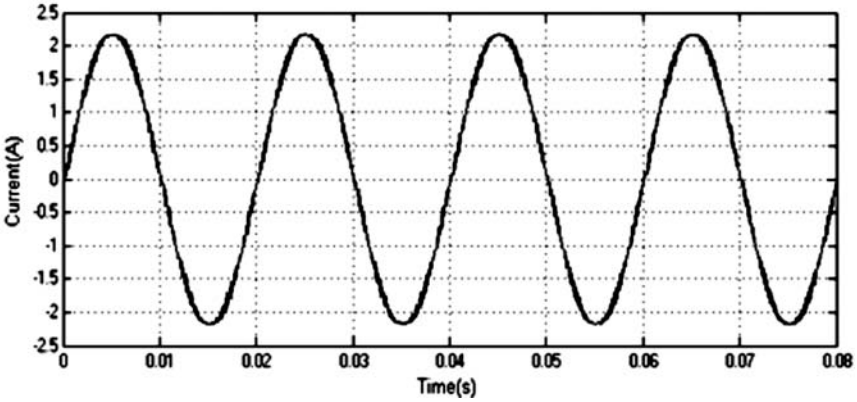

Fig. 13. Output current of NPC inverter with LCR filter.

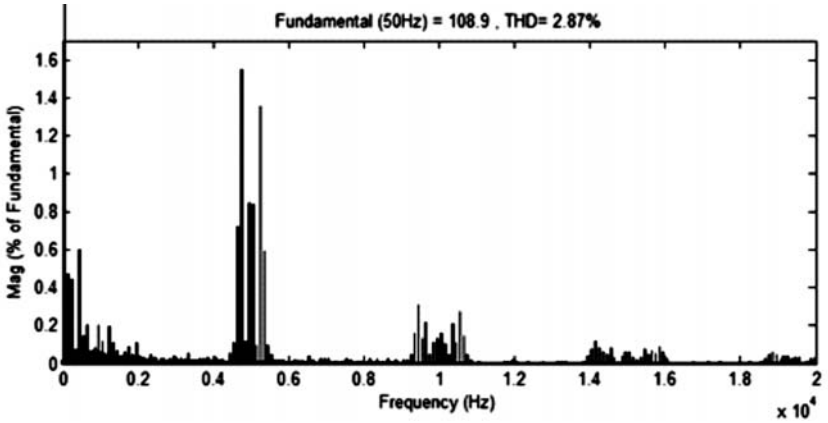

Fig. 14. Harmonic spectrum of NPC inverter with LCR filter

The performance of the filter is analyzed with different values of cut off frequencies and inductor values. Table 6 shows the THD obtained for cut off frequencies of 800 Hz, 1200 Hz and 1500 Hz for inductor impedances of 5%, 4% and 3%. It can be seen that with increase in the cut off frequency, for a particular inductor value, the THD content on the output waveforms decrease. Also, with increase in the impedance of the filter inductor, the THD decreases for a particular cut off frequency. Thus the parameters of the filter circuit needs careful design procedure in order to obtain better quality waveforms with reduced harmonic distortion.

Table 6. THD values for different inductor values and cut off frequencies

L_f impedance in % of load impedance	***Cut off frequency(Hz)***		
	800	***1200***	***1500***
5%	2.49%	2.87%	3.09%
4%	2.71%	3.22%	3.52%
3%	2.99%	3.69%	4.11%

6. CONCLUSION

The analysis of a three level and five level NPC inverter is carried out in this work. Multicarrier PDPWM technique is employed to generate gating pulses the inverter switches. The output waveforms and harmonic spectrum are captured for the two inverters and a comparison of THD on the output waveforms is done. In order to reduce the harmonic content on the output of the multilevel inverter, a passive LC filter is designed. For different filter parameter and cut off frequency values, the performance of the filter is analyzed. It is found that with the designed filter, the output THD on the five level NPC inverter waveforms is reduced to 2.87% which is well within the IEEE standards.

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