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DC-AC Hybrid Cascaded Nine Level Converter for Battery Management Applied in Electric Vehicles

N. Kalaiarasi[1], Ravi Varma[2], S. Paramasivam[3] and S.S. Dash[4]

ABSTRACT

In this paper, each battery cell can be controlled to be connected into the circuit or to be bypassed by a half-bridge converter. All half- bridges are cascaded to output a staircase shape DC voltage. Then, the H-bridge converter is used to change the direction of the DC bus voltages to make up AC voltages. The outputs of the converter are multilevel voltages with less harmonics and lower dv/dt, which is helpful to improve the performance of the motor drives. By separate control according to the SOC (state-of-charge) of each cell, the energy utilization ratio of the batteries can be improved. The imbalance of terminal voltage and SOC can also be avoided, fault-tolerant can be easily realized by modular cascaded circuit, so the life of the battery stack will be extended. MATLAB simulation is done to verify the performance of the proposed converter.

Keywords: Battery cell, Electric vehicle (EV), Hybrid cascaded multilevel converter, Voltage balance, State of charge (SOC).

1. INTRODUCTION

An energy storage system plays an important role in electric vehicles (EV). Batteries, such as lead-acid or lithium batteries, are the most popular units because of their appropriate energy density and cost. Since the voltages of these kinds of battery cells are relatively low, a large number of battery cells need to be connected in series to meet the voltage requirement of the motor drive [1],[2]. Due to the manufacturing variability, cell architecture and degradation with use, the characters such as volume and resistance will be different between these cascaded battery cells. In a traditional method, all the battery cells are directly connected in series and are charged or discharged by the same current, the terminal voltage and state-of-charge (SOC) will be different because of the electrochemical characteristic differences between the battery cells.

When one of the cells reaches its cut-off voltage the charge and discharge have to be stopped. Moreover, when any cell is fatally damaged, the whole battery stack cannot be used anymore. So the battery cell screening must be processed to reduce these differences, and voltage or SOC equalization circuit is often needed in practical applications to protect the battery cells from overcharging or overdischarging [3], [4].

Generally, the equalization circuit has a group of inductance and converters, which can realize energy transfer between battery cells. The energy in the cells with higher terminal voltage or SOC can be transferred to others to realize the voltage and SOC equalization. Since the voltage balance is realized by energy exchange between cells, the energy utilization ratio is improved. The disadvantage is that a lot of components are required in these topologies, and the control of the converters is also complex [5]-[13].

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Multilevel converters are widely used in medium or high voltage motor drives [14]-[19]. The battery cells can be cascaded in series combining with the converters instead of connection in series directly. In [20], the cascaded H-bridge converters are used for the voltage balance of the battery cells. Each H-bridge cell is used to control one battery cell; then the voltage balance can be realized by the separate control of charging and discharging. The output voltage of the converter is multilevel which is suitable for the motor drives.

The cascaded topology has better fault tolerant ability by its modular design, and has no limitation on the number of cascaded cells, so it is very suitable to produce a higher voltage output using these low-voltage battery cells, especially for the application in power grid. Compared to the traditional voltage balance circuit, the multilevel converters are very suitable for the balance of battery cells. Because of the power density limitation of batteries, some ultracapacitors are used to improve the power density. Multilevel converters with battery cells are also very convenient for the combination of battery and ultracapacitors.

A hybrid cascaded nine level converter is proposed in this paper which can realize the terminal voltage or SOC balance between the battery cells. The converter can also realize the charge and discharge control of the battery cells. A desired AC voltage can be output at the H-bridge sides to drive the electric motor, or to connect to the power grid. So additional battery chargers or motor drive inverters are not necessary any more under this situation.

The AC output of the converter is multilevel voltage, while the number of voltage levels is proportional to the number of cascaded battery cells. So in the applications of EV, the output AC voltage is approximately ideal sine waves. The harmonics and dv/dt can be greatly reduced than the traditional two-level converters. Simulation is done to verify the performance of the proposed hybrid cascaded multilevel converter in this paper.

The introduction of the paper is explained in section I. Then the proposed system is explained in section II. It is then followed by the loss analysis and comparison in section III. Then the simulink results are explained in section IV and the conclusion in section V.

2. PROPOSED SYSTEM

The principal function of the inverters is to generate an AC voltage from a DC source voltage. If the DC voltage is composed by many small voltage sources connected in series, it becomes possible to generate an output voltage with several steps. Multilevel inverters include an arrangement of semiconductors and DC voltage sources required to generate a staircase output voltage waveform. Fig.1 shows the schematic diagram of voltage source-inverters with a different number of levels.

It is well known that a two level inverter, such as the one shown in Fig.1(a), generates an output voltage with two different values (levels), V_C and "zero," with respect to the negative terminal of the dc source

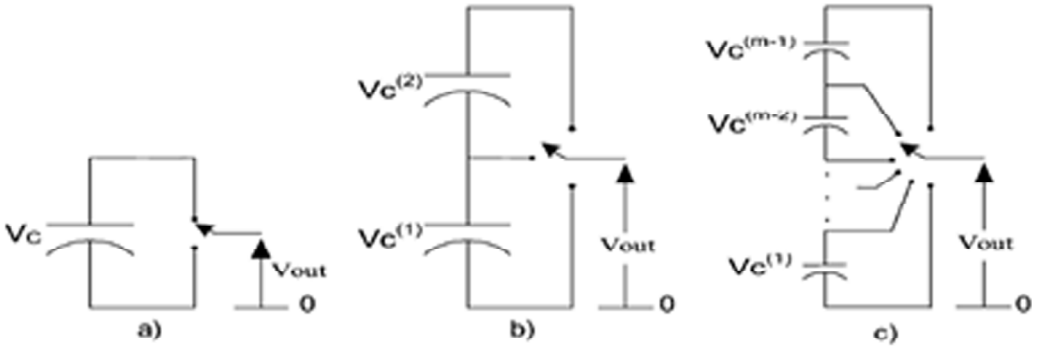

Figure 1: Basic Multilevel Inverters (a) Two levels, (b) Three levels, and (c) m Levels.

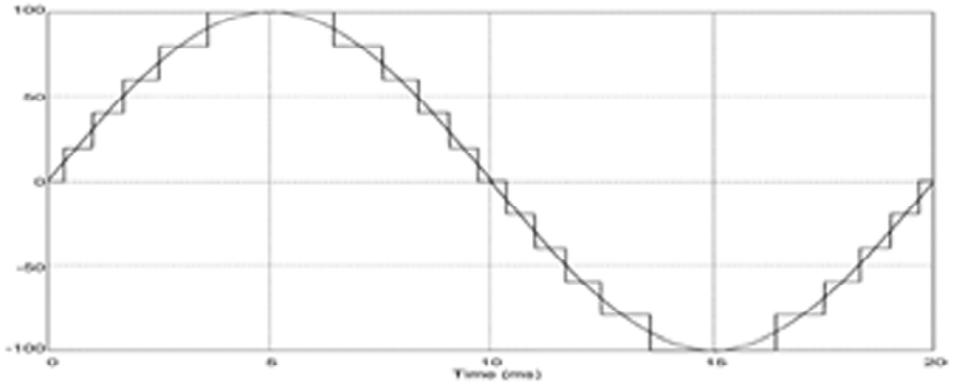

Figure 2: Voltage Waveform of an 11-Level Inverter.

("0"), while a three-level module, Fig. 1 (b) generates three different voltages at the output ($2V_C$, V_C, and "zero"). The different positions of the ideal switches are implemented with a number of semiconductors that are in direct relation with the output voltage number of levels. Multilevel inverters are implemented with small DC sources to form a staircase AC waveform, which follows a given reference template. For example, having ten DC sources with magnitudes equal to 20 V each, a composed 11-level waveform can be obtained (five positive, five negatives, and zero with respect to the middle point between the ten sources), generating a sinusoidal waveform with 100-V amplitude as shown in Fig.2.

It can be observed that the larger the number of the inverter DC supplies, the greater the number of steps that can be generated, obtaining smaller harmonic distortion. However, the number of DC sources is directly related to the number of levels through the equation n= m-1, Where 'n' is the number of DC supplies connected in series and 'm' is the number of the output voltage levels. In order to get a 51-level inverter output voltage, 50-V supplies would be required, which is too much for a simple topology.

Besides the problem of having to use too many power supplies to get a multilevel inverter, there is a second problem which is also important, the number of power semiconductors required to implement the commutation circuit. Technical literature has proposed two converter topologies for the implementation of the power commutation, using force-commutated devices [transistors or gate turnoff Thyristors (GTOs)].

Compared with the diode-clamped and flying-capacitors inverter, Cascaded inverter requires least number of components i.e. the cascaded inverter does not require any voltage-clamping diodes or voltage balancing capacitors to achieve the same number of voltage levels. Soft switching technique can be used to reduce switching losses and device stresses.

From the above discussion an optimized circuit layout and packaging are possible with cascaded topology because each level has the same structure and there are no extra clamping diodes or voltage balancing capacitors.

2.1. Topology Of The Hybrid Cascaded Multilevel Converter

The hybrid-cascaded multilevel converter proposed in this paper is shown in Fig. 3, it has a cascaded half-bridges with battery cells on the left and an H- bridge inverters on the right. The output of the cascaded half-bridges is the DC bus which is connected to the DC input of the H-bridge. The half-bridge at the left makes the battery cell to be involved into the voltage producing or to be bypassed.

Therefore, by control of the cascaded half-bridges, the number of battery cells connected in the circuit will be changed, that leads to a variable voltage to be produced at the DC bus. The H-bridge is just used to alternate the direction of the DC voltage to produce AC waveforms. Hence, the switching frequency of devices in the H-bridge equals to the base frequency of the desired AC voltage.

The low voltage devices are used in the cascaded half-bridges which works in higher switching frequency to reduce harmonics, such as MOSFETs with low on resistance. The higher voltage devices are used in the H-bridges which works just in base frequency. So the high voltage large capacity devices such as GTO or IGCT can be used in the H-bridges.

The three-phase converter topology is shown in Fig. 4. If the number of battery cells in each phase is n, then the devices used in one phase cascaded half-bridges is 2*n. Compared to the traditional equalization circuit the number of devices used is comparatively less.

Since all the half-bridges can be controlled individually, a staircase shape half-sinusoidal-wave voltage can be produced on the DC bus and it is given to the input of the H-bridge. So, a multilevel AC voltage can be formed at the output side of the H-bridge, the number of AC voltage levels is 2"n+1 where n is the number of cascaded half-bridges in each phase. On the other hand, the more of the cascaded cells, the more voltage levels at the output side, and the output voltage is closer to the ideal sinusoidal. So it is a suitable topology for the energy storage system in electric vehicles.

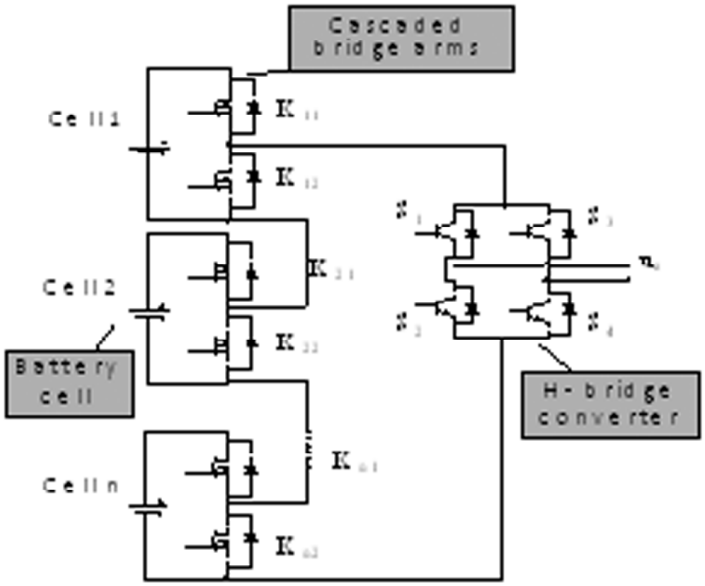

Figure 3: Hybrid cascaded multilevel converter.

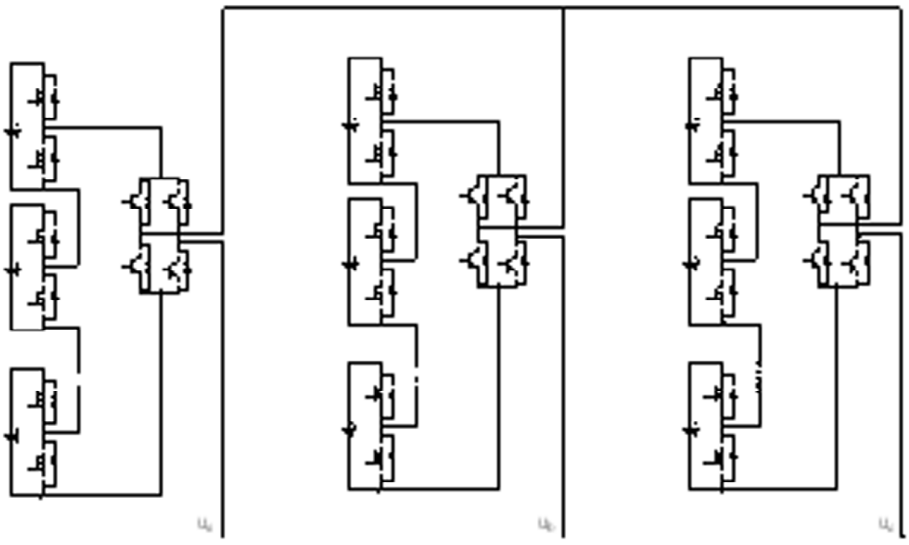

Figure 4: Three-phase hybrid cascaded multilevel converter.

2.2. Control Method of The Converter

The switching state of the cascaded half-bridge converter is as follows:

Sx = 1 Upper switch is conducted, lower switch is OFF

Sx = 0 Lower switch is conducted, upper switch is OFF.

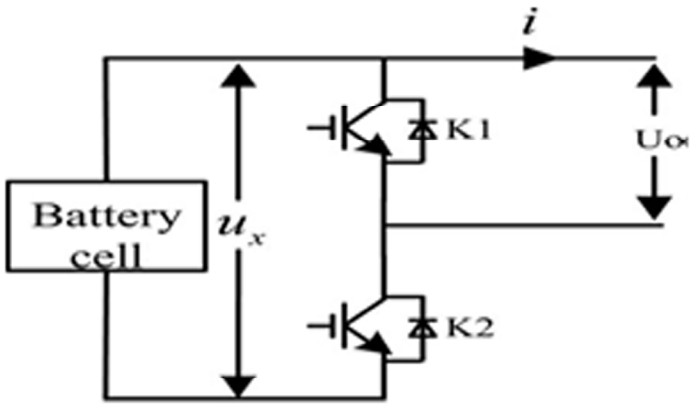

Figure 5: Single half-bridge circuit

The modulation ratio mx of each half bridge is defined as the average value of the switching state in a PWM period. In the relative half-bridge converter shown in Fig. 5, when $S_x = 1$, the battery is connected in the circuit and is discharged or charged which is found by the direction of the external current. When $S_x = 0$, the battery cell is bypassed from the circuit, the battery is neither discharged nor charged. When $0 < mx < 1$, the half-bridge works in a switching state. The instantaneous discharging power from this cell is

$$P = S_X . u_X . i \quad (1)$$

Here u_x is the battery cell voltage and i is the charging current on the DC bus. In the proposed converter, the H-bridge is just used to alternate the direction of the DC bus voltage, so the reference voltage of the DC bus is the absolute value of the ac reference voltage, just like a half-sinusoidal-wave at a steady state. It means that all the battery cells need not supply the load at the same time. As the output current is the same for all cells connected in the circuit, the charged or discharged energy of each cell is determined by the period of this cell connected into the circuit, which can be used for the voltage or energy equalization. The cell with higher voltage or SOC can be discharged more or to be charged less. For the cascaded multilevel converters, generally there are two kinds modulation method: phase-shift PWM and carrier cascaded PWM.

As the terminal voltage or SOC balance control must be realized by the PWM, so the carrier-cascaded PWM is suitable as the modulation ratio difference between different cells can be used for the balance control. In the carrier-cascaded PWM, only one half-bridge converter in each phase is allowed to work in switching state, the others keep their state unchangeable with $S_x = 1$ or $S_x = 0$, so the switching loss can be reduced. When the converter is used to feed a load, the battery with higher terminal voltage or SOC is preferentially used to form the DC bus voltage with $S_x = 1$. The battery with lower terminal voltage or SOC will be controlled in switch state with $0 < mx < 1$ or be bypassed with $S_x = 0$. The modified carrier-cascaded PWM method realize the control of the converter and voltage equalization.

The terminal voltages of the battery cells determines its position in the carrier wave. In the discharging process, the bottom layer of the carrier wave has the battery cells with higher voltage while the cells with lower voltage at the top layer. Then, the cells at the top layer will be used less and less energy is consumed from these cells. In the proposed PWM method, the carrier arranged by terminal voltage can realize the

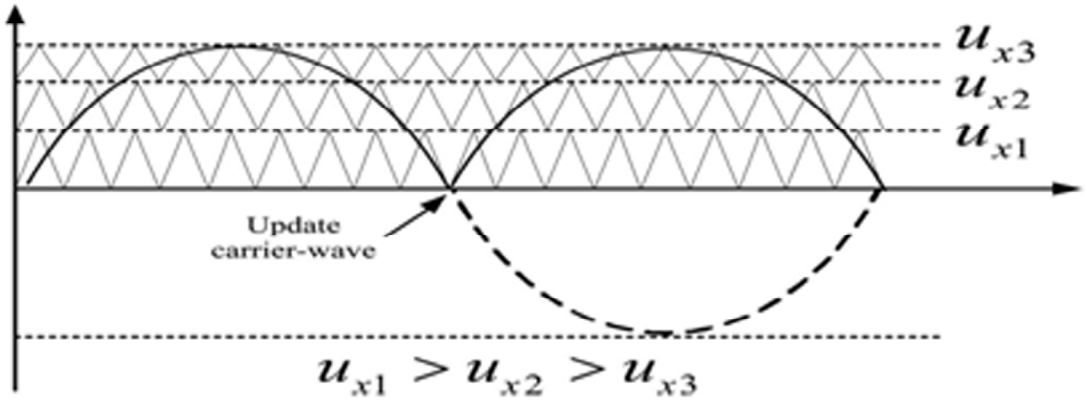

Figure 6: Carrier wave during discharging.

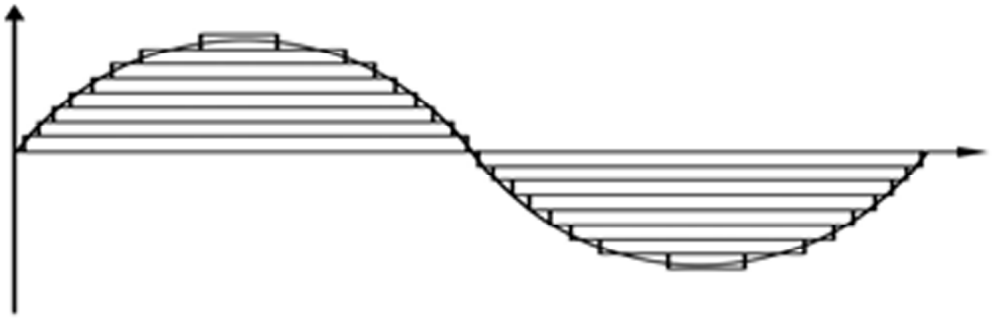

Figure 7: Base frequency modulation

terminal voltage balance, while the carrier arranged by SOC can realize the SOC balance. Since the SOC is difficult to be estimated in the batteries in practice, the terminal voltage balance is usually used. Normally, the cut-off voltage during charge and discharge will not change inspite of the variation of manufacturing variability, cell architecture, and degradation with use. So the overcharge and over discharge can also be eliminated even the terminal voltages are used instead of the SOC for the carrier-wave arrangement. To reduce the dv/dt and EMI, only one half-bridge is allowed to change its switching state at the same time for the continuous reference voltage. Therefore, the carrier wave is only rearranged when the modulation wave is zero and the rearranged carrier only becomes effective when the carrier wave is zero. So the carrier wave is only rearranged at most twice during one reference AC voltage cycle as shown in Fig. 6.

The battery's terminal voltage and SOC change very slowly during the normal use, so the carrier wave updated by base frequency is enough for the voltage and SOC balance. If the number of the cascaded cells is large enough, all the half-bridges can just work in switch-on or switch-off state to form the staircase shape voltage. So the switching frequency of all the half-bridges can only be base frequency as shown in Fig. 7, where the output AC voltage is still very approach to the ideal sinusoidal wave which is similar with the multilevel converter. The half-bridge can be bypassed, when one cell is damaged and there is no influence on the other cells. The output voltage of the phase with bypassed cell will be reduced. For symmetry, the three-phase reference voltage must be reduced to fit the output voltage ability. To improve the output voltage, the neutral shift three-phase PWM can be adopted. The bypass method and the neutral shift PWM is very similar with the method explained in [20].

3. LOSS ANALYSIS AND COMPARISON

The loss analysis and comparison are done theoriticaly. In the traditional circuit the three-phase two-level inverter is used for the discharging control and the energy transfer circuit is used for the voltage balance. In the proposed hybrid-cascaded circuit, the cascaded half-bridges are used for voltage balance control and

also the discharging control associated with the H-bridge converters. The switching loss and the conduction losses in these two circuits are quite different. To do a clear comparison, the switching and conduction loss is analyzed. In the hybrid-cascaded converter, the energy loss is composed of several parts

$$J_{Loss} = J_{s:\_B} + J_{s\_H} + J_{c\_B} + J_{c\_H} \quad (2)$$

Here, J_{s_B} and J_{s_H} are the switching losses of the cascaded half-bridges and the H-bridge converters, while J_{c_H} and J_{c_B} are the conduction losses. In the traditional circuit the energy loss is composed by

$$J_{Loss} = J_{s\_I} + J_{s\_T} + J_{c\_I} + J_{c\_T} \quad (3)$$

where J_{s_I} and J_{s_T} are the switching losses of the three-phase inverter and the energy transfer circuit for voltage balance. J_{c_I} and J_{c_T} are the conduction losses.

First, the switching loss is analyzed and compared under the requirement of same switching times in the output AC voltage. That means the equivalent switching frequency of the cascaded half-bridges in hybrid-cascaded converter is the same as the traditional inverter. The switching loss is determined by the voltage and current stress on the semiconductor devices, and also the switching time

$$J_s = \int_0^{T_{switch}} u \,.\, idt \quad (4)$$

In the proposed hybrid-cascaded converter, the H-bridge converter always switch when the DC bus voltage is zero. So the switching loss of the H-bridge is almost zero

$$J_{s\_H} \approx 0 \quad (5)$$

The equivalent switching frequency of the half-bridges is the same as the traditional converter, but only one half-bridge is active at the any instantaneous in each phase. The voltage step of each half-bridge is only the battery cell voltage which is much lower than the whole DC bus voltage. Furthermore, if the lower conduction voltage drop and faster turn-off device such as MOSFET is used in the proposed converter, the switching loss of the half-bridge will be much smaller

$$J_{s\_B} = J_{s\_I}/n \quad (6)$$

In the traditional circuit, the voltage balance circuit will still cause some switching loss determined by the voltage imbalance. So in the proposed new topology, the switching loss is much smaller compared to the traditional two-level inverter

The conduction loss is determined by the on-resistance of the switching devices and the current value. Whatever the switching state, one switch device in each half-bridge and two devices in H-bridge are connected in the circuit of each phase, so the conduction loss power can be calculated by

$$P_{c\_B} = I^2 R_{c\_B} \,.\, n \quad (7)$$

$$P_{c\_H} = I^2 R_{c\_H} . 2 \quad (8)$$

Here, I is the rms value of the output current, R_{c_B} is the on-resistance of the MOSFET in the half-bridge, R_{c_H} is the device on-resistance used in the H-bridge, and n is the number of the cascaded cells. In the traditional three-phase inverter, only one device is connected in the circuit of each phase, the conduction loss power in each phase is just

$$P_{c\_I} = I^2 R_{c\_I} \quad (9)$$

where R_{c_I} is the on-resistance of the devices used in the inverter. The on-loss on cascaded half-bridges can be reduced furthermore by reducing the number of the cascaded cells, while the on-loss of the H-bridges

Table 1
Loss Comparison

		Loss in a single switching course	*Conduction Loss Power*
Traditional circuit	*Energy transfer circuit*	Determined by imbalance	Determined by Imbalance
	3-phase inverter legs	$J_{s\_}I$	$P_{c\_}I = I^2R_{c\_}I$
Proposed circuit	Cascaded half-bridges	Much less than $J_{s\_}I/n$	$P_{c\_}B = I^2R_{c\_}B^{n}$
	H-bridges	Near zero	$P_{c\_}H = I^2R_{c\_}H^{2}$

cannot be reduced. From the above analysis, the switching loss of the proposed converter is much less than the traditional converter, although the on-loss is larger than the traditional converter. The compared results are shown in Table 1.

4. SIMULATION RESULTS

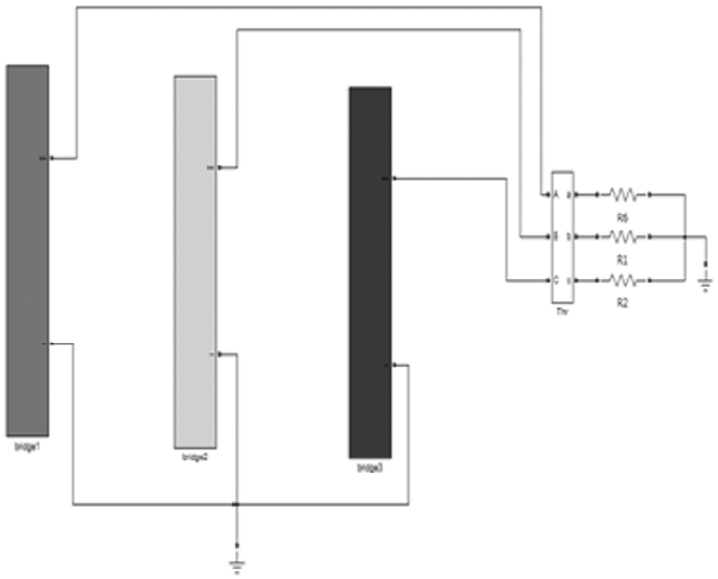

Figure 8: Simulink model of three phase nine level converter

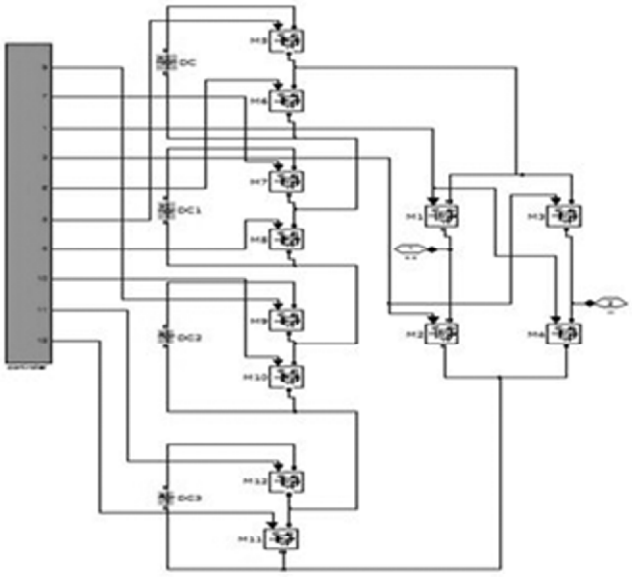

Figure 9: Simulink model of single phase nine level converter

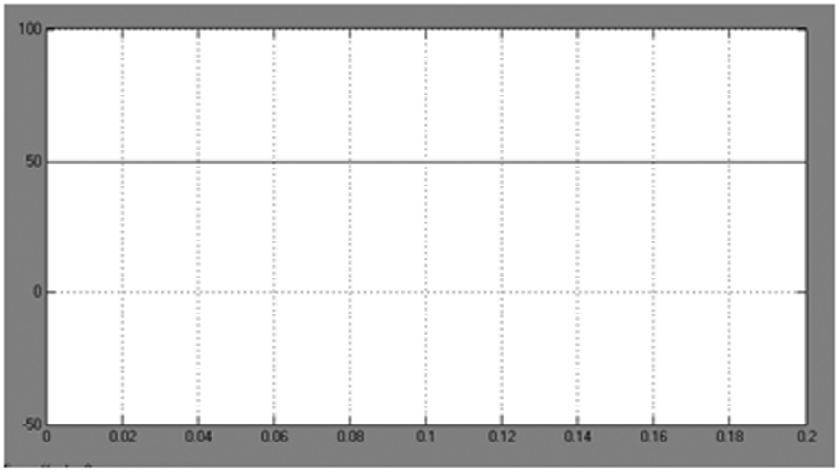

Figure 10: Input DC voltage

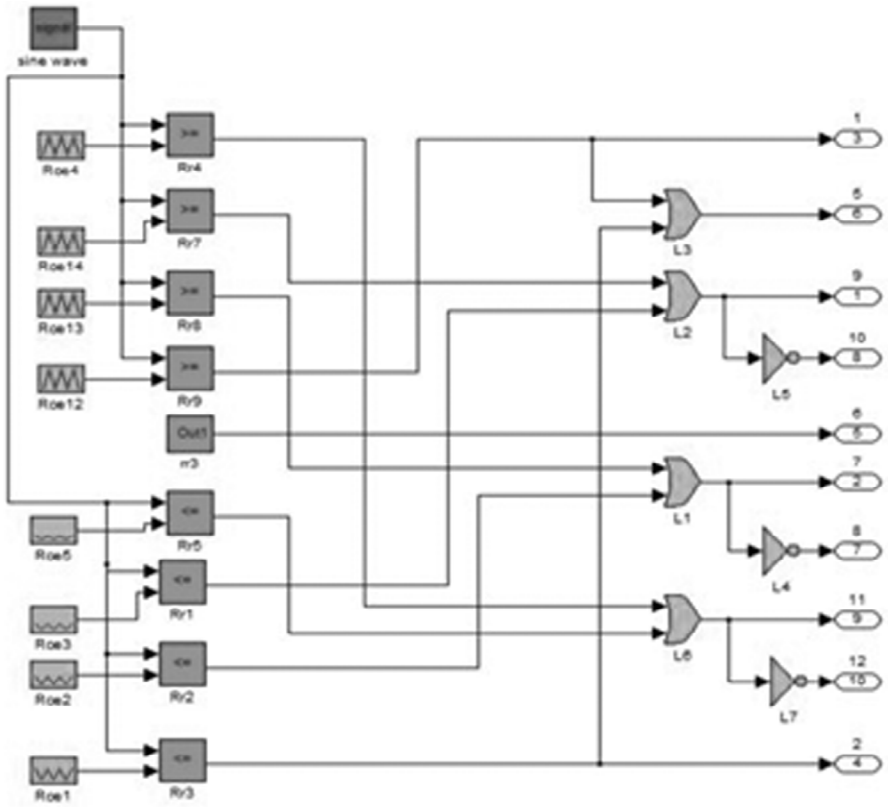

Figure 11: Firing circuit for nine level converter

Sine Wave Peak Amplitude (V)	*Reference Wave*	
	Time Values	*Output Values*
8.8	[0 .1e-3 .2e-3]	[7 9 7]
8.8	[0 .1e-3 .2e-3]	[5 7 5]
8.8	[0 .1e-3 .2e-3]	[3 5 3]
8.8	[0 .1e-3 .2e-3]	[1 3 1]
8.8	[0 .1e-3 .2e-3]	[-7 -9 -7]
8.8	[0 .1e-3 .2e-3]	[-5 -7 -5]
8.8	[0 .1e-3 .2e-3]	[-3 -5 -3]
8.8	[0 .1e-3 .2e-3]	[-1 -3 -1]

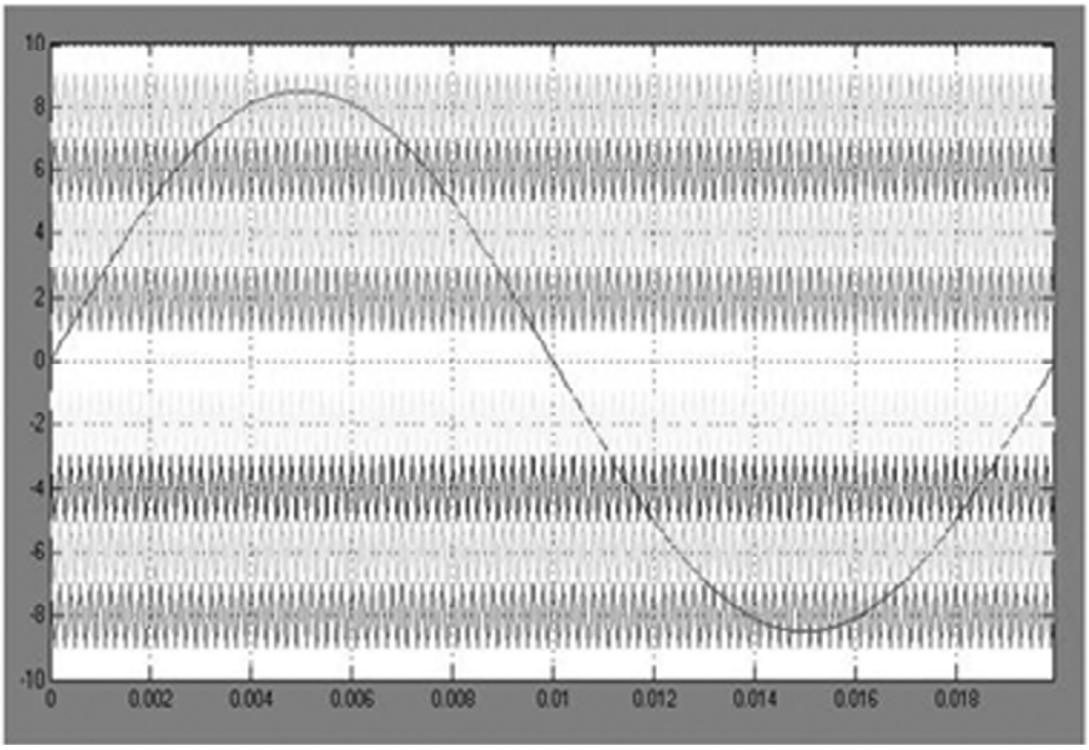

Figure 12: Pulse generation using carrier-cascaded PWM technique

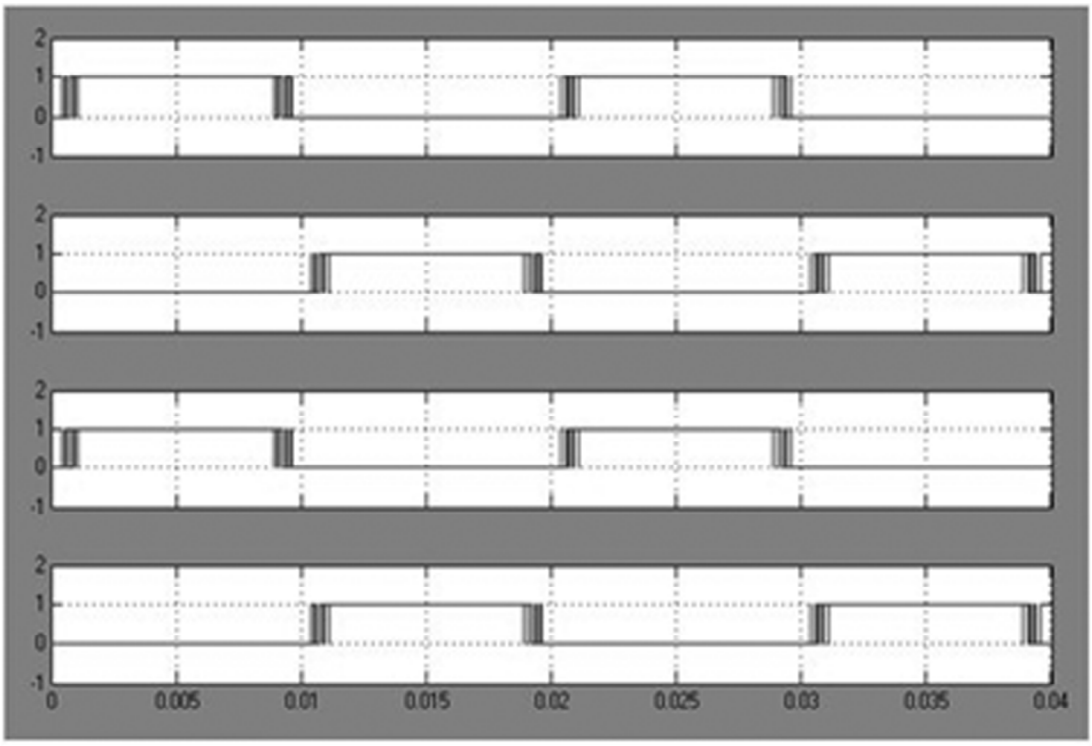

Figure 13: Simulink of driving pulse for H-bridge inverter

The above are output of the hybrid-cascaded multilevel converter proposed in this paper. The seven-level and nine-level MLI has been simulated using MATLAB. The Total Harmoic Distortion of hybrid-cascaded ninelevel converter with pulse width modulation technique is very low compared with seven level MLI. This results in low loss, reduces the harmonics and better voltage. The comparison of the parameters for seven-level and nine-level is shown in Table II.

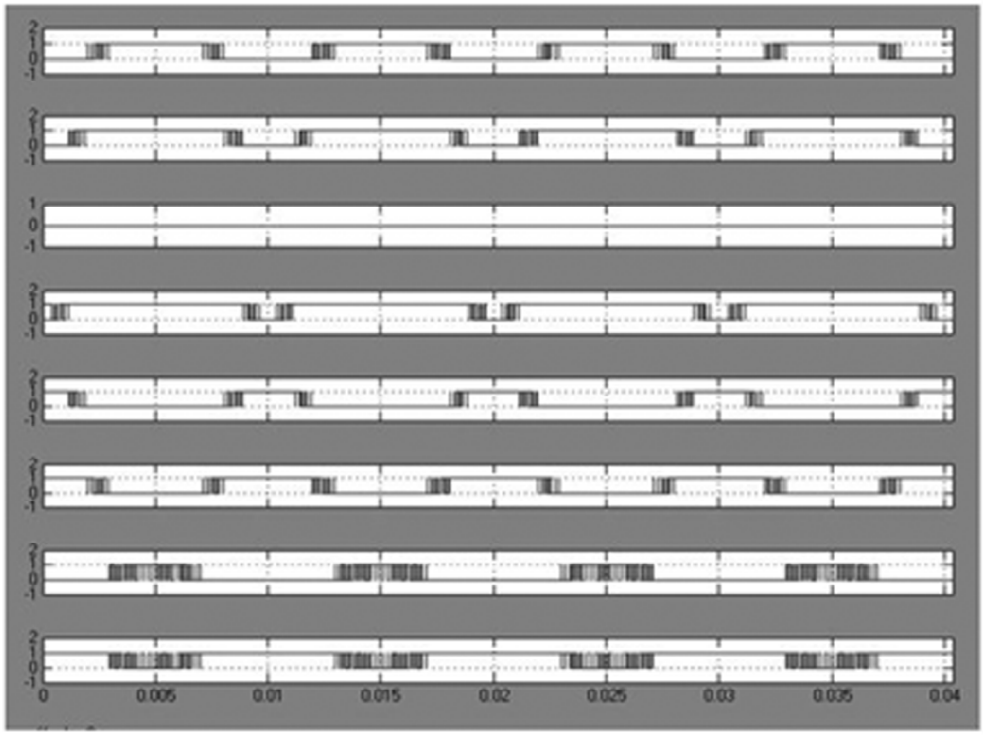

Figure 14: Simulink of driving pulse for level module switches

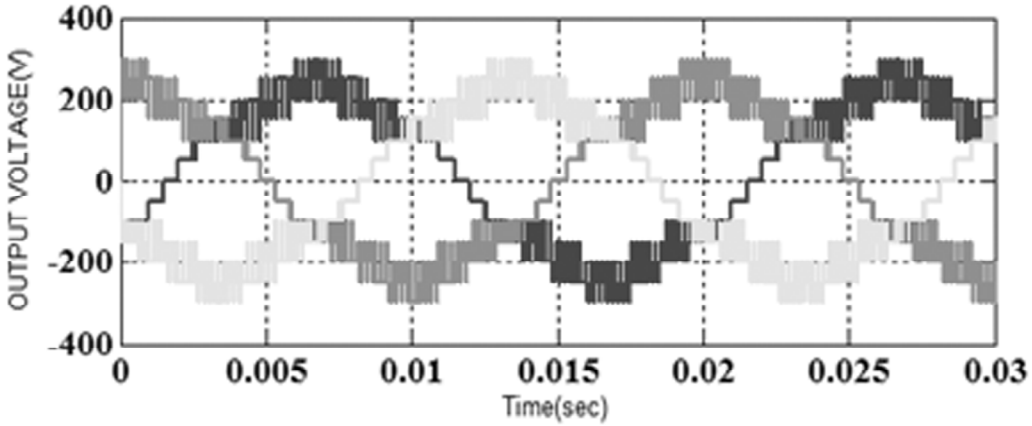

Figure 15: Output line voltage of seven level converter

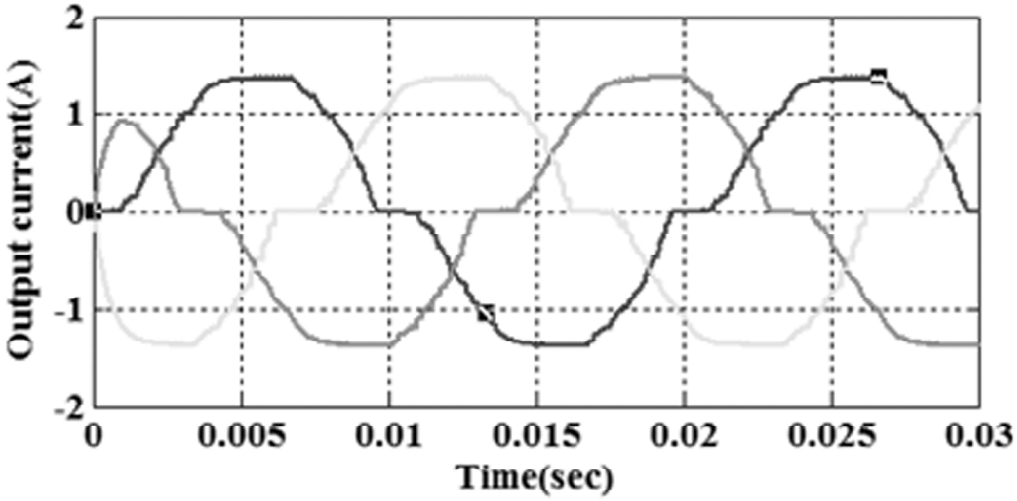

Figure 16: Output current of seven level converter

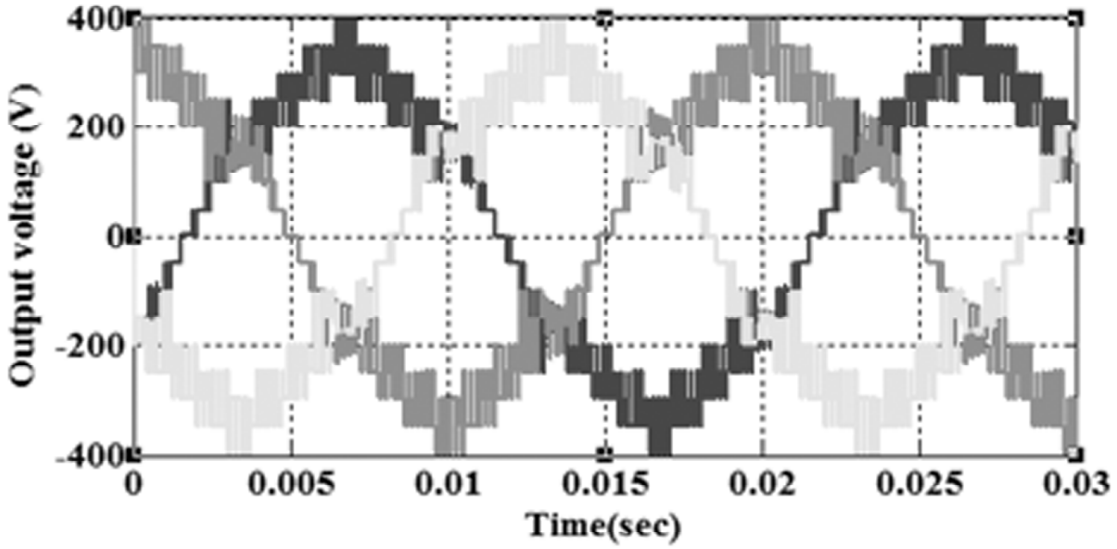

Figure 17: Output line voltage of nine level converter

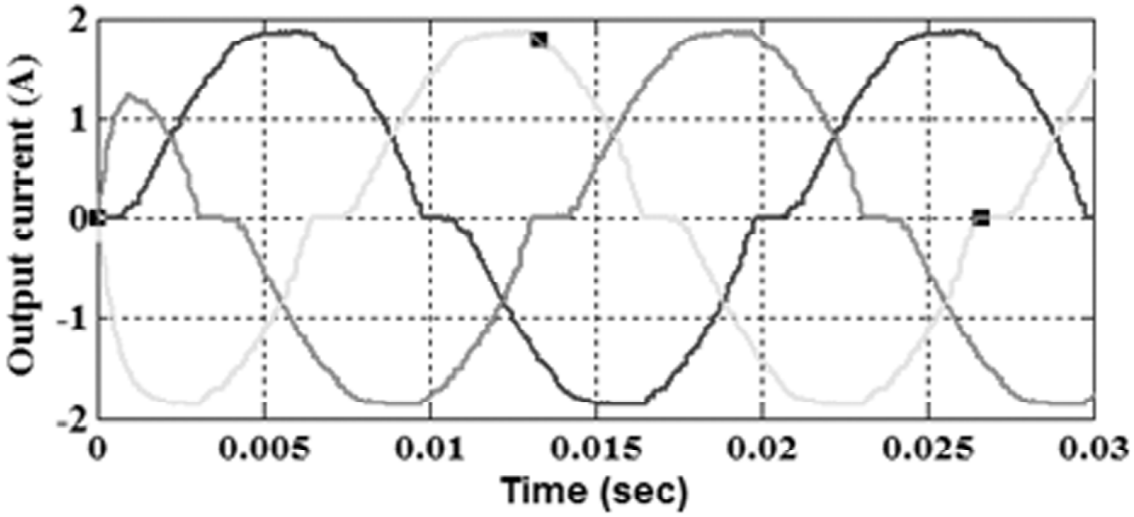

Figure 18: Output current of nine level converter

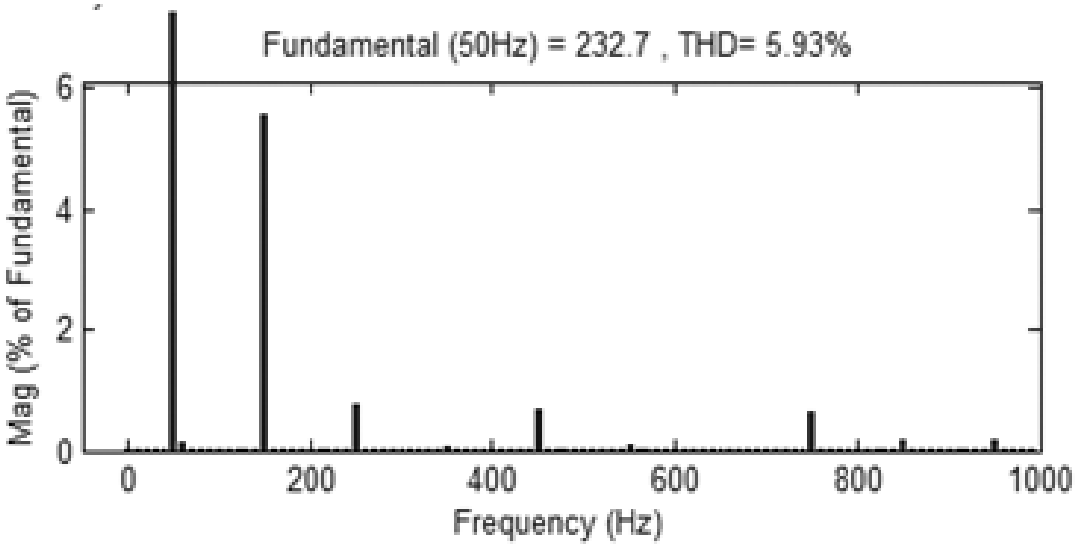

Figure 19: FFT Analysis for seven level converter output voltage

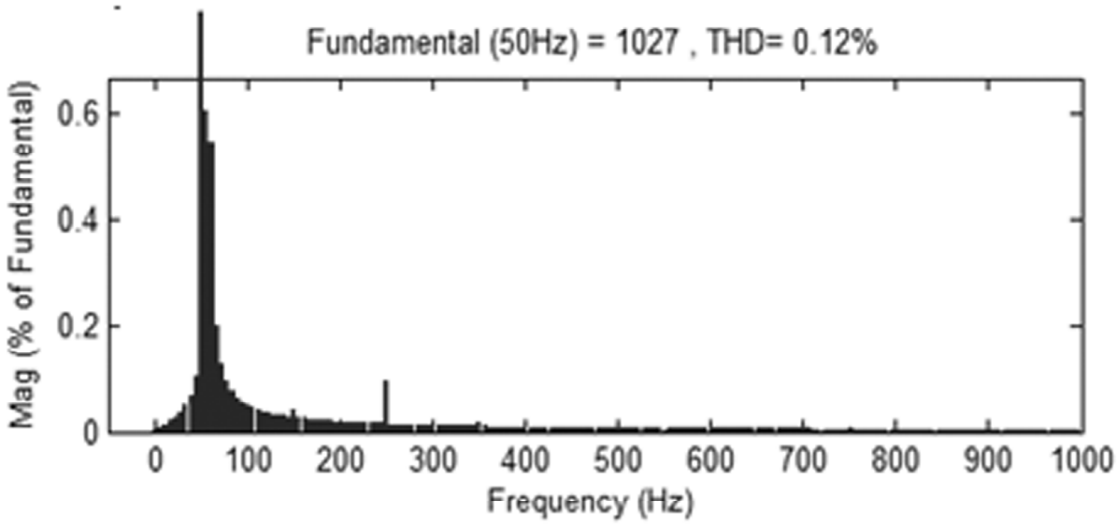

Figure 20: FFT Analysis for nine level converter output current

Table 2
Performance Comparison of Seven Level and Nine Level Converter

	Output voltage	*Output current*	*THD for O/P voltage*	*THD for O/P Voltage with filter*
Seven-level	300 V	1.4 A	26.64%	5.93 %
Nine-level	400 V	1.8 A	19.98%	0.12 %

5. CONCLUSION

The hybrid-cascaded nine level converter proposed in this paper can actualize the charging and discharging of the battery cells while the terminal voltage or SOC balance control can be realized at the same time. The proposed converter with modular structure can reach any number of cascaded levels and is suitable for the energy storage system control with low-voltage battery cells or battery modules. The fault module can be bypassed without affecting the running of the other ones, so the converter has a good fault-tolerant character which can significantly improve the system reliability. The PWM method with low switching loss for both discharging and charging control is proposed considering the balance control at the same time.

The output of the circuit is multilevel AC voltages where the number of levels is proportional to the number of battery cells. So the output AC voltage is nearly the ideal sinusoidal

wave which can improve the control performance of the motor control in EV's. The switching loss and the conduction losses of the proposed system is compared with the traditional system. The losses in the proposed system is lesser than the losses in the traditional system. The nine-level hybrid-cascaded multilevel converter improves output voltage, reduces output total harmonic distortion. These schemes are confirmed by MATLB simulation results.

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