

Performance comparison of Seven Level Inverter and Nine Level Inverter with minimum devices

K. Mohan Raj¹, C. Ashwin Parthasarathy², Subhransu Sekhar Dash³, M. Arun Noyal Doss⁴

ABSTRACT

This paper proposes to compare the performances of seven level inverter and nine level inverter. Multicarrier carrier PWM techniques such as phase disposition (PD), phase oppose disposition (POD), alternate phase oppose disposition (APOD) techniques are used. Simulation results are implemented in Matlab/Simulink environment to show the total harmonic distortion (THD) and third harmonic level of seven-level and nine-level inverter.

Keywords: Multilevel inverter, multicarrier PWM techniques

1. INTRODUCTION

As the fossil fuels are becoming expensive, solar energy is gaining more attention in the grid side. Small capacity grid connected systems employing solar energy is used in residential applications [1]-[2]. The power conversion is more important in the grid system where dc power from the solar cell is converted to ac power before feeding this power to grid. The power coming out from solar is very much less which gets boosted dc-dc converter before feeding it to inverter stage. [2]- [4].

The power conversion efficiency is more important to insure that there is no wastage of energy generated by solar cell array. [5]. The multilevel inverter integrates renewable energy resources with the grid. The purpose of integrating renewable energy to the grid is to provide active power by means of power electronic devices. The voltage change in multilevel inverter is used to improve the power conversion efficiency of inverter and also reduces the switching stress on the inverter [6]-[7].

An inverter and chopper circuit is implemented. This circuit uses carrier based pulse width modulation technique to generate capacitor voltages [8]. The back-to-back m-level diode clamped converter is modeled to balance the dc bus capacitors based on average power flow [9]. Multilevel converters use fast predictive digital control method to compute the optimal vector using three phase multilevel dynamic model equations [10].

A flying capacitor multicell converter is presented. It uses modified phase shifted pulse width modulation to maintain the self-balancing property of the flying capacitor converter [11]. A single leg five level flying capacitor converter implements modified phase shifted pulse width modulation to achieve faster voltage balancing in flying capacitor converter [12]. A flying capacitor converter uses space vector pulse width modulation to reduce the switching state of the flying capacitor converter and to carry out voltage balancing in the converter [13].

¹ SRM UNIVERSITY INDIA, Email: mohanraj@srmi.ac.in

² SRM UNIVERSITY INDIA, Email: ashwinpart@srmi.ac.in

³ SRM UNIVERSITY INDIA, Email: munu_dash_2k@yahoo.com

⁴ SRM UNIVERSITY INDIA, Email: arunoyal@srmi.ac.in

The active power control of individual multilevel converter cells is implemented in battery energy storage systems to charge and discharge battery at different power levels to obtain three phase balanced line to line voltage [14]. A new voltage balancing controller is proposed. A control algorithm is implemented in cascaded multilevel converters to balance the capacitor voltages and to eliminate the coupling effect between voltage balancing controller and controller without additional voltage balance controllers [15].

Multilevel inverters include diode clamped, flying capacitor, and cascaded H-bridge inverter types. Diode clamped and flying capacitor inverters can develop seven level voltages and nine level voltages. These two inverters are limited due to difficulty in regulation of their voltages and power circuits in both inverters are complicated. Asymmetric configuration of cascaded H-bridge multilevel inverter is used to generate higher level voltages, so cascaded H-bridge inverter is very popular in increasing voltage levels [16] - [17].

A single phase seven level grid connected inverter is used in photovoltaic systems. Three dc capacitors are used to generate three voltage levels resulting in voltage unbalancing [18]. A seven level inverter topology is introduced. The power electronic switches of level generation part are switched at high frequency [19]. A modular multilevel inverter is proposed. This inverter is similar to cascaded H-bridge type applied to the photovoltaic grid connected generator [20].

A multilevel dc-link inverter is presented. This inverter consists of several individual dc-blocks, with each dc-block comprised of solar cell, power electronic switch and a diode [21]. A novel transformer less grid connected photovoltaic system is implemented to reduce leakage current by connecting the negative terminal of the solar cell array directly to the ground [22]-[23]. Perturb and observe technique is introduced to track maximum power from the solar PV array depending on panel temperature and irradiance conditions [24]. The solar energy power processing system is operated with high efficiency and particularly high reliability to transfer electric power from PV panel to the grid [25]. The current controllers for single phase PV grid inverters are proposed. The nonlinear inductance is designed to track periodic signals or to compensate disturbances [26]-[27]. Different maximum power point tracking techniques is studied for photovoltaic systems [28]. A control strategy is introduced based on new discontinuous PWM method to balance the dc link voltage of neutral point clamped inverter [29].

A new simplified space vector PWM technique is implemented in three level inverters. It simplifies the space vector diagram of three-level inverter and has the same dc link voltage utilization [30]-[31]. A predictive control of a three phase neutral point inverter is proposed based on discrete time model system to predict future values of voltage and current of capacitors in the dc link [32]. The generalized multilevel inverter topology balances the voltage level by itself without depending on load characteristics [33].

An effective voltage balancing in diode clamped converters is used for power factor correction [34]. A new operational mode is studied in diode clamped inverter to avoid the voltage imbalance problem in dc link capacitors [35]. A new control strategy for cascaded multilevel converter is proposed along with new individual voltage balancing technique to solve the problems of dc voltage balance [36].

This paperproposes to compare the performances of seven level and nine level inverter integrated with dc-dc power converter. Here multicarrier carrier PWM techniques such as phase disposition (PD), phase oppose disposition (POD), alternate phase disposition (APOD) techniques are used to compare the performances of both inverters.

2. SEVEN LEVEL INVERTER FEDDC-DC CONVERTER

The block diagram of seven level inverter fed dc-dc converter, is shown in Figure 1. It comprises of a dc source, dc-dc converter, capacitor selection network, seven level inverter and load.

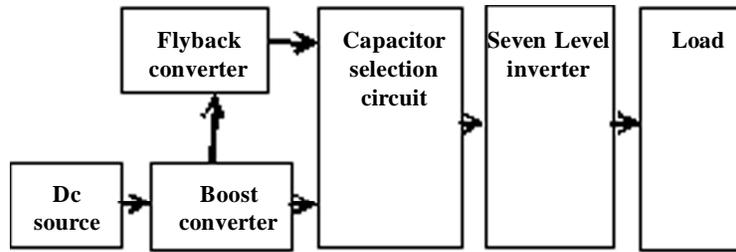


Figure 1: Block diagram of seven level inverter fed dc-dc converter.

The boost converter is a dc-dc converter used for boosting up the voltage from dc source. The boost converter is separated from fly back converter by means of isolation transformer. The seven-level inverter comprises of capacitor selection circuit and full bridge inverter circuit.

The boost converter is composed of an inductor L_D , a power electronic switch S_{d1} , and a diode, D_{d3} which charges capacitor $C2$ of seven level inverter. The flyback converter is composed of an inductor L_D , power electronic switches S_{D1} and S_{D2} , a transformer, and diodes D_{d1} and D_{d2} . The flyback converter charges capacitor $C1$ of the seven-level inverter. The circuit diagram for seven level inverter fed dc-dc power converter is shown in the Figure 2.

3. MODES OF OPERATION

Mode 1

In this mode switches S_{S1} and S_{S2} of the capacitor selection circuit are OFF. $C1$ is discharged through $D1$. The switches $S1$ and $S4$ conduct and the output voltage of the inverter is V_{DC} .

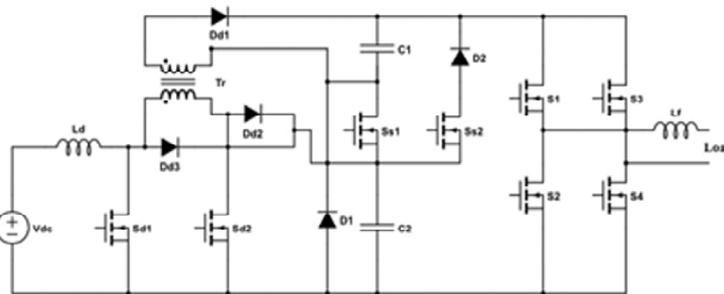


Figure 2: Configuration of seven level inverter fed dc-dc power converter.

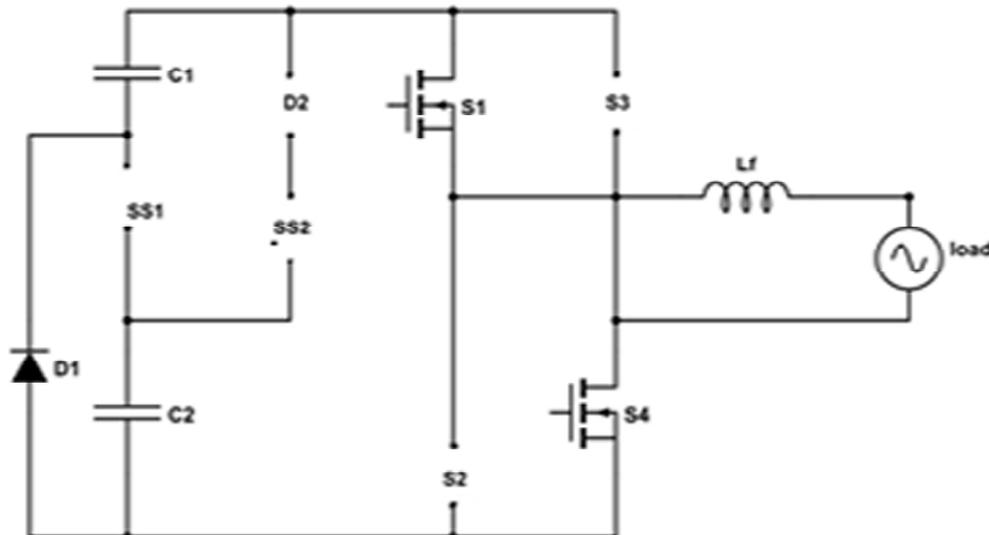


Figure 3: Mode 1 operation of seven level inverter.

Mode 2

In this mode switch S_{s2} is ON. C2 is discharged through S_{s2} and D2. The switches S1 and S4 conduct and the output voltage of the inverter is $2V_{DC}$.

Mode 3

During this mode, switches S_{s1} and S_{s2} are ON. Both C1 and C2 are discharged. The switches S1 and S4 conduct and output voltage of the inverter is $3V_{DC}$.

During negative half cycle switches S2 and S3 will conduct and produces $-V_{DC}$. The switches S_{s1} and S_{s2} of the capacitor selection circuit are operated at high frequency and because of these switches, voltages $-2V_{DC}$ and $-3V_{DC}$ are produced

4. NINE LEVEL INVERTER FEDDC-DC CONVERTER

The block diagram of nine level inverter fed dc-dc converter, is shown in the Figure 6. It comprises of dc-dc boost converter, nine level inverter and load.

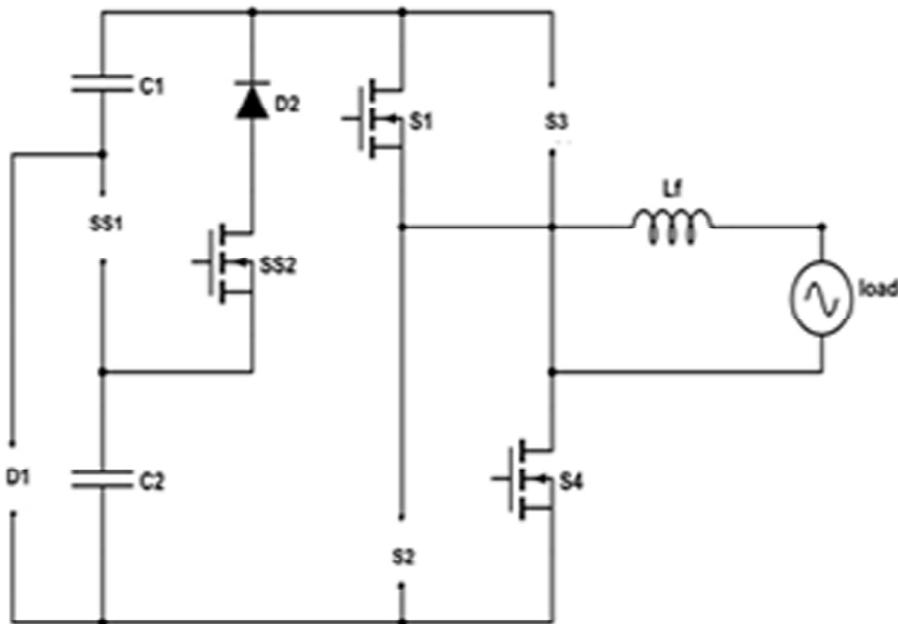


Figure 4: Mode 2 operation of seven level inverter.

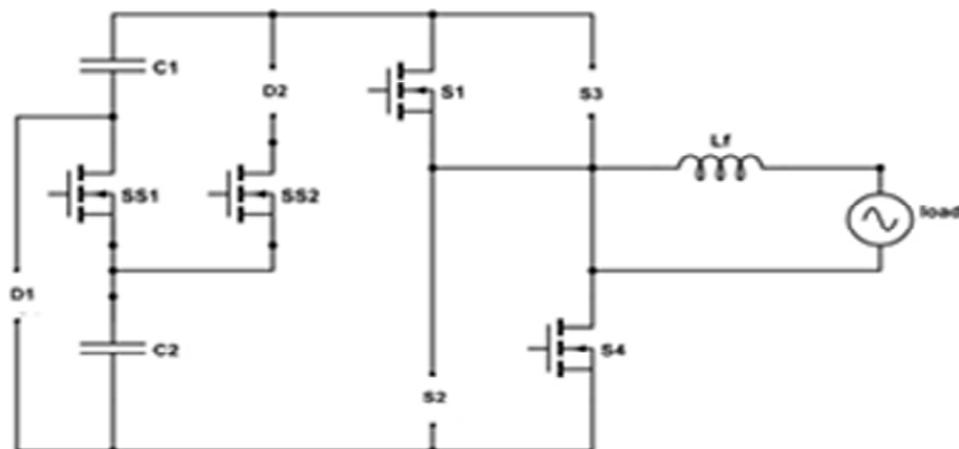


Figure 5: Mode 3 operation of seven level inverter.

The boost converter boosts up the voltage from dc source and feeds it to nine-level inverter where the nine-level inverter generates nine level voltages.

The circuit diagram of nine level inverter fed boost converter, is shown in the Figure 7. As seen in the figure boost converter is integrated with nine-level inverter. Boost converter consists of a switch, inductance and a diode. Asymmetrical configuration is used for nine level inverter to achieve 9 level output.

The nine-level inverter has one source and one flying capacitor. In the nine-level inverter during positive half cycle the switches S1, S4, S5, S8 will be conducting and during negative half cycle the switches S2, S3, S6, S7 will be conducting.

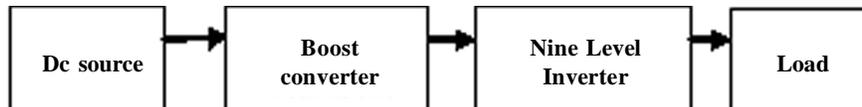


Figure 6: Block diagram of nine level inverter fed dc-dc converter

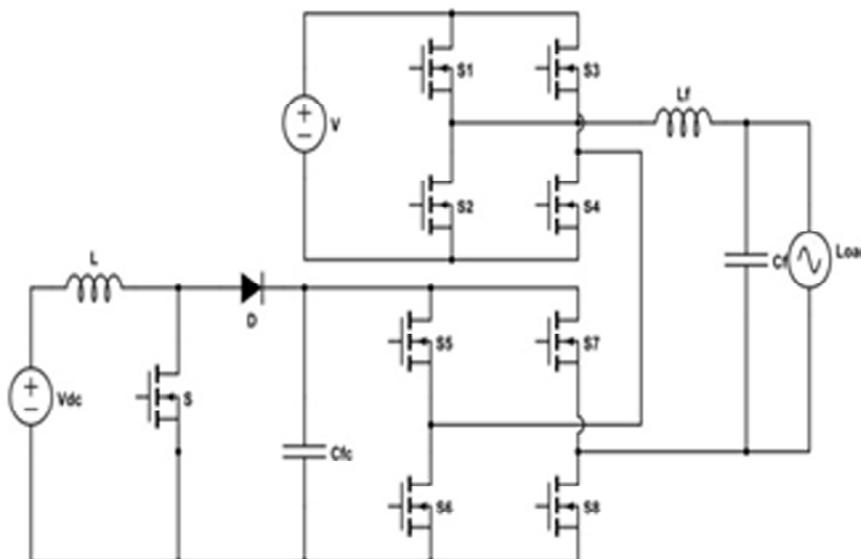


Figure 7: Configuration of nine level inverter fed dc-dc boost converter.

5. MODES OF OPERATION

Mode 1

The switches S2, S4, S5 and S8 conduct to give $1V_{dc}$. The lower half produces $1V_{dc}$ with the help of V_{s2} , while upper half acts as closed path. The voltage source V_{s1} is not utilized during mode 1.

Mode 2:

During mode 2, switches S1, S4, S6 and S7 conduct and voltage across V_{s1} is $3V_{DC}$ and voltage across V_{s2} is $1V_{DC}$. The difference between these two voltages is $2V_{DC}$.

Mode 3:

During mode 3, switches S1, S4, S5 and S7 conduct. V_{s2} is not utilized so the voltage from V_{s1} is $3V_{DC}$ which appears across load.

Mode 4:

During mode 4, switches S1, S4, S5 and S8 conduct. Both V_{s1} and V_{s2} sources are utilized to obtain $4V_{DC}$.

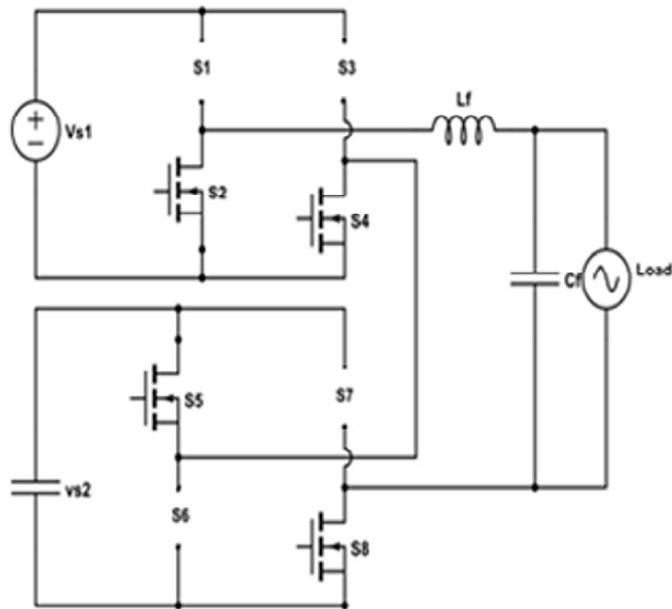


Figure 8: Mode 1 operation of nine level inverter.

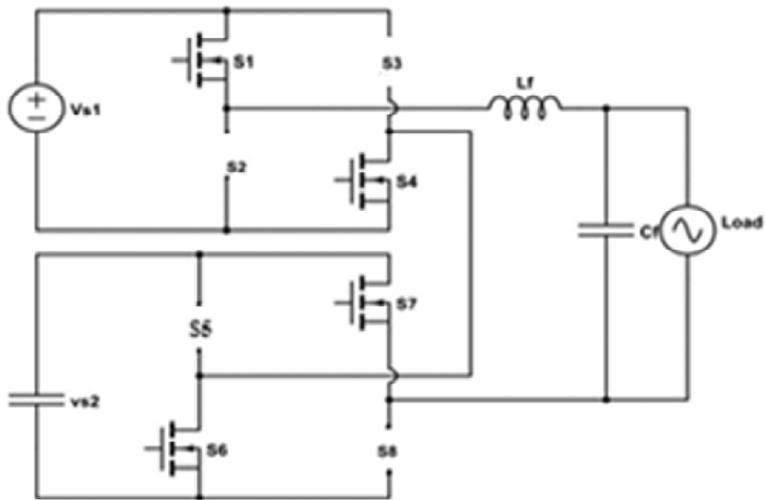


Figure 9: Mode 2 operation of nine level inverter.

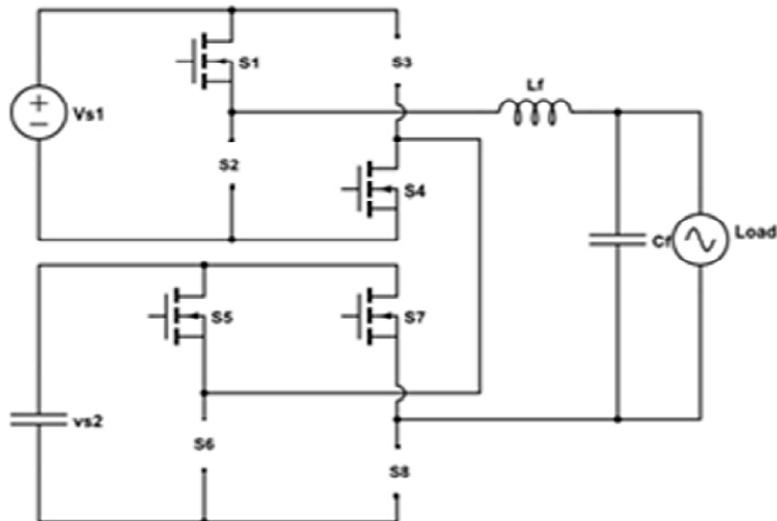


Figure 10: Mode 3 operation of nine level inverter.

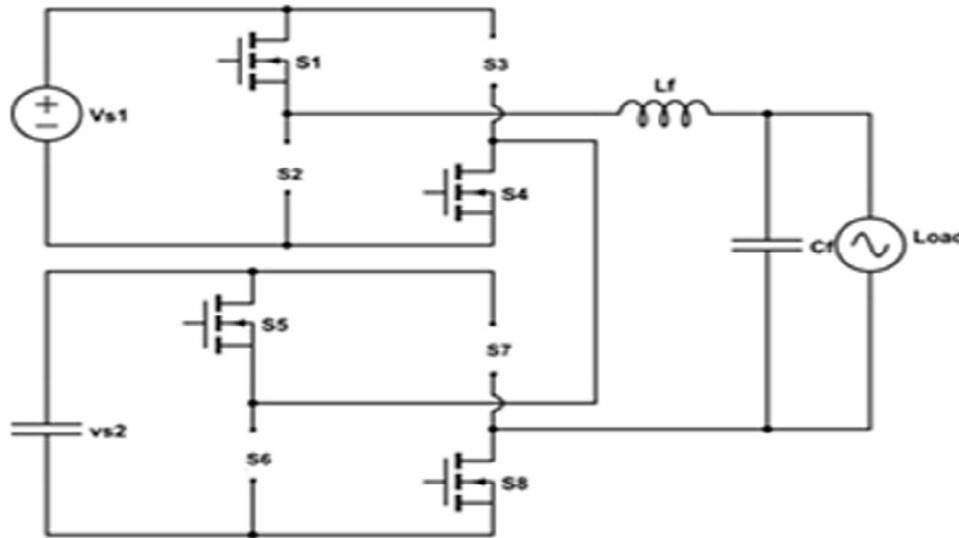


Figure 11: Mode 4 operation of nine level inverter.

6. PULSE WIDTH MODULATION TECHNIQUES

6.1. Phase Disposition (PD) Technique

The phase disposition technique as one of the carrier based PWM methods is based on the comparison of sinusoidal reference waveform with carrier signals in phase with each other.

6.2. Phase Opposition Disposition (POD) Technique

In the POD-PWM method the carrier signals above the zero axes are in phase. The carrier signals below zero are also in phase, but 180° phase shifted to the above carrier signals.

6.3. Alternate Phase Oppose Disposition Technique (APOD)

In case of alternate phase opposition disposition (APOD) modulation, every carrier waveform is out of phase with its neighbouring carrier waveform by 180°

7. SIMULATION RESULTS

The simulation circuit of seven-level inverter fed dc-dc converter is shown in the Figure 12.

In this circuit the multicarrier PWM techniques such as PD, POD, and APOD are implemented.

The carrier and reference signals for phase disposition technique, is shown in the Figure 13. It is seen that all carrier waves are in phase with each other and is compared with reference sinusoidal signal.

The carrier and reference waveforms for phase disposition technique is shown in the Figure 14. It is seen that carrier waves above the reference axis are in phase with each other. These waves are phase shifted by 180° to the carrier waves below the reference axis.

The carrier and reference waves generation for alternate phase oppose disposition is shown in the Figure 15. It is seen that each carrier wave is out of phase with neighbouring carrier wave.

The output voltage of dc-dc boost converter is shown in the Figure 16. Here output voltage obtained for boost converter is 100V and it is used for charging capacitor C2 of seven-level inverter.

The output voltage of flyback converter is shown in Figure 17. Here output voltage obtained is 50V and it is used for charging capacitor C1 of seven-level inverter.

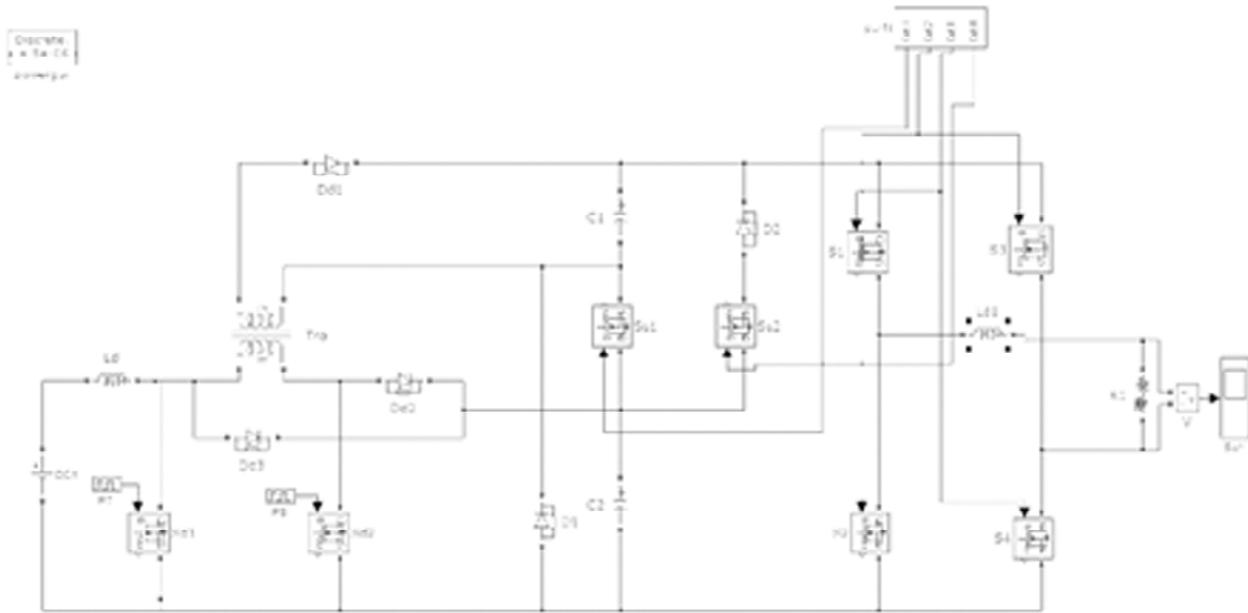


Figure 12: Simulation circuit of seven level inverter fed dc-dc converter

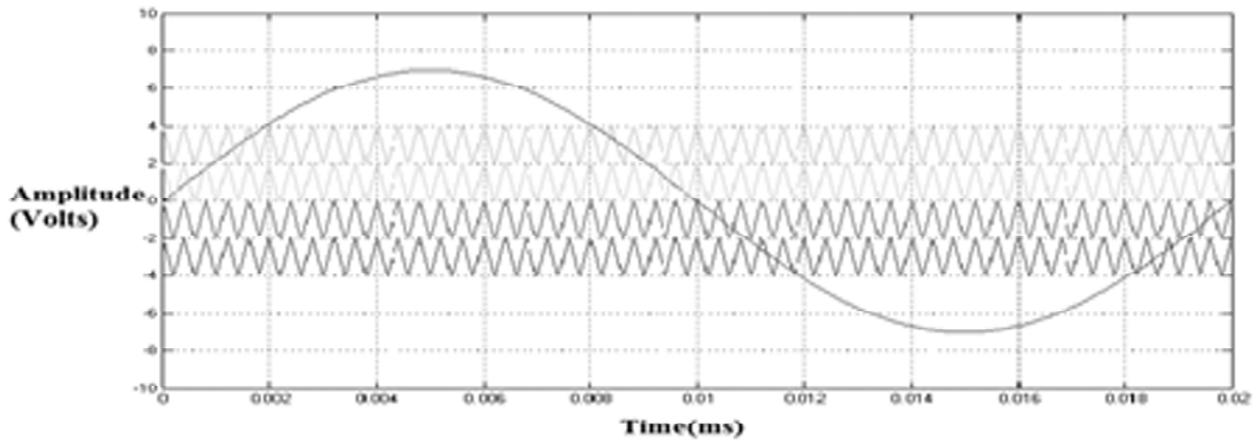


Figure 13: Carrier and reference wave for phase disposition.

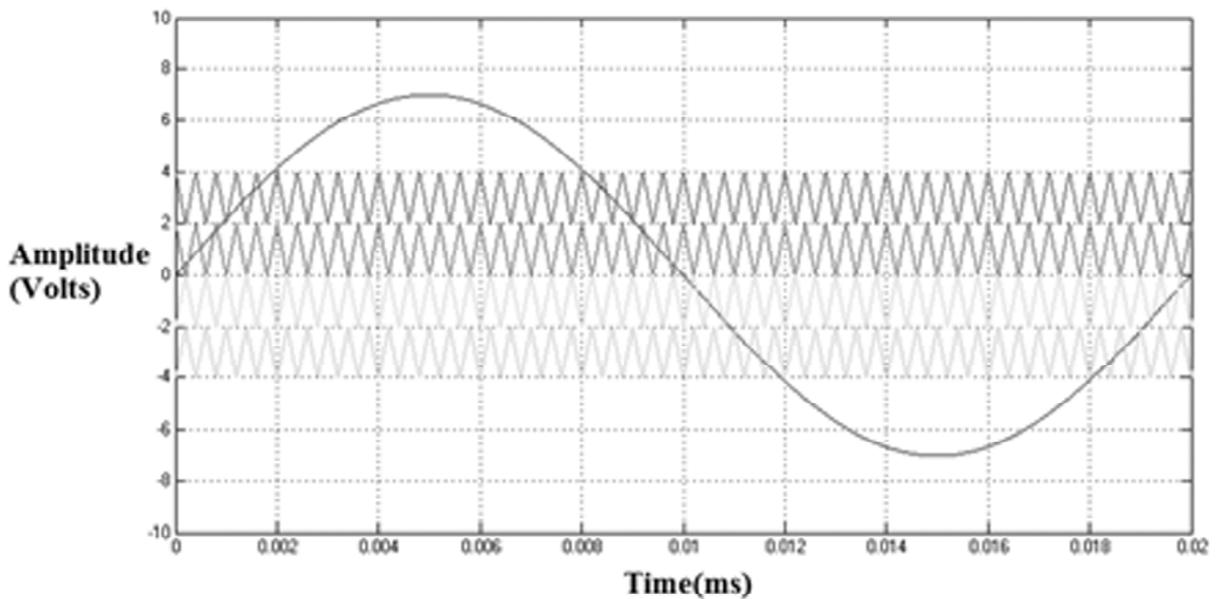


Figure 14: Carrier and reference waves for phase oppose disposition.

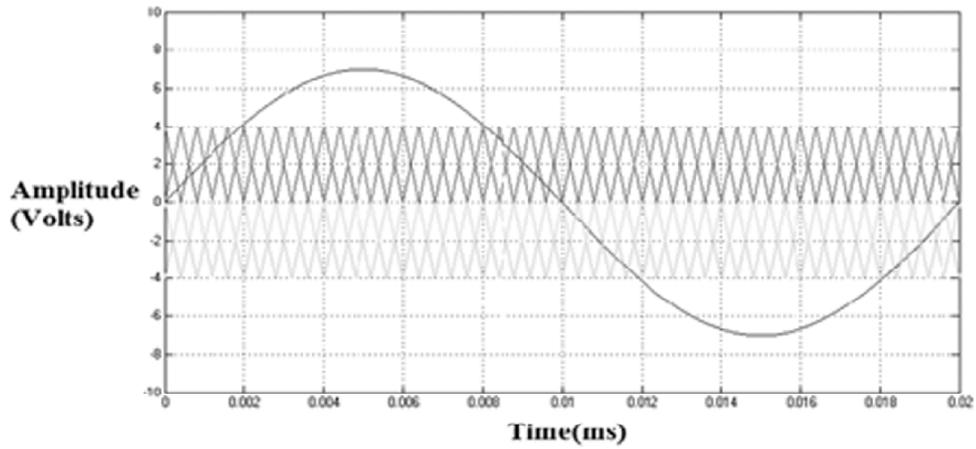


Figure 15: Carrier and reference waves for alternate phase oppose disposition.

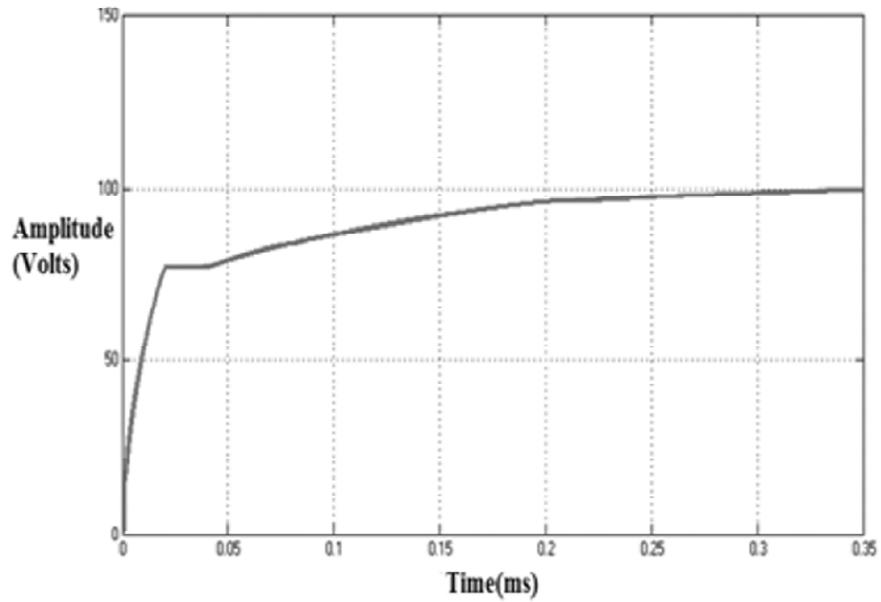


Figure 16: Output voltage of boost converter

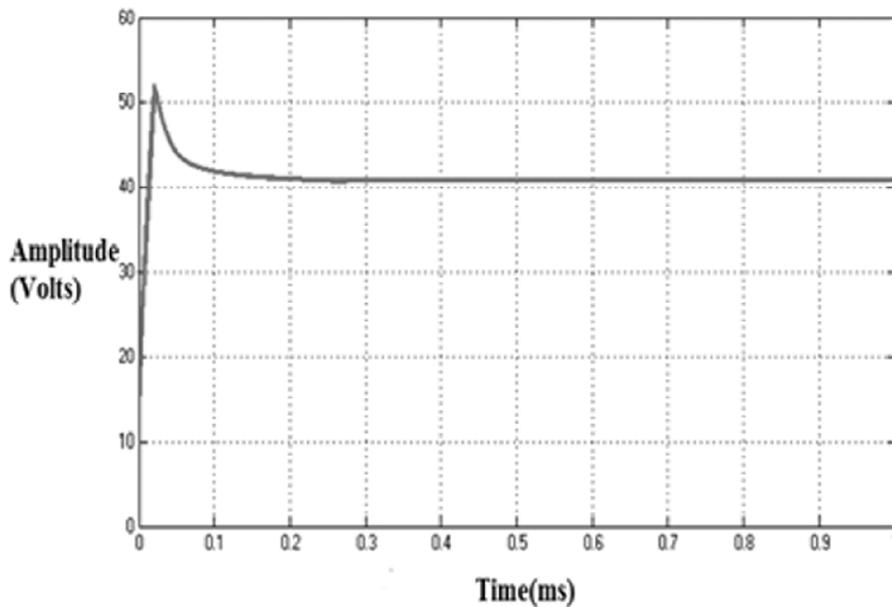


Figure 17: Output voltage of flyback converter

The output voltage for seven-level inverter is shown in the Figure 18. Here switches S1 and S4 of the full bridge inverter conduct to produce $1V_{DC}$. The switches S_{S1} and S_{S2} of the capacitor selection circuit are operated at high frequency and because of these switches $2V_{DC}$ and $3V_{DC}$ are obtained.

The simulation circuit for nine-level inverter fed boost converter is shown in Figure 19.

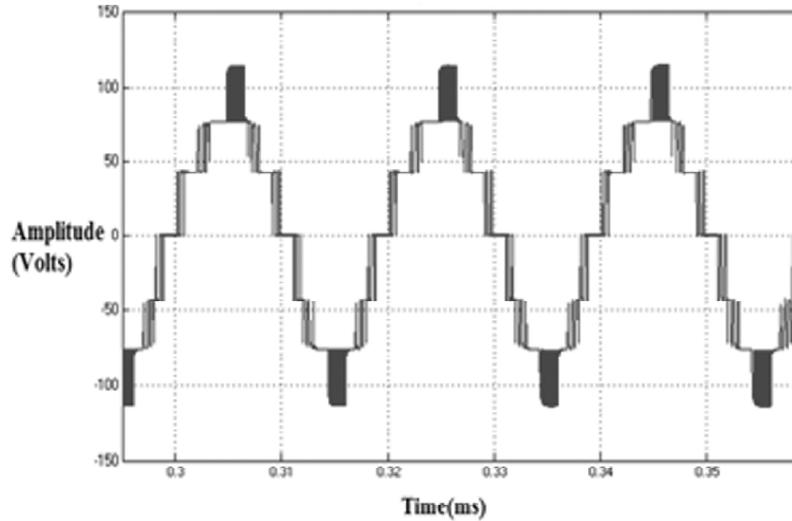


Figure 18: Output voltage waveform of seven level inverter

Table 1
THD's and 3rd harmonic levels for seven-level inverter

Techniques	THD	3 rd harmonic
Phase disposition(PD)	24.04	14.54
Phase oppose disposition(POD)	24.26	14.53
Alternate Phase Oppose disposition(POD)	23.02	13.96

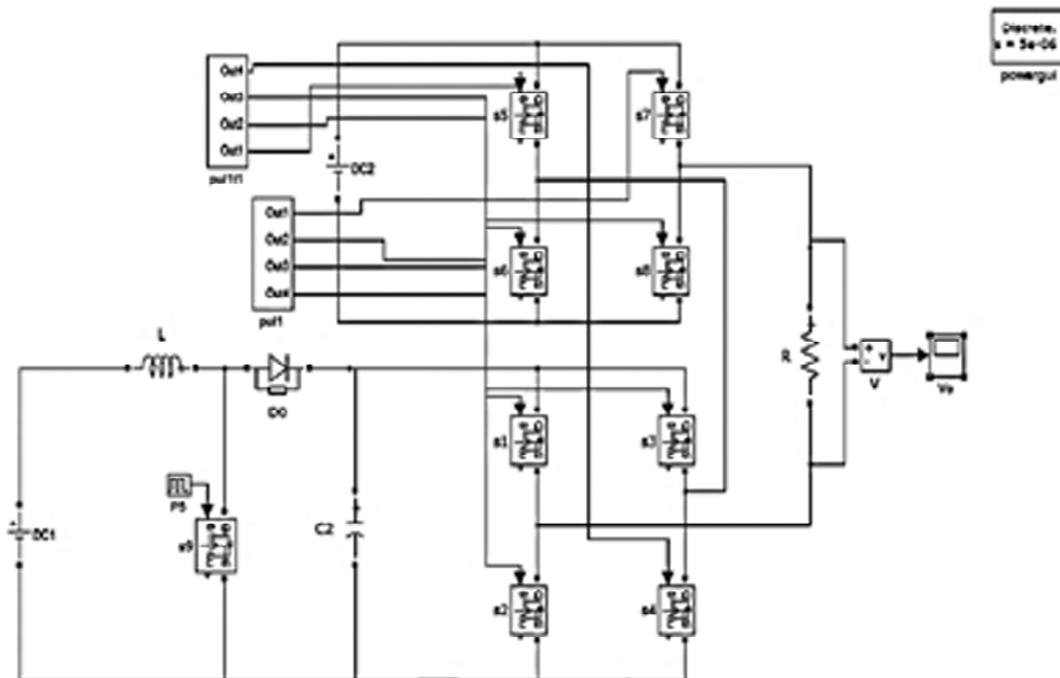


Figure19: Simulation circuit for nine level inverter fed boost converter

As seen in the Figure boost converter is integrated with nine- level inverter. Here multicarrier PWM techniques such as Phase disposition (PD), Phase Oppose disposition (POD), Alternate Phase Oppose Disposition (APOD) is used to generate pulses for inverter.

The carrier and reference waveform for phase disposition technique is shown in the Figure 20. It is seen that all carrier waves are in phase with each other and is compared with reference sinusoidal signal.

The carrier and reference waveform for phase oppose disposition is shown in the Figure 21. Carrier waves above the reference axis are in phase with each other. These waves are phase shifted by 180° to the carrier waves below the reference axis.

The carrier and reference waveform for alternate phase oppose disposition is shown in the Figure 22. Each carrier wave is out of phase with neighbouring carrier wave.

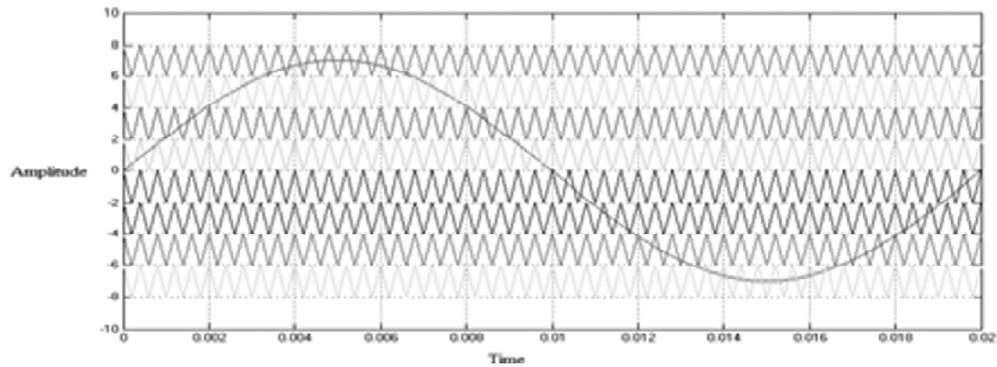


Figure 20: Carrier and reference wave for phase disposition.

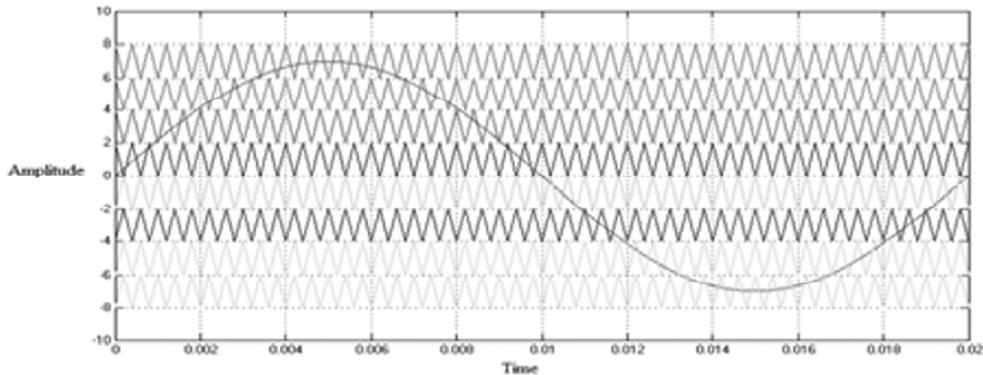


Figure 21: Carrier and reference wave for phase oppose disposition

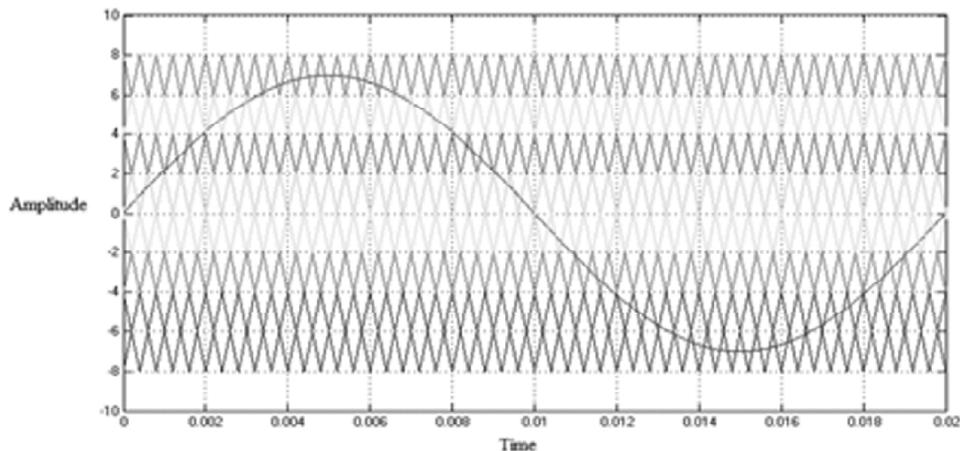


Figure 22: Carrier and reference wave for alternate phase oppose disposition

The output voltage waveform for boost converter is shown in the Figure 23. Here output voltage obtained is 150V.

When the switches S2, S4, S5, and S8 are conducting then the voltage generated is V_{DC} . When the switches S1, S4, S6, and S7 are conducting then the voltage generated is $2V_{DC}$.

When the switches S1, S4, S5, and S7 are conducting the voltage generated is $3V_{DC}$. The output voltage waveform for nine-level inverter is shown in the figure 24. During positive half cycle when the switches S1, S4, S5, and S8 are conducting the generated voltage is $4V_{DC}$. When no switches are conducting then the voltage generated is zero. During negative half cycle the generated voltages are $-4V_{DC}$, $-3V_{DC}$, $-2V_{DC}$, $-V_{DC}$.

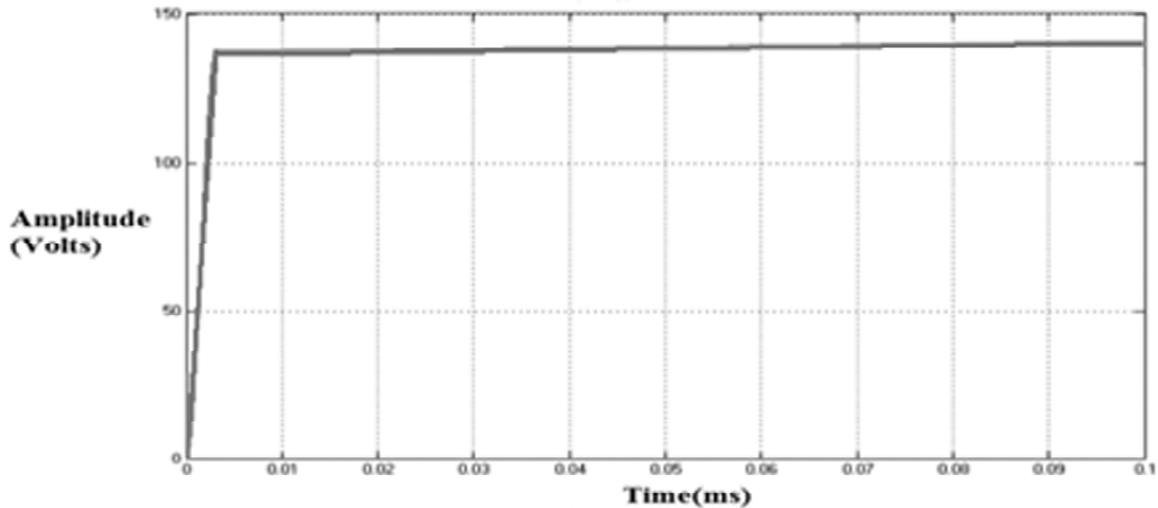


Figure 23: Output voltage of boost converter

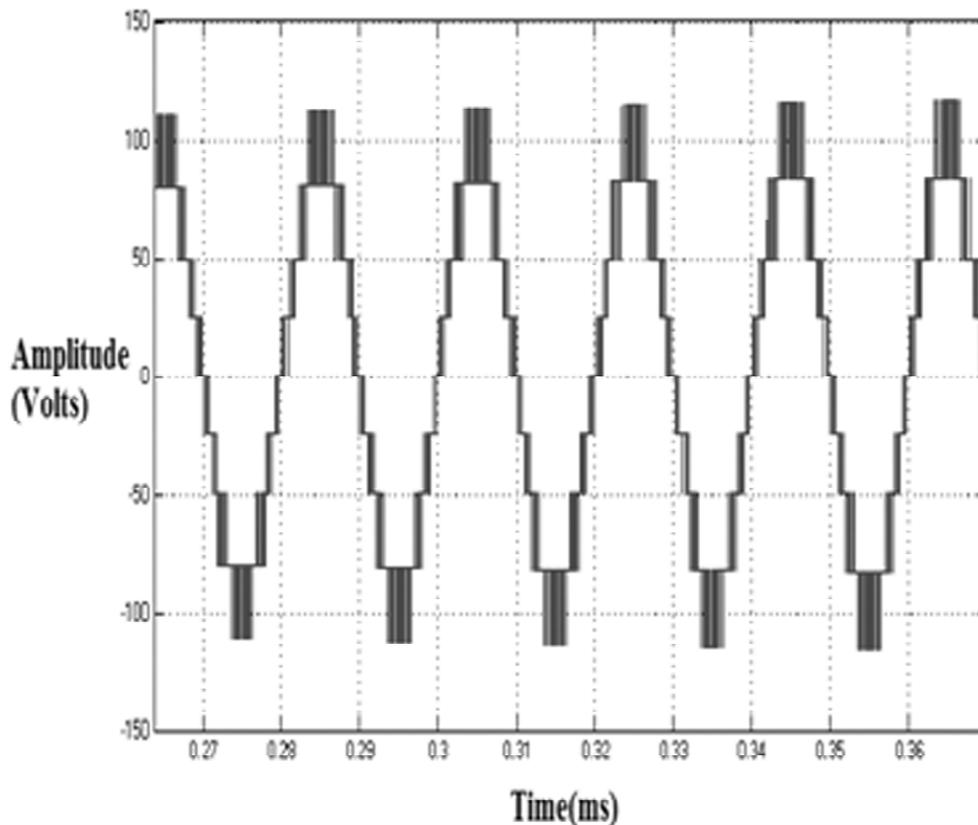


Figure 24: Output voltage of nine level inverter

Table 2
THD'S and 3rd harmonic levels for nine-level inverter

<i>Techniques</i>	<i>THD</i>	<i>3rd harmonic</i>
Phase disposition(PD)	18.04	2.04
Phase Oppose Disposition(APOD)	18.19	2.00
Alternate Phase Oppose Disposition(POD)	16.86	0.20

8. CONCLUSION

Thus the simulation of Seven Level Inverter and Nine Level Inverter fed with DC-DC Power Converter is done. Here multicarrier PWM techniques namely Phase Disposition (PD), Phase Oppose Disposition (POD), Alternate Phase Oppose Disposition (APOD) is implemented and comparison between these inverters such as THD, 3rd harmonic level is shown. Simulation results shows that the nine level inverter shows better performances in terms of THD's and 3rd harmonic level compared to seven level inverter.

REFERENCES

- [1] R. A. Mastromauro, M. Liserre, and A. Dell'Aquila, "Control issues in single-stage photovoltaic systems: MPPT, current and voltage control," *IEEE Trans. Ind. Informat.*, vol. 8, no. 2, pp. 241–254, May. 2012.
- [2] Z. Zhao, M. Xu, Q. Chen, J. S. Jason Lai, and Y. H. Cho, "Derivation, analysis, and implementation of a boost–buck converter-based high-efficiency pv inverter," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1304–1313, Mar. 2012.
- [3] M. Hanif, M. Basu, and K. Gaughan, "Understanding the operation of a Z-source inverter for photovoltaic application with a design example," *IET Power Electron.*, vol. 4, no. 3, pp. 278–287, 2011.
- [4] J.-M. Shen, H. L. Jou, and J. C. Wu, "Novel transformer-less grid-connected power converter with negative grounding for photovoltaic generation system," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1818–1829, Apr. 2012.
- [5] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics Converters, Applications and Design*, Media Enhanced 3rd ed. New York, NY, USA: Wiley, 2003.
- [6] K. Hasegawa and H. Akagi, "Low-modulation-index operation of a five level diode-clamped pwm inverter with a dc-voltage-balancing circuit for a motor drive," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3495–3505, Aug. 2012.
- [7] E. Pouresmaeil, D. Montesinos-Miracle, and O. Gomis-Bellmunt, "Control scheme of three-level NPC inverter for integration of renewable energy resources into AC grid," *IEEE Syst. J.*, vol. 6, no. 2, pp. 242–253, Jun. 2012.
- [8] S. Srikanthan and M. K. Mishra, "DC capacitor voltage equalization in neutral clamped inverters for DSTATCOM application," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2768–2775, Aug. 2010.
- [9] M. Chaves, E. Margato, J. F. Silva, and S. F. Pinto, "New approach in back-to-back m-level diode clamped multilevel converter modelling and direct current bus voltages balancing," *IET power Electron.*, vol. 3, no. 4, pp. 578–589, 2010.
- [10] J. D. Barros, J. F. A. Silva, and E. G. A. Jesus, "Fast-predictive optimal control of NPC multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 2, pp. 619–627, Feb. 2013.
- [11] A. K. Sadigh, S. H. Hosseini, M. Sabahi, and G. B. Gharehpetian, "Double flying capacitor multicell converter based on modified phase-shifted pulsewidth modulation," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1517–1526, Jun. 2010.
- [12] S. Thielemans, A. Ruderman, B. Reznikov, and J. Melkebeek, "Improved natural balancing with modified phase-shifted PWM for single-leg five level flying-capacitor converters," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1658–1667, Apr. 2012.
- [13] S. Choi and M. Saeedifard, "Capacitor voltage balancing of flying capacitor multilevel converters by space vector PWM," *IEEE Trans. Power Delivery*, vol. 27, no. 3, pp. 1154–1161, Jul. 2012.
- [14] L. Maharjan, T. Yamagishi, and H. Akagi, "Active-power control of individual converter cells for a battery energy storage system based on a multilevel cascade pwm converter," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1099–1107, Mar. 2012.
- [15] J. Chavarria, D. Biel, F. Guinjoan, C. Meza, and J. J. Negroni, "Energy balance control of PV cascaded multilevel grid-connected inverters under level-shifted and phase-shifted PWMs," *IEEE Trans. Ind. Electron.*, vol. 60, no. 1, pp. 98–111, Jan. 2013.
- [16] J. Pereda and J. Dixon, "High-frequency link: A solution for using only one DC source in asymmetric cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 3884–3892, Sep. 2011.

- [17] N. A. Rahim, K. Chaniago, and J. Selvaraj, "Single-phase seven-level grid-connected inverter for photovoltaic system," *IEEE Trans. Ind. Electr.*, vol. 58, no. 6, pp. 2435–2443, Jun. 2011.
- [18] Y. Ounejjar, K. Al-Hadded, and L. A. Dessaint, "A novel six-band hysteresis control for the packed U cells seven-level converter: Experimental validation," *IEEE Trans. Ind. Electron.*, vol. 59, no. 10, pp. 3808–3816, Oct. 2012.
- [19] J. Mei, B. Xiao, K. Shen, and L. M. Jian Yong Zheng, "Modular multilevel inverter with new modulation method and its application to photovoltaic grid-connected generator," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5063–5073, Nov. 2013.
- [20] I. Abdalla, J. Corda, and L. Zhang, "Multilevel DC-link inverter and control algorithm to overcome the PV partial shading," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 11–18, Jan. 2013.
- [21] J. M. Shen, H. L. Jou, and J. C. Wu, "Novel transformer-less grid connected power converter with negative grounding for photovoltaic generation system," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1818–1829, Apr. 2012.
- [22] R. Gonzalez, J. Lopez, P. Sanchis, and L. Marroyo, "Transformerless inverter for single-phase photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 693–697, Mar. 2007.
- [23] N. Femia, G. Petrone, G. Spagnuolo, and M. Vitelli, "Optimization of perturb and observe maximum powerpoint tracking method," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 963–973, Jul. 2005.
- [24] G. Petrone, G. Spagnuolo, R. Teodorescu, M. Veerachary, and M. Vitelli, "Reliability issues in photovoltaic power processing systems," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2569–2580, Jul. 2008.
- [25] R. A. Mastromauro, M. Liserre, and A. Dell'Aquila, "Study of the effects of inductor non linear behavior on the performance of current controllers," *IEEE Trans. Ind. Electron.*, vol. 55, no. 5, pp. 2043–2052, May 2008.
- [26] D. N. Zmood and D. G. Holmes, "Stationary frame current regulation of PWM inverters with zero steady-state error," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 814–822, May 2003.
- [27] T. Eramand P.L. Chapman, "Compar is on of photo voltaic array maximum power point tracking techniques," *IEEE Trans. Energy Convers.*, vol. 22, no.2, pp.439–449, Jun.2007
- [28] C. S. Ma, T. J. Kim, D. W. Kang, and D. S. Hyun, "A simple control strategy for balancing the DC-link voltage of neutral-point-clamped inverter at low modulation index," in *Proc. IECON*, Nov. 2–6, 2003, pp. 2167–2172.
- [29] J. H. Suh, C. H. Choi, and D. S. Hyun, "A new simplified space-vector PWM method for three-level inverters," in *Conf. Rec. APEC*, Mar. 14–18, 1999, pp. 515–520.
- [30] Y. H. Lee, R. Y. Kim, and D. S. Hyun, "A novel SVPWM strategy considering DC-link balancing for a multilevel voltage source inverter," in *Proc. IEEE Appl. Power. Electron. Conf.*, Mar. 14–18, 1999, pp. 509–514.
- [31] R. Vargas, P. Cortes, U. Ammann, J. Rodriguez, and J. Pont, "Predictive control of a three-phase neutral point clamped inverter," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2697–2705, Oct. 2007.
- [32] F. Z. Peng, "A generalized multilevel inverter topology with self voltage balancing," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 611–618, Mar./Apr. 2001.
- [33] M. Marchesoni and P. Tenca, "Diode-clamped multilevel converters: A practicable way to balance DC-link voltages," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 752–765, Aug. 2002.
- [34] G.P. Adam, S.J. Finney, A.M. Massoud, and B.W. Williams, "Capacitor balance issues of the diode-clamped multi level inverter operated in a quasi two-state mode," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 3088–3099, Aug. 2008.
- [35] J. A. Barrena, L. Marroyo, M. A. R. Vidal, and J. R. T. Apraiz, "Individual voltage balancing strategy for PWM cascaded H-Bridge converter based STATCOM," *IEEE Trans. Ind. Electron.*, vol. 55, no. 1, pp. 21–29, Jan. 2008.