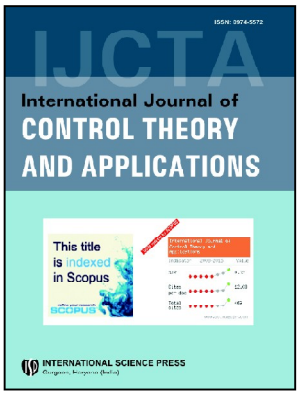

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Design of Low Power PISO & PIPO Shift Registers using Lector Technique in 50nm Technology

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Abstract: Power dissipation is of import intellection in the design of CMOS VLSI circuits. High power consumption leads to decrease in the battery life in the suit of battery-powered utilization and affects reliability, packaging and cooling costs. The development of digital integrated circuits is challenged by higher power consumption as voltages scale downward with the geometries, outset voltages must also drop-off to gain the execution advantages of the new technology, but leakage current increases exponentially leading to increase in leakage power. Today leakage power has become an progressively crucial issue in processor hardware and software design. With the main section of leakage, the sub-threshold current, drastically raises with the decay of device dimensions, leakage commands an ever exploding share in the processor power consumption. If the circuit is idle there is a large amount of power will be wasted because of Leakage currents. Efficient leakage power reduction techniques have become critical for the deep submicron and nanometre circuits. In this paper, a 4-bit PISO and PIPO Shift registers are designed using LECTOR technique and is analysed with different types of sleep techniques. In this paper, digital schematic editor (DSCH2) for designing; simulation and layout generation is done using Micro Wind Layout Editor.

Keywords: *CMOS Scaling, Leakage power, D flip-flop, Shift Register, Dual sleep, Dual stack, Stacked sleep, LECTOR*

I. INTRODUCTION

Power consumption is one of the major issues of VLSI circuit design, for which CMOS is the primary technology. The power consumption of CMOS consists of dynamic and static components. Dynamic power is used up when transistors are changing, and inactive power is consumed regardless of transistor switching. Dynamic power consumption was antecedently the individual largest interest for low-power chip designers since changing power accounted for 90% or more of the total chip power. Still, as the feature size diminish, e.g., to 90nm and below, static power has become a great challenge for current and future technologies.

The scaling of procedure technologies to Nano meter regimen has resulted in a speedy increase in leakage power dissipation. Hence, there is a great need to reduce static power dissipation during periods of inactivity. The power reduction requisite be achieved without trading-off performance which makes it difficult to diminish

leakage during normal operation. There are different VLSI techniques to trim down leakage power. Scaling improves transistor density and practicality on a chip.

Scaling helps to increment speed and frequency of operation and hence higher performance. As voltages scale downward with the dimensions, threshold voltages must also decrement to gain the performance advantages of the new technology but leakage current increases exponentially. Gating of Power supply is one such well known technique where a sleep transistor is added between actual ground rail and virtual ground. In this paper, we describe a new technique called as LECTOR (LEakage Control TransistOR) for leakage power reduction for designing 4-bit PISO and PIPO Shift registers using CMOS technology. Former techniques are concise and compared with LECTOR approach presented in this paper.

II. SHIFT REGISTERS

To store digital data, a type of sequential logic circuit called as Shift registers were used. They are a group of flip-flops connected in a series so that the output from one flip-flop becomes the input of the next flip-flop. All flip-flops is driven by a same clock pulse, and all are set or reset at the same time. Since the shift register stores data it implemented using flip-flops. In this paper D flip-flop were used to design shift registers.

Types of shift registers

Parallel in - Serial Out Shift Registers

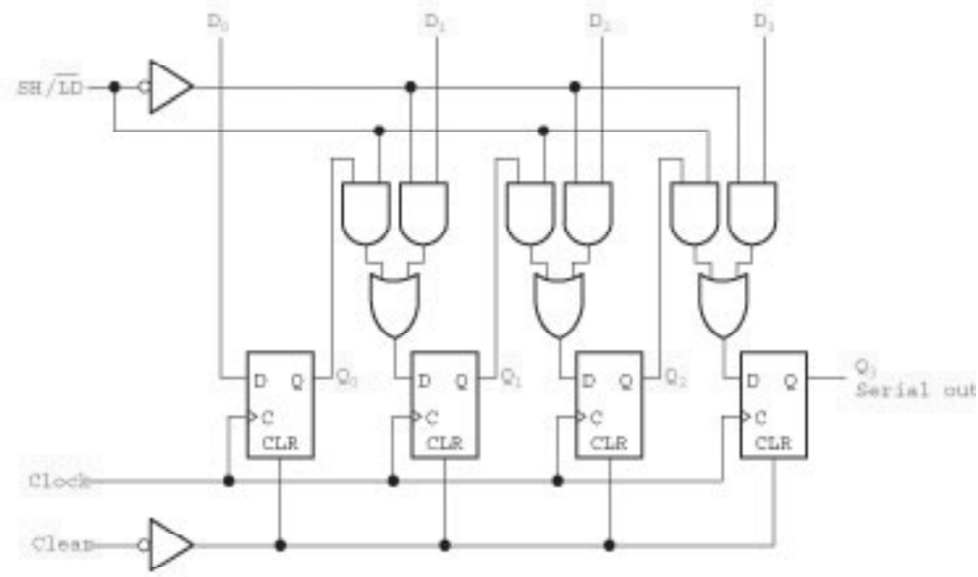

Figure 1: Four-Bit PISO Shift Register

Data bits are get into parallel fashion. The circuit shown below is a four-bit parallel input serial output register. Output of past Flip Flop is related to the input of the next one via a combinational circuit. Shift mode or load mode are the two common modes which this circuit can work.

Parallel in - Parallel Out Shift Registers

For PIPO shift registers, all data bits appear on the parallel outputs immediately following the co-occurring entry of the data bits. The below given circuit is a 4-bit PIPO shift register build using D flip-flops.

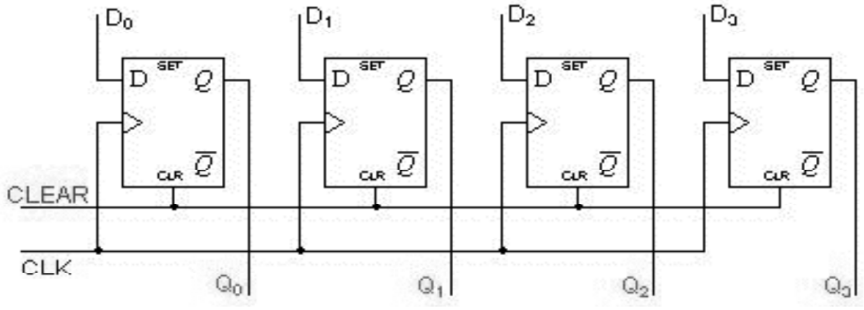

Figure 3: Four-Bit PIPO Shift Register

In this circuit, parallel inputs are D's and parallel outputs are the Q's. The data at the D flip-flop inputs appears at the corresponding outputs simultaneously, Once the register is clocked.

III. SLEEP TECHNIQUES

(A) Dual Sleep Transistor Approach

Different types of methods are existed for leakage power reduction. One of such methods is dual sleep transistor approach. It uses two extra pull- up and two excess pull-down transistors in sleep mode either in OFF state or in ON state.

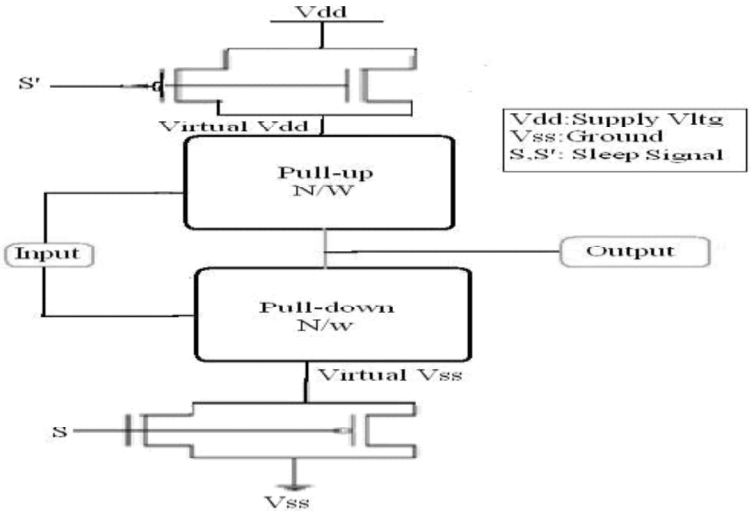

Figure 4: Dual Sleep Transistor Approach

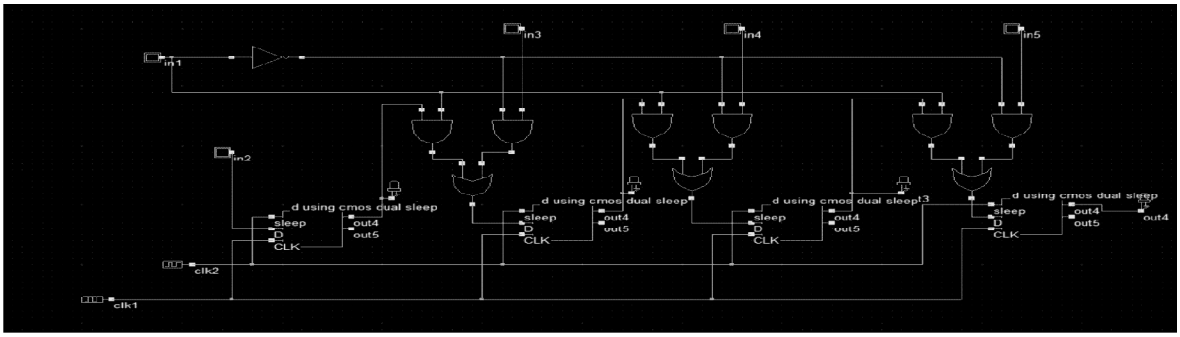

Figure 5: Block Diagram of PISO using dual sleep

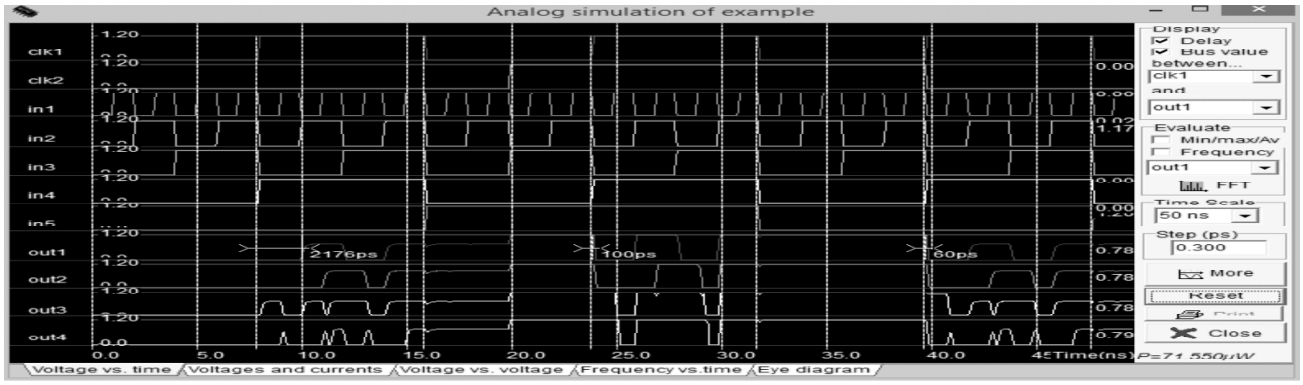

Figure 6: Simulation result of PISO using dual sleep

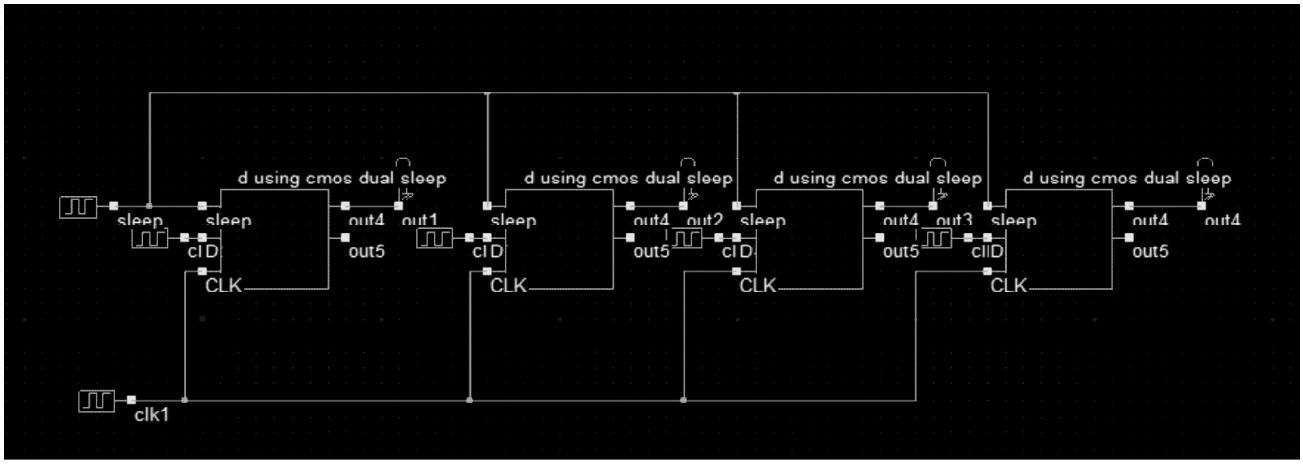

Figure 7: Block Diagram of PIPO using dual sleep

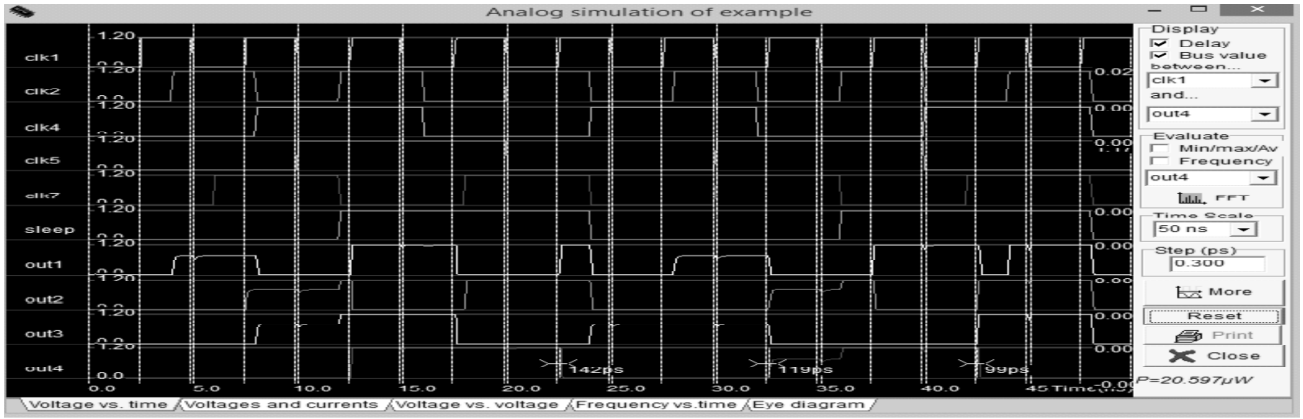

Figure 8: Simulation result of PIPO using dual sleep

(B) Dual Stack Approach

In dual stack approach, 2 PMOS in the pull- down network and 2 NMOS in the pull-up network are used in addition to the sleep transistors. The advantage is that NMOS degrades the high logic level while PMOS degrades the low logic level.

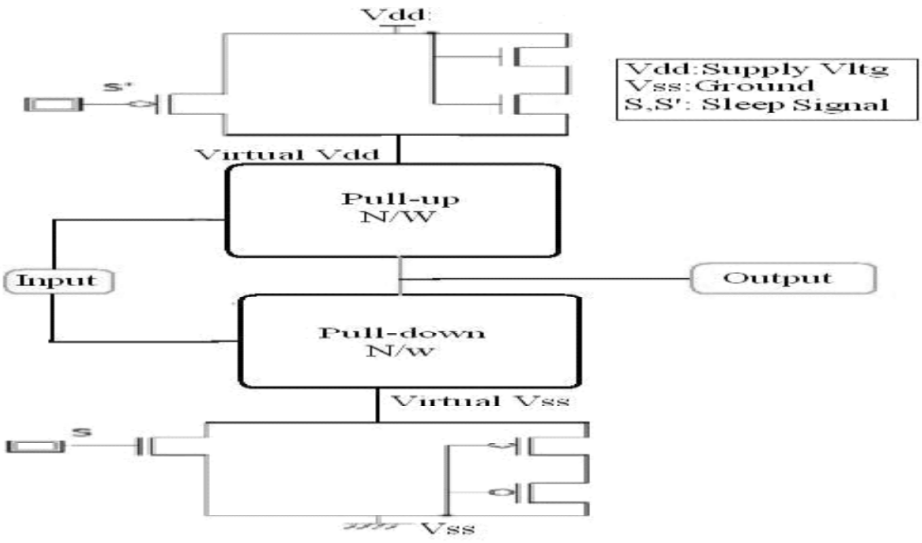

Figure 9: Dual Stack Approach

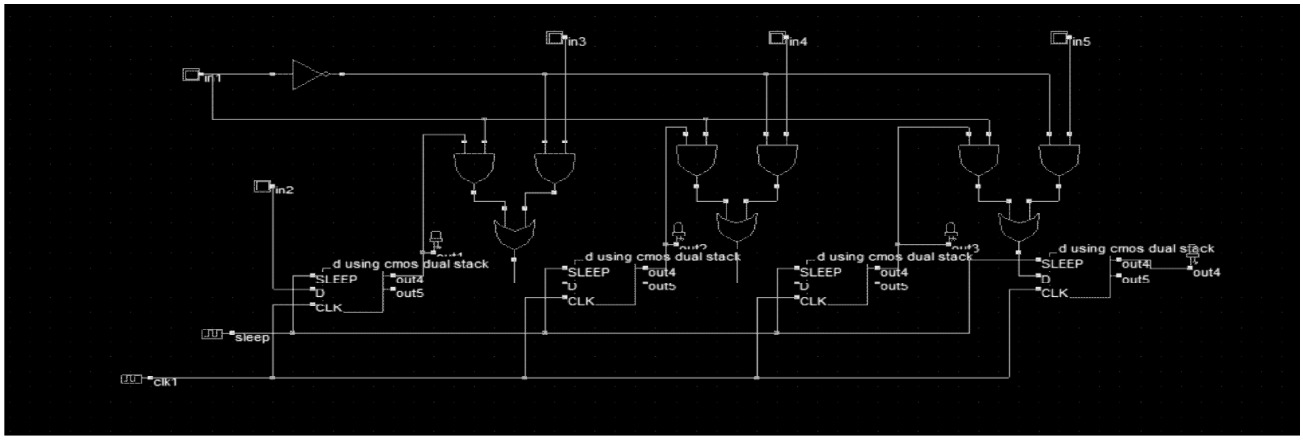

Figure 10: Block Diagram of PISO using dual stack

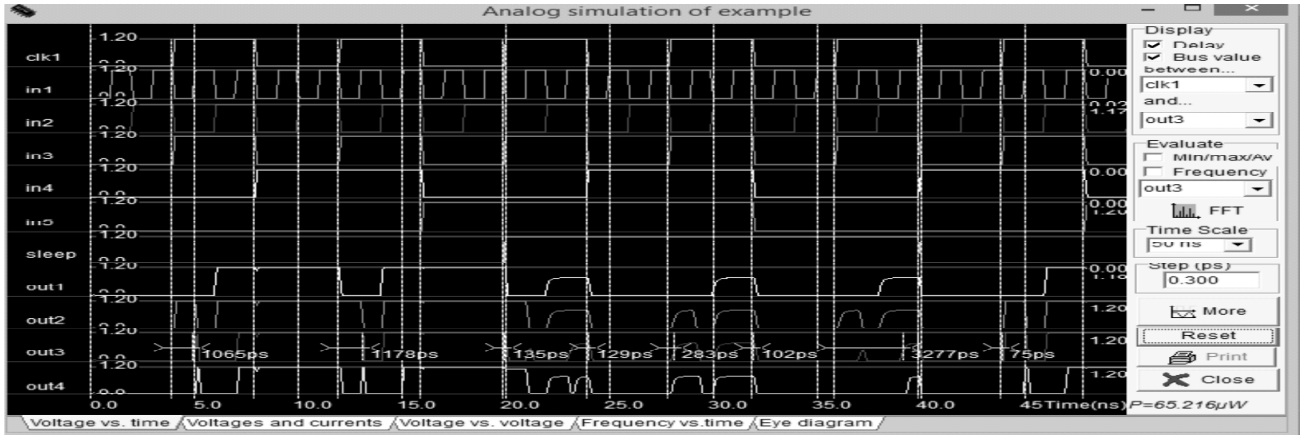

Figure 11: Simulation result of PISO using dual stack

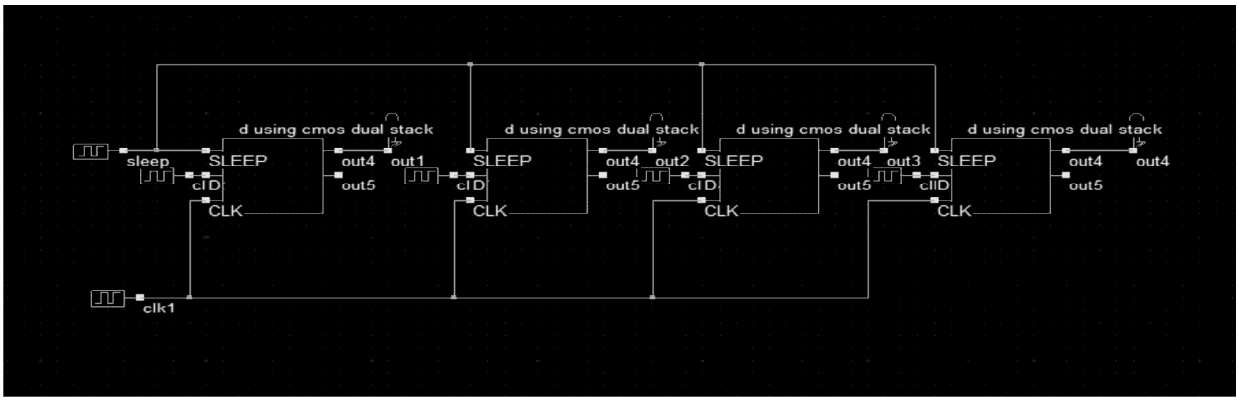

Figure 12: Block Diagram of PIPO using dual stack

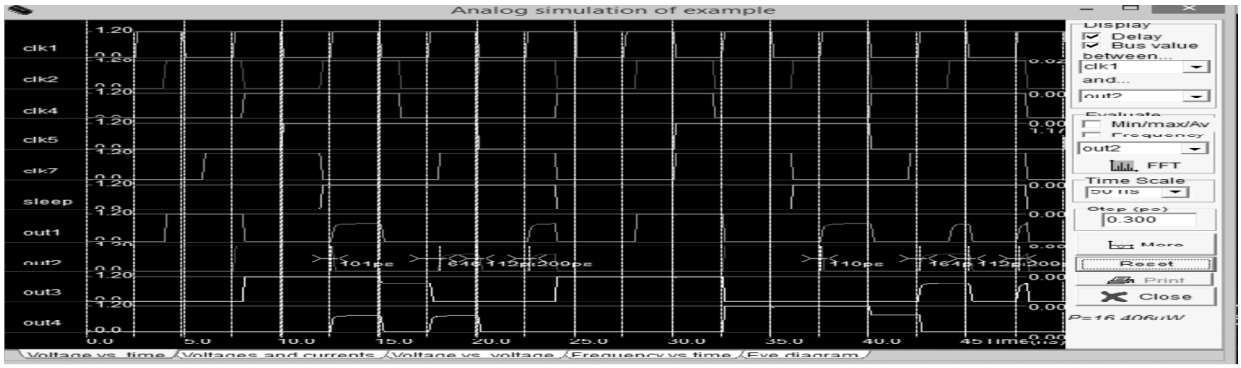

Figure 13: Simulation result of PIPO using dual stack

(C) Stacked Sleep Transistor Approach

In this technique, sleep transistor was acquiring stacked, which bring down the leakage current to great level. Two stacked sleep transistors in power supply bar and two stacked sleep transistor in ground were used in this approach. Thus leakage reduction takes place in two steps. Firstly, due to stack effect of sleep transistor and next due to sleep transistor itself. It is notable fact that NMOS are not efficient in transient the power supply. But in this technique, stacked sleep transistor uses PMOS in the power supply and NMOS in the ground for maintaining exact logic state of the circuit.

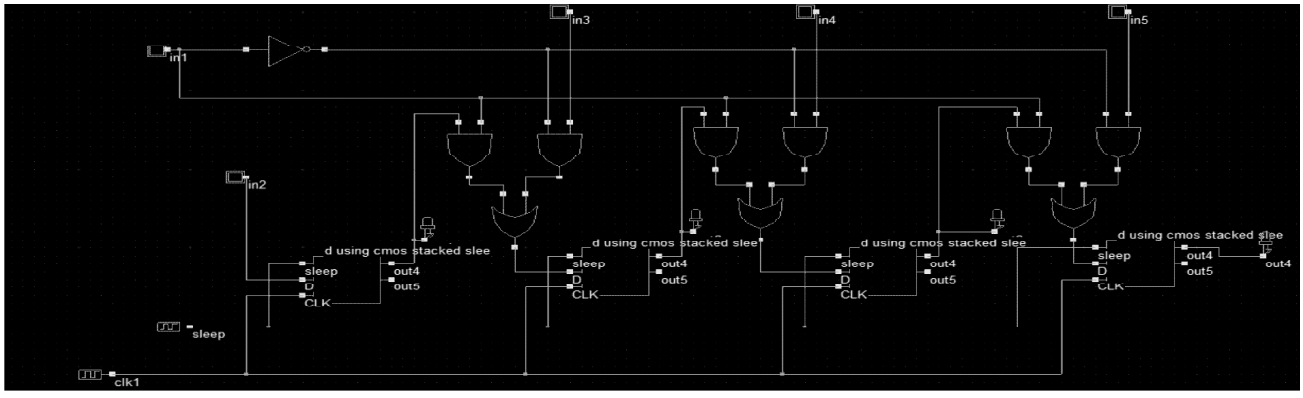

Figure 15: Block Diagram of PISO using stacked sleep

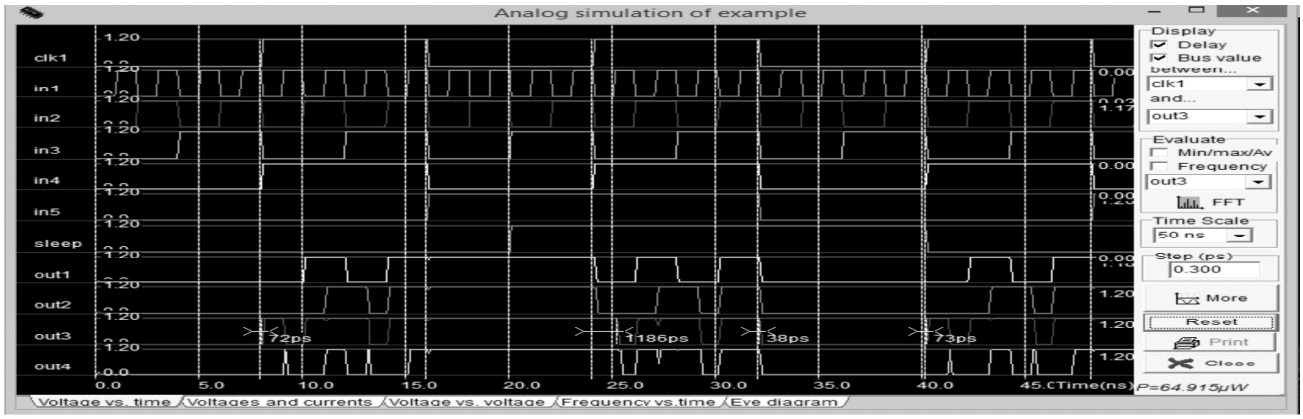

Figure 16: Simulation result of PISO using stacked sleep

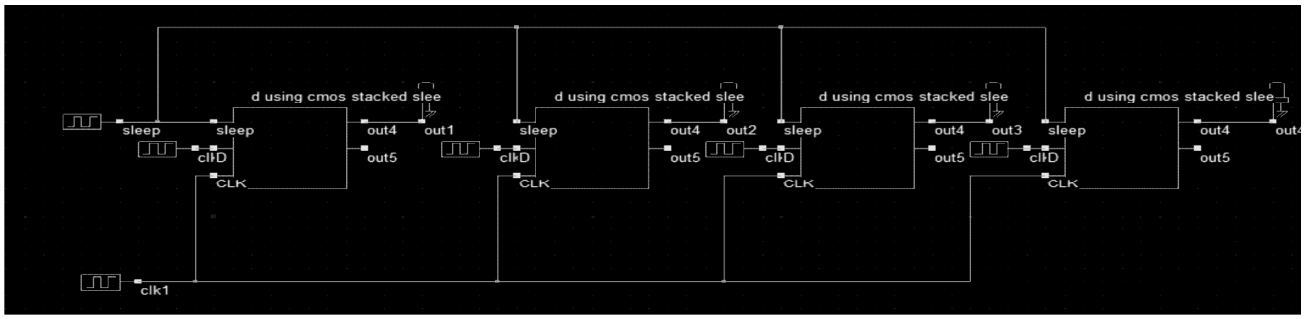

Figure 17: Block Diagram of PIPO using stacked sleep

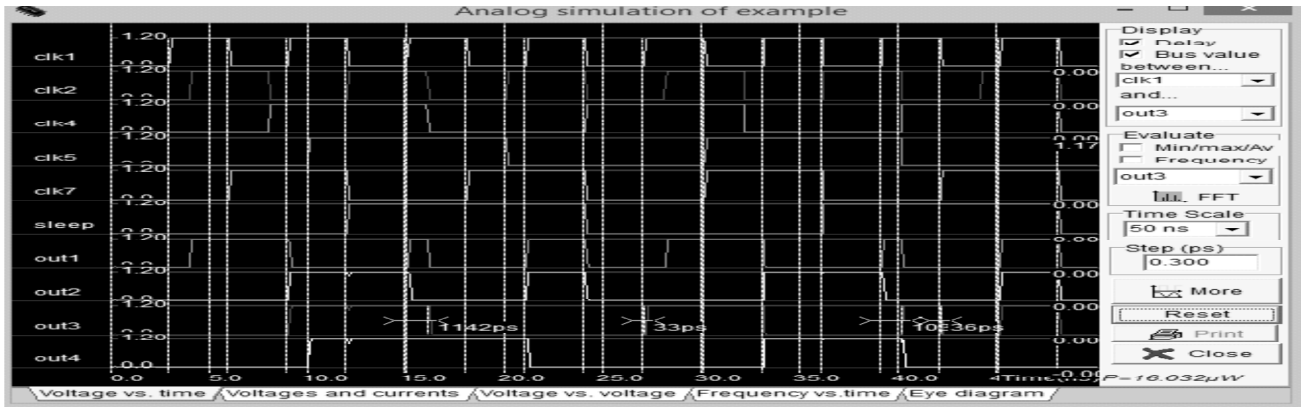

Figure 18: Simulation result of PIPO using stacked sleep

IV. PROPOSED TECHNIQUE

The proposed technique for leakage reduction in CMOS circuits is called LECTOR. It provides two Leakage Control Transistors (LCTs), a p- type and an n-type within the logic gate for which the gate terminal of each LCT is controlled by the source terminal of the other. LECTOR is efficient in idle and active states of the circuit resulting in better leakage reduction. Either one of the two LCTs is always "near its cut- off voltage" for any input vector combination, thus increasing the stacking effect without any additional control signal.

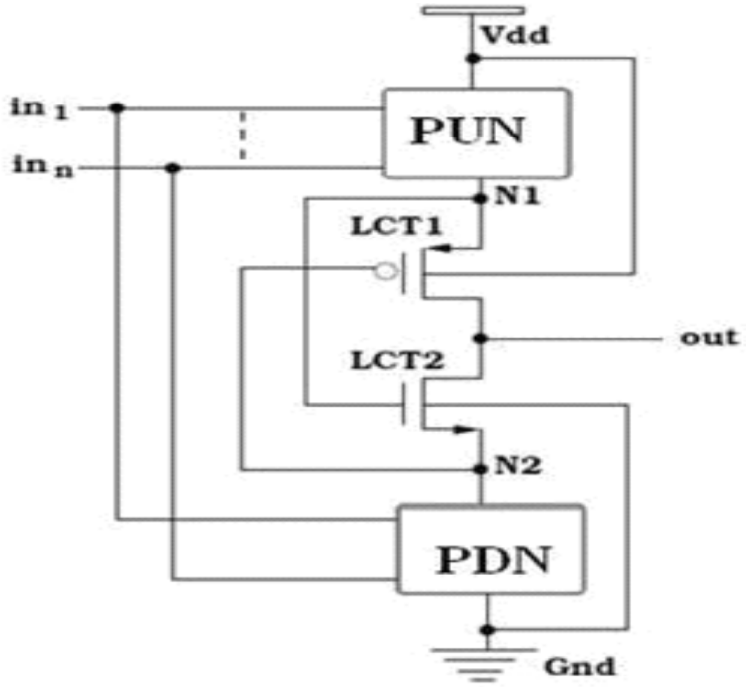

Figure 19: Lector technique

It works based on the fact that a state with more than one transistor off in a path from supply voltage to ground is distant little leaky than a state with only one transistor off in any supply to ground path. The LCTs are self-controlled and do not require any control logic unlike in the popularly used sleep transistor method. [12]

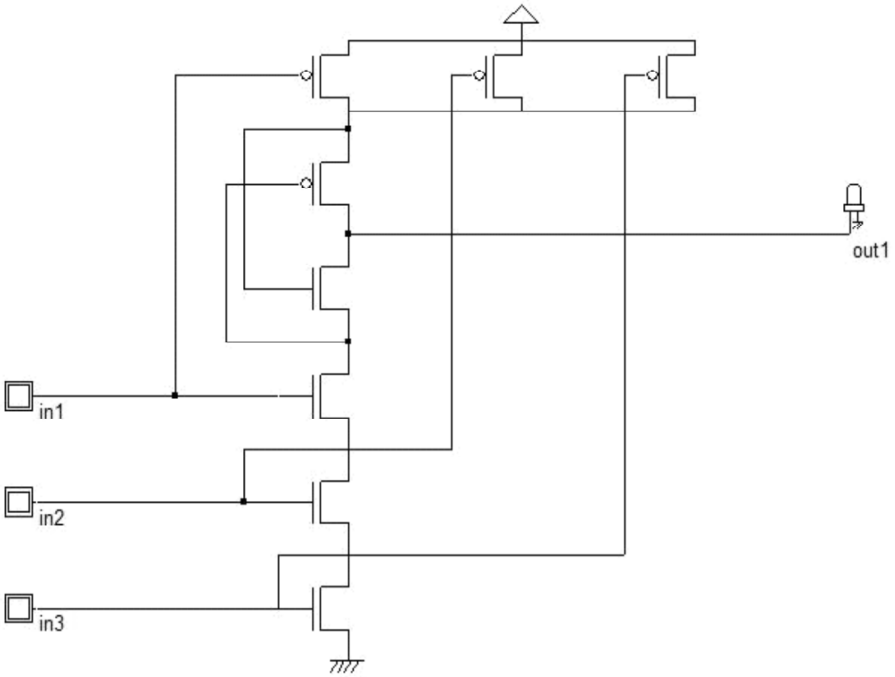

Figure 20: 3-input NAND gate using Lector

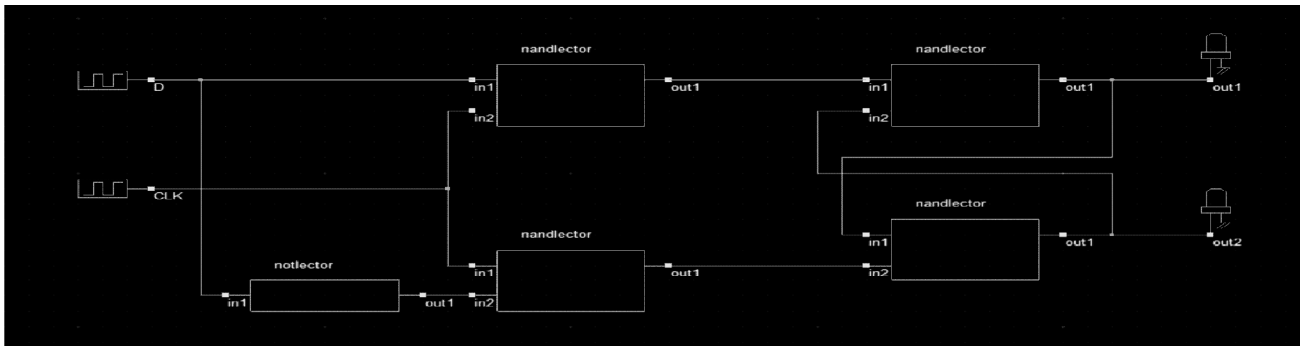

Figure 21: Block Diagram of D Flip Flop using Lector technique

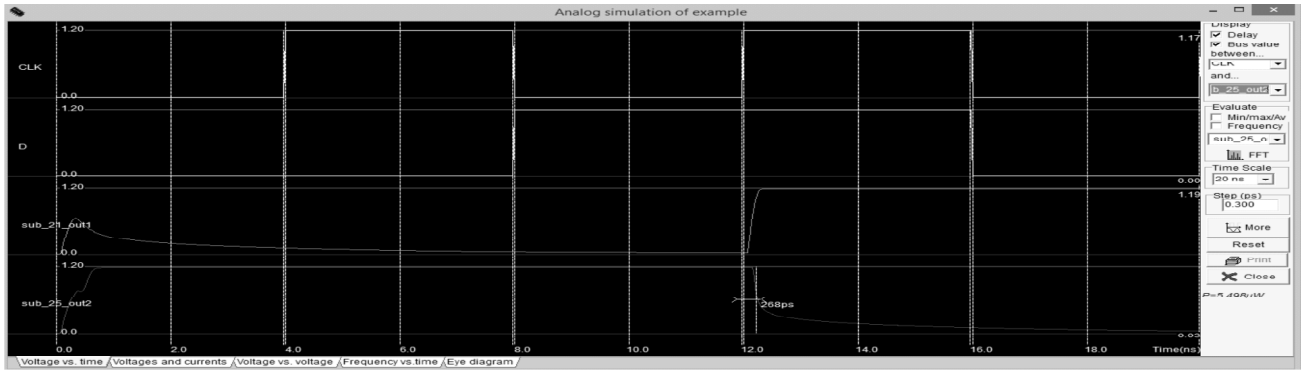

Figure 22: Simulation Result of D Flip Flop using Lector technique

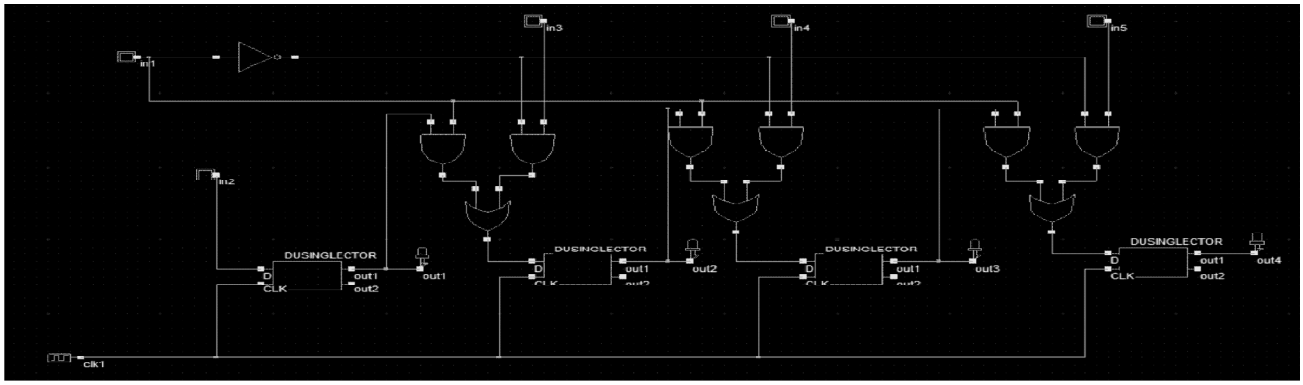

Figure 23: Block Diagram of PISO using Lector technique

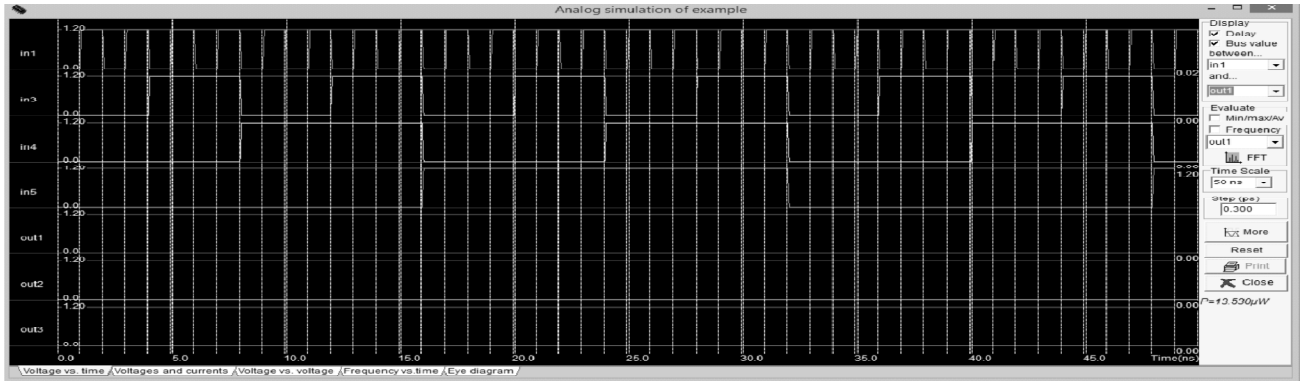

Figure 24: Simulation Result of PISO using Lector technique

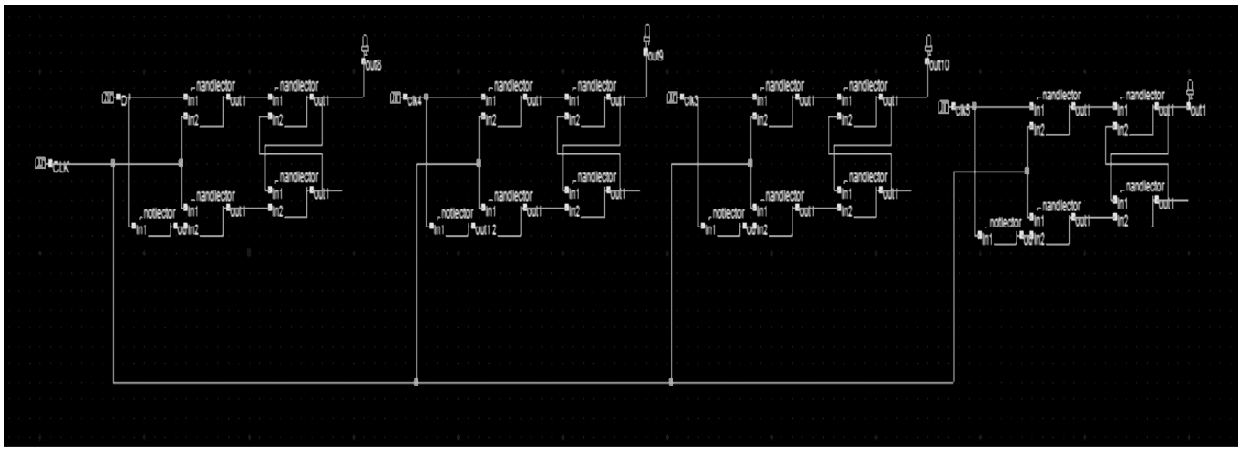

Figure 25: Block Diagram of PIPO using Lector technique

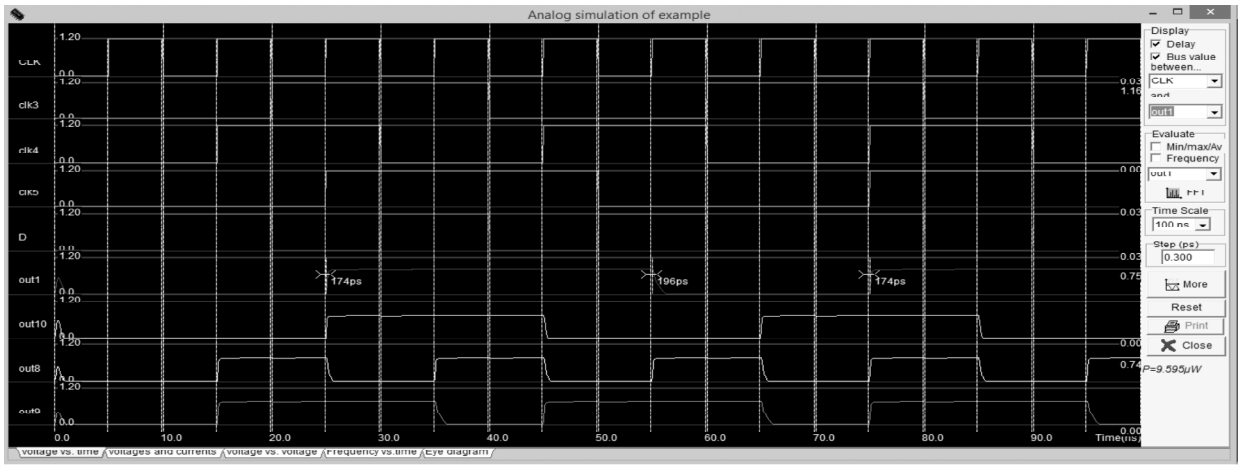

Figure 26: Simulation Result of PIPO using Lector technique

V. COMPARISON TABLE

We compare the LECTOR technique with different sleep techniques in terms of power consumption and the results are tabulated.

Table 1
Comparison table of power dissipation of d- flip flop and shift register types in all sleep techniques and proposed technique

APPROACH (*µm*)	*D-FLIP FLOP* (*µm*)	*PISO Shift Register* (*µm*)	*PIPO Shift Register* (*µm*)
LOGIC GATES	7.542	75.848	17.586
CMOS	12.579	75.634	29.463
DUAL SLEEP	7.512	71.550	20.597
DUAL STACK	6.699	65.216	16.406
STACKED SLEEP	6.713	64.915	16.032
LECTOR	**5.492**	**13.530**	**9.595**

VI. CONCLUSION

Sub threshold leakage power consumption in nano scale technology is great challenge to VLSI designers. Although there are several techniques to reduce leakage power, based upon the technology and design approach the designer can choose the techniques. In this paper, Power consumption of 4-bit PISO and PIPO Shift Register is reduced using different sleep methods and LECTOR technique. Unlike other leakage control techniques, LECTOR does not need any additional control circuitry to monitor the states of the circuit. Also the power consumption is greatly reduced using LECTOR technique with minimal possible area and this method can be used in various integrated circuits for power efficiency.

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