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Design of Glitch Free Universal Gates Based for Combinational and Sequential Circuit

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ABSTRACT

We present a glitch free module using strobe signal which overcomes the limitation of delay mismatch in a wide range of applications. The proposed strobe signal logic can control the occurrence of glitch at both the rising edge and falling edge of the circuit. The theoretical demonstration of the glitch free operation of the proposed strobe signal module is also derived in the paper. The previously proposed digitally controlled delay lines (DCDL) has been compared to this technology. Simulation results show the correctness of the module with no delay mismatch with respect to the previously proposed DCDL (Digitally -Controlled Delay Lines-)--. As an example application, the strobe signal logic is used in configurable error free frequency detector (a frequency counter) which can control the occurrence of glitch during the sudden modulation of the frequency. The employ of the proposed strobe signal can hold the operation of the gate for a specific time until the other gate completes its operation so that there is no delay mismatch.

Keywords: Digitally -Controlled Delay Lines (DCDL), Integral Non-Linearity(INL),strobe signal, configurable error free frequency detector, Tristate Inverter (TINV).

1. INTRODUCTION

In the most common applications digitally controlled delay lines are employed to process clock signals thus a Glitch free operation is a must. The necessary condition to avoid Glitching by using a DCDL (Digitally -Controlled Delay Lines)-[3] - which have no Glitch in presence of Delay control code switching. This approach use a DCDL (Digitally Controlled Delay Lines), delay cells chain and a MUX to choose the wanted cell output, but the MUX delay increases with the increase in number of cells[1], thus a DCDL (Digitally Controlled Delay Lines) topology is employed which uses a delay cells chain and consequently solves the trade of related to MUX of previous structures. The DCDL (Digitally Controlled Delay Lines-)- is constructed by using a regular cascade of equal delay elements. Glitching in these topologies can be avoided by using a thermometric code for the control bits. The further modifications can be carried by using the clock tree structure and double clock functionality but these structures consume more area and hard to design [2]. We present the design and experimental evaluation of the (STROBE) in this paper [3-6]. This logic circuit are used to reduce the low layout complexity and the control signal can be used in any platform and also it reduces the further chances for glitches to appear.

1.1. Electronics Glitch

An electronics glitch is an undesired transition that can occurs before the signal settles to its intended value. In other words, glitch is an electrical pulse of short duration that is usually occurred by a fault or design error, particularly in a digital circuit. For example, many electronic components, such as Flops are triggered by a pulse that must not be shorter than a specified minimum duration can be achieved. A pulse shorter than the specified minimum is called a glitch. A related concept is the run a pulse whose amplitude is lesser than the minimum level specified for correct operation, and a spike, a short pulse close to a glitch but often

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caused by crosstalk. A glitch can occur in the presence of race condition in a poorly designed digital logic circuit.

2. NAND-BASED DCDL AND CONTROL BITS DRIVING CIRCUITS

(A) Nand Based DCDL using Two Control Bits

The circuit is composed by a series of equal delay- elements (DE), each composed by four NAND gates. In the figure 1 —A denotes the fast input of each NAND gate. Gates marked with —D are dummy cells added for load balancing. The circuit delay is governed by control-bits Si, which encode the delay control-code with a thermometric code: Si = 0 for i < c and Si = 1for i > c. By using this encoding technic, each DE can be either in pass- state or in turn-state contain all NAND gates present the same load and, therefore in a first order approximation, present the same delay. The delay of each NAND gate can be obtained by low-to-high and high-to-low output commutation, respectively. In DCDL (Digitally Controlled Delay Lines-)-applications, can be avoided DCDL (Digitally Controlled Delay Lines-)- output Glitching, the switching of delay control-bits is synchronized with the switching of the input signal making control bit slower glitching can be avoided if the control-bits arrival time is lower-level than the arrival time of the input signal .The first DE which switches to the turn- state.

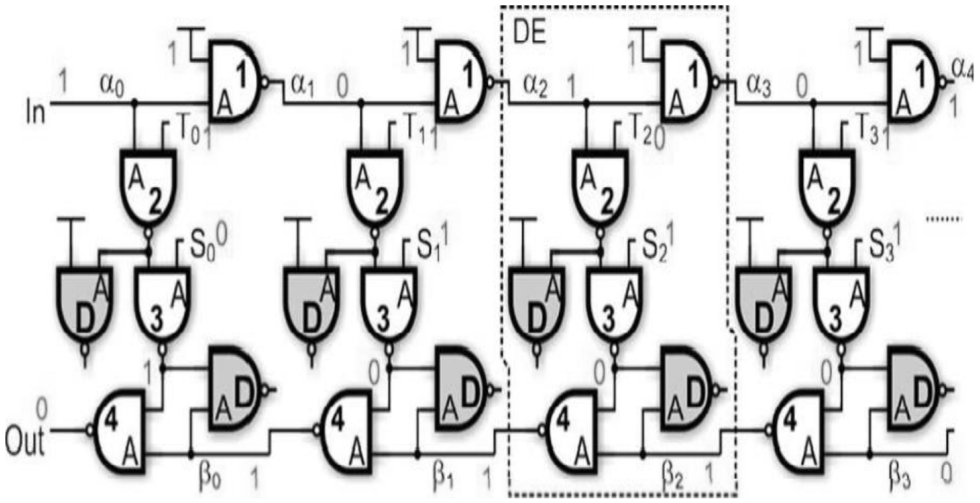

Figure 1: NAND Based DCDL with more delay elements

Waveform

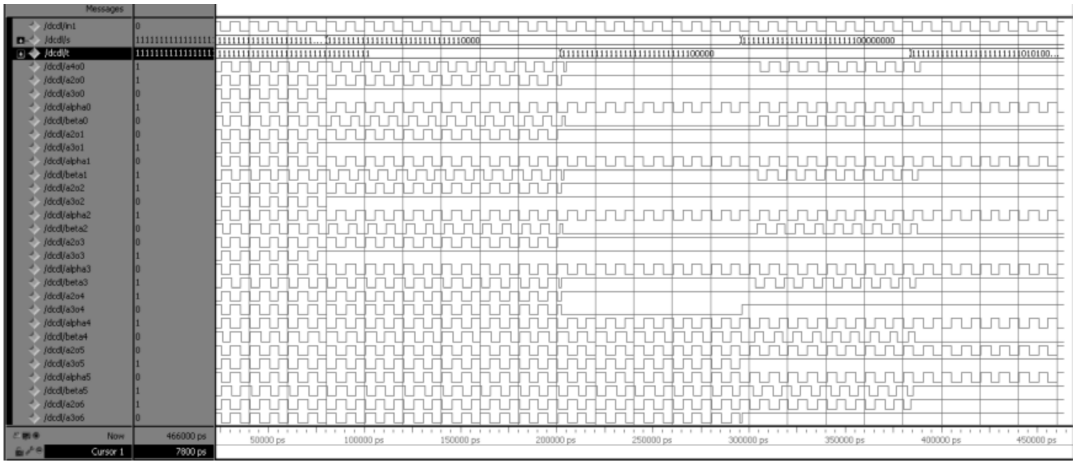

Figure 1.1: Simulation of *NAND Based DCDL*

The proposed technic is designed in a 90nm CMOS technology, with 1volt supply voltage. The Digitally Controlled delay lines contain 64 delay elements. All NAND based DCDL (Digitally Controlled Delay Lines) have been sized in order to optimize timing margin and reduce the glitching which is shown in figure 1.1. The output of the proposed DCDL (Digitally Controlled Delay Lines) is simulated by the three step switching mechanism. The simulation confirms that no Glitching is obtained at the output. By analyzing it is noted that Si- Selection bits signals have to be delayed with respect to Ti-Control bits signals to avoid glitches. But it cannot control the occurrence of glitch at both the rising edge and falling edge of the circuit, this adds to a disadvantage along with the complex layout structure.

(B) Driving Circuit Using Nand Based DCDL

Driving circuit can be used to generate the control-bits of the DCDL (Digitally Controlled Delay Lines). By analyzing, it can be noted that Si signals have to be delayed with respect to Ti signals and that it could be useful to have a different delay for LH (Low to High) and HL (High to Low) transitions. The existing DCDL (Digitally Controlled Delay Lines) uses dual edge triggered flip-flop as the driving circuit. This consumes more power. When this is adopted in the DLL (Digital Delay Lines)- this power consumption is also high.

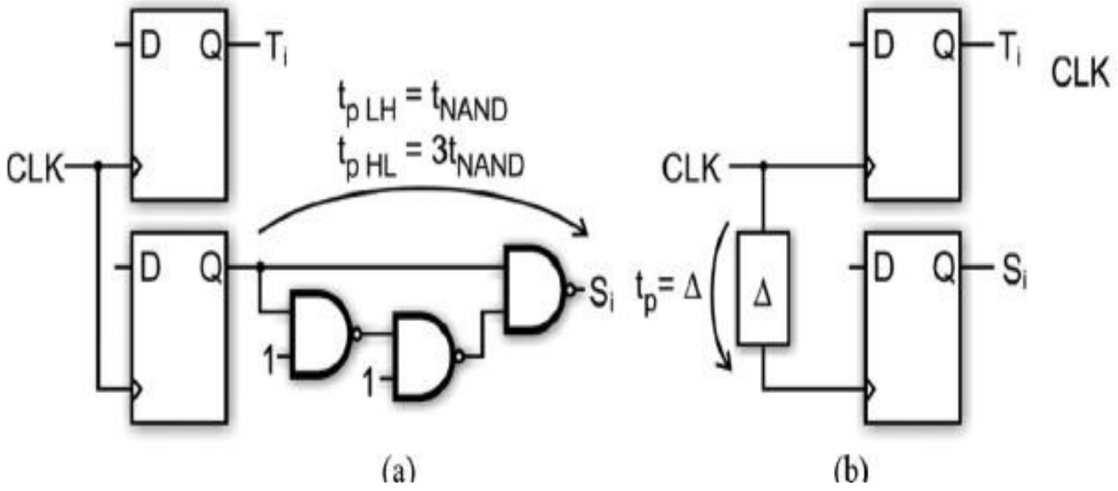

Figure 2: Driving circuits for control bits. (a) Si signal delayed with different LH/HL delays by using NAND based circuit. (b) Si signal delayed using clock tree delay.

3. PROPOSED STROBE SIGNAL MODULE

To glitch free module using strobe signal which overcomes the limitation of delay mismatch in a wide range of applications. The proposed strobe signal logic can control the occurrence of glitch at both the rising edge and falling edge of the circuit. The theoretical demonstration of the glitch free operation of the proposed strobe signal module is also derived in the paper [7]. The previously proposed digitally controlled delay lines (DCDL) has been compared to this technology. Simulation results show the correctness of the module with no delay mismatch with respect to the previously proposed DCDL (Digitally Controlled Delay Lines). As an example application, the strobe signal logic is used in configurable error free frequency detector (a frequency counter) which can control the occurrence of glitch during the sudden modulation of the frequency. The employ of the proposed strobe signal can hold the operation of the gate for a specific time until the other gate completes its operation so that there is no delay mismatch. DCDL (Digitally Controlled Delay Lines) is proposed to reduce power consumption [8-14].

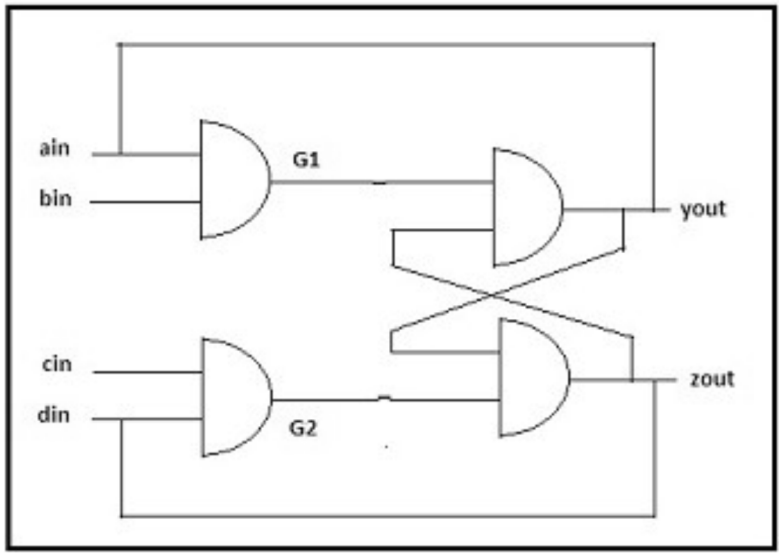

Figure 3: Strobe Signal Module

Waveform

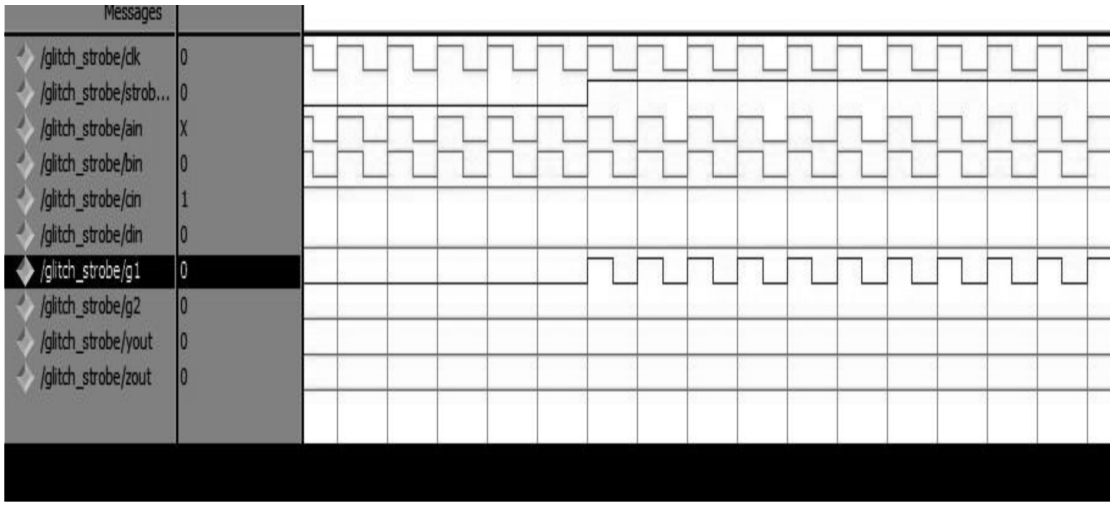

Figure 3.1: Simulation of Strobe Signal Module

When the strobe signal is 1, it will trigger the gate1 and hold the operation until the gate2 completes its operation and Zout is generated. When the strobe signal is 0, it will not trigger the gate.

4. CONFIGURABLE ERROR FREE FREQUENCY DETECTOR USING STROBE SIGNAL

Strobe have the property that either Data or Strobe can changes its logical values in one clock cycle, but never both. This allows for easy clock recovery with a good jitter tolerance by the two signal line values. There is an equivalent way to specify the relationship between Data and Strobe. For even-numbered Data bits, Strobe is the opposite of Data. For odd-numbered Data bits, Strobe is the same as Data. From this definition it is more obvious that the XOR of Data and Strobe will yield a clock signal. Also, it specifies the simplest means of generating the Strobe signal for a given Data stream. The reference signal has to be specified as it provides the range and the unknown signal is to be tested. Strobe control controls the operation of the gate for a specific period of time, so that there is no delay mismatch. It is used for both rising edge and falling edge of the clock.

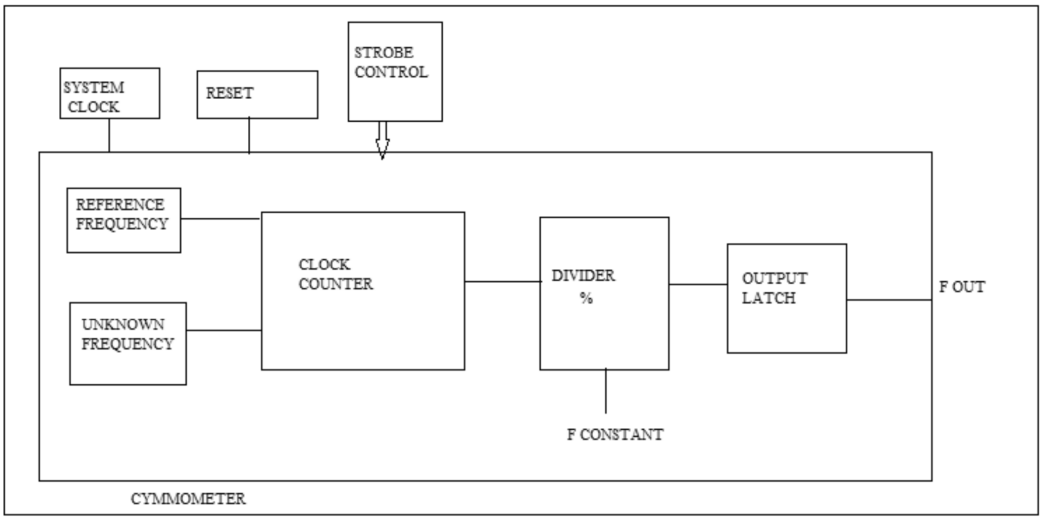

Figure 4: Configurable error free frequency detector

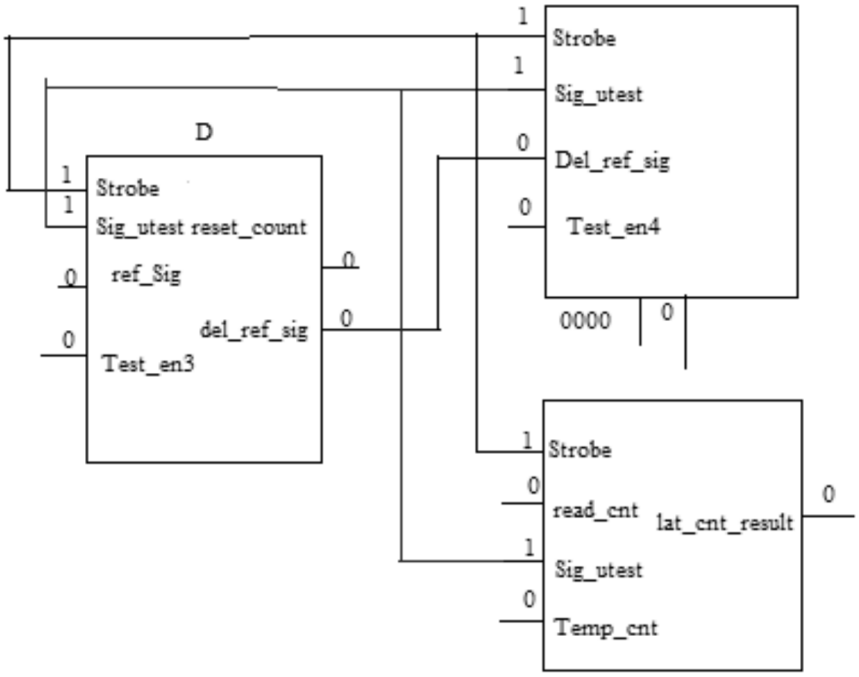

Figure 4.1: Data Flow Graph

Waveform

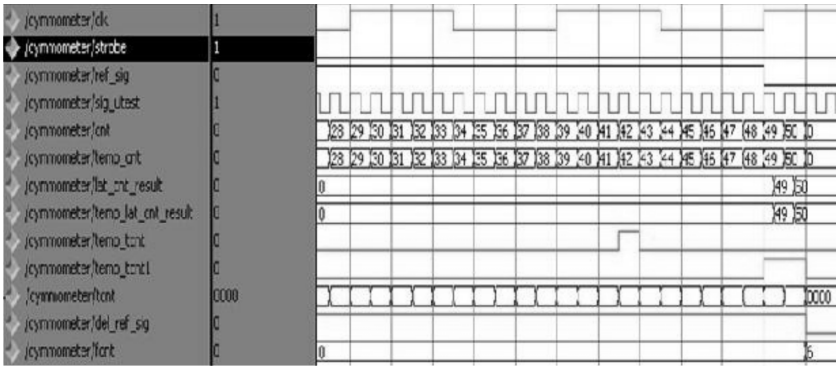

Figure 4.2: Simulation of Configurable of error free frequency detector

Table
Comparison of all the glitch removing approach

	Glitch	*INL*	*Powerdissipation*
Strobe Based[3]	no	0.8	0.77
NAND Based [2]	yes	0.7	0.92
TINV Based [4]	no	0.6	1.49
Mux Based [7]	no	0.3	1.33

5. CONCLUSION

A Strobe control module is presented which avoids the Glitching problem of previous circuits. A timing model of the Strobe structure implemented in the configurable error free frequency detector is developed to demonstrate the glitch free property of the proposed circuit. As an additional, the developed model also provides an explanation in order to guarantee a glitch free operation. The proposed Strobe signal logic can control the occurrence of glitch at both the rising and falling edge of the clock. The theoretical demonstration of the glitch free operation of the proposed Strobe signal module is also derived in the paper. Simulation results show that the correctness of the module with no delay mismatch compared to the previously proposed NAND based DCDL (Digitally Controlled Delay Lines).

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REFERENCES

[1] Davide De Caro, Senior member, IEEE, "Glitch free NAND based digitally controlled," *IEEE transactions on VLSI,* vol. 21, No. 1, January 2013.

[2] Arnold M. Frisch "Self Calibrating strobe signal generator", US Patent no US7219269, May, 2007.

[3] C.C Chung and C.Y.Lee,"An all digital phase locked loop for high speed clock generation" *IEEE j.Solid State Circuits*, vol. 38, no. 2, pp.347351, Feb 2003.

[4] F. Lin, J. Miller, A. Schoenfeld, M. Ma, and R. J. Baker, "A register controlled symmetrical DLL for double-data-rate DRAM," *IEEE J.Solid-State Circuits*, vol. 34,no. 4, pp. 565568, Apr. 1999.

[5] R. J. Yang and S. I. Liu, "A 40550 MHz harmonic-free all digital delay locked loop using a variable SAR algorithm," IEEE J. Solid- State Circuits, vol. 42, no. 2, pp. 361373, Feb. 2007.

[6] K. H. Choi, J. B. Shin, J. Y. Sim, and H. J. Park, "An interpolating digitally controlledoscillator for a wide range all digital PLL," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 9, pp. 20552063, Sep. 2009.

[7] Narendra Anand, Sung-Ju Lee, Edward W. Knightly,"Strobe:Actively securing wire-less communications using zero forcing beam forming".

[8] S. Karvonen, T. Riley, and J. Kostamovaara, "A low noise quadrature subsampling mixer," in *Proc. IEEE Int. Symp. Circuits and Systems*, 2001, pp. 790–793.

[9] S. Lindfors, A. Parssinen, and K. A. Halonen, "A 3-V 230-MHz CMOS decimation subsampler," *IEEE Trans. Circuits Syst. II*, vol. 50, pp. 105–117, Mar. 2003.

[10] G. T. Uehara and P. R. Grey, "Parallelism in analog and digital PRML magnetic disk read channel equalizers," *IEEE Trans. Magn.*, vol. 31, pp. 1174–1179, Mar. 1995.

[11] K. Muhammad, R. B. Staszewski, and C.-M. Hung, "Joint common mode voltage and differential offset voltage control scheme in a low-IF receiver," in *Proc. IEEE Radio Frequency Integrated Circuits (RFIC) Symp.*, June 2004, pp. 405–408.

[12] G. Gomez and B. Haroun, "A 1.5 V 2.4/2.9 mW 79/50 dB DR modulator for GSM/WCDMAin a 0.13 m digital process," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2002, pp. 242–243.

[13] J. Koh, K. Muhammad, B. Staszewski, G. Gomez, and B. Horoun, "A sigma-delta ADC with a built-in anti-aliasing filter for Bluetooth receiver in 130 nm digital process," presented at the IEEE Custom Integrated Circuits Conf., Oct. 2004, 25-6.

[14] P. T. M. van Zeijl *et al.*, "A Bluetooth radio in 0.18 _m CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2002, pp. 86–87.