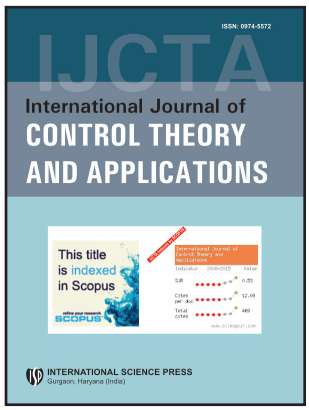

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Three Phase Four Wire PV-UPQC with Reduced DC Link Voltage for Power Quality Enhancement

T.M. Thamizh Thentral[a], B. Nikhil[b], and R. Jegatheesan[c]

[a]*Assistant Professor, Department of Electrical and Electronics Engineering, SRM University, India-603203. Email: thamizhthentral.t@ktr.srmuniv.ac.in*
[b]*M.Tech, Department of Power Electronics and Drives, SRM University, India-603203*
[c]*Professor, Department of Electrical and Electronics Engineering, SRM University, India-603203*

Abstract: The incorporation of PV array to Unified Power Quality Conditioner (UPQC), a custom power device to compensate unbalances in source voltage and to eliminate harmonic currents is dealt in this paper. This PV array will help to improve the duration of voltage compensation. Further dc link voltage rating of UPQC is also reduced without degrading its compensating ability. In this topology, a capacitor in series with the interfacing inductor of the shunt active filter is used and the system neutral is connected to the negative terminal of the dc-link voltage which avoids the necessity of the fourth leg in the Voltage Source Inverter (VSI) of the shunt active filter. The average switching frequency of the switches present in series and shunt Active Power Filter (APF) has been considerably reduced, resulting in making the system less bulky. A three phase four wire system is employed so as to give additional flexibility to the VSI to operate independently. A dynamic model of the proposed model has to be implemented using MATLAB domain, and corresponding results demonstrating the enhancement of power quality are`` shown.

Index Terms/keywords: PV array, unified power quality conditioner voltage source inverter, active power filter, dc link voltage, non-linear load, power quality.

1. INTRODUCTION

In the present day scenario with the advent of power electronics and digital control technology the density of non-linear loads connected to the grid has been increasing enormously. These non-linear loads cause source voltage distortions such as voltage sag, voltage swell, entry of current harmonics into the system and also lead to Power Quality (PQ) problems [1]. There are several methods which have been adopted to compensate these voltage unbalances and to eliminate the current harmonics. Initially, passive filters have been used to compensate the issues caused by the non-linear loads. However, these passive filters cannot be applied in wide range variations and also the size of the system is bulky and costly. Further, the incorporation of passive filters leads to resonance. These filters can deal only with limited power quality issues. Present day power electronic devices which are connected in series or shunt or both for enhancement of power quality and for improvement

the reliability of the supply systems include devices called custom power devices. These custom power devices include Dynamic Voltage Restorer (DVR), Distribution Static Compensator (D-STATCOM), and Unified Power Quality Conditioner (UPQC). The compensating device that is connected in shunt to the grid is termed asD-SATCOM [2]. The main reason behind connecting the compensating device in shunt to the system is to provide harmonic isolation between the load and the source, to provide load VAR compensation, to operate nearly at unity power factor and to balance the source current even if the load is unbalanced. The compensating device that has been connected in series to the supply system can be technically termed as DVR. The main purpose of incorporating a DVR in the grid is to compensate the voltage unbalances such as voltage sag, swell and voltage distortion. The combination of both these series and shunt compensating devices i.e.., DVR and D-STATCOM results in UPQC, useful to compensate the current quality issues like harmonics, reactive power unbalances and source voltage quality issues like sag, swell, interruptions, and unbalances thus improving the overall reliability of the system.

DC-link voltage rating of the capacitor greatly influences the performance of the Active Power Filter (APF). Generally, the voltage required for the shunt active power filter is more when compared to the voltage required for the series active power filter. Incorporating a common dc link voltage for both series and shunt active power filters leads to additional stress on the switches of the series APF thereby making the series APF bulky. The dc link voltage value should be greater than or equal to $\sqrt{6}$ times the phase voltage of the system. When dc link voltage is less than this value, the performance of the APF gets affected. The basic condition for Volt Ampere Reactive Power (VAR) compensation is the magnitude of reference voltage i.e.., reference dc-bus capacitor voltage should be higher than the voltage at the point of common coupling (PCC).

In general, the dc-link voltage required for the series APF and shunt APF is not the same. The shunt APF requires a higher value of dc link voltage compared to the dc-link voltage requirement of the series APF. As two separate dc-link voltages cannot be organized for a single UPQC topology, a considerable value of dc link voltage will be taken to both the active power filters in common. However, this will result in the increase of voltage stress on the switches of the series active power filter which leads to a bulky series APF. A three-phase four wire system has several advantages when compared with a three phase three-wire system. When a three-phase four wire system is employed, neutral clamped topology is used so that independent control of each leg of series and shunt APF is enabled. Also, a T-connected transformer enables the scope for avoiding the four-leg topology of the shunt active power filter. In this paper PV array is incorporated to the UPQC so that the duration of load voltage compensation can be improved. Also by adopting the proposed topology, the dc link voltage rating can be sufficiently reduced. The proposed topology consists of a combined system of PV array and UPQC.

2. CONVENTIONAL AND PROPOSED UPQC TOPOLOGIES

The conventional and proposed topologies of UPQC have been discussed here. The Figure shows the conventional UPQC topology employing three phase four wire system with neutral clamped topology. As the neutral clamped topology have been employed independent operation of each leg is attained [3-6]. Also, the switch count is reduced when compared to the pre-existing four leg topologies where eight switches are used [7]. In the Figure shown v_{as}, v_{bs}, v_{cs} represent the source voltages of respective phases a, b, c. Similarly, v_{al}, v_{bl}, v_{cl} are the corresponding voltages at the load side. The voltages v_{ase}, $v_{bse,}$ v_{cse} are the voltages injected by the series active power filter. Three phase currents from the source side are represented by i_{as}, i_{bs}, i_{cs}. Three phase currents drawn by the loads are represented by i_{al}, i_{bl}, i_{cl}. The currents from the shunt active power filter are denoted as i_{ash}, i_{bsh}, i_{csh} and i_n represents the neutral current flowing in the circuit. The PCC is a point in the electrical system where multiple consumer loads or multiple electrical loads can be connected. At this point a linear load comprising of series RL branch and a non-linear load comprising of a three leg diode bridge is connected. The interfacing inductance and resistance are of the shunt active power filter are represented by L_{sh}, $R_{sh.}$ The filter capacitance and interfacing

inductance of the series active power filter are denoted as c_{se}, L_{se}. The dc link capacitors and the voltages across them are denoted as $C_1 = C_2 = C_{dc}$ and $V_1 = V_2 = V_{dc}$.

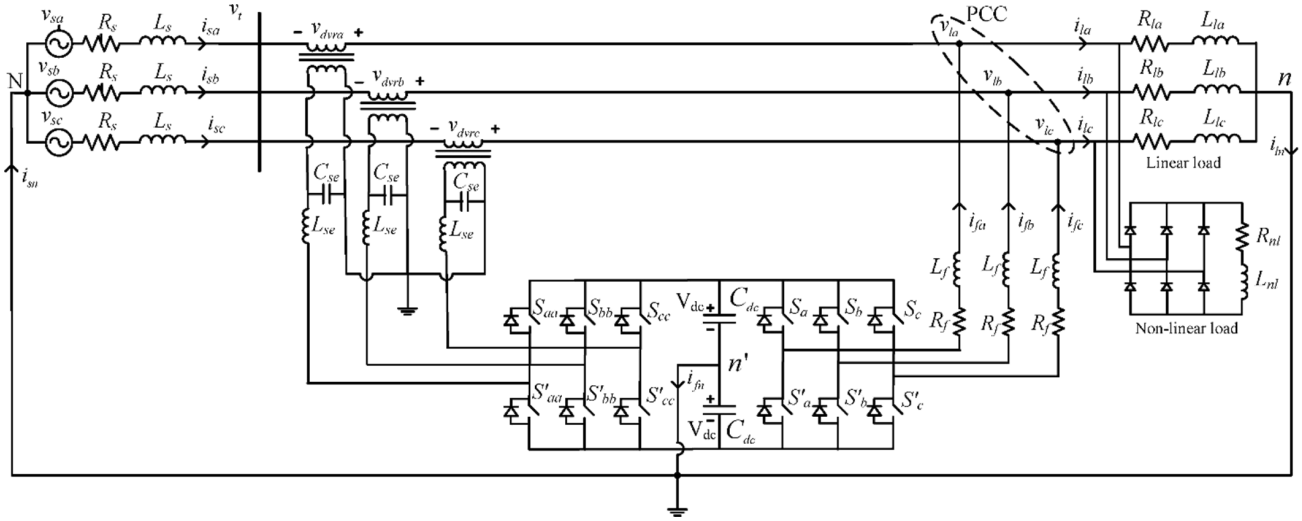

Figure 1: Unified power quality conditioner conventional topology

Figure 2 represents the proposed UPQC topology. The proposed PV-UPQC system consists of two voltage source inverters, a common dc link capacitor acting as source and a PV array. A number of PV modules are connected in series to form a PV array. Hence, the shunt APF converts PV generated energy to grid as well as eliminates current harmonics [8]. The series APF deals with the compensation of voltage unbalances. Compared to the conventional UPQC topology, the proposed UPQC topology uses an optimal value of the dc link voltage. The conventional topology uses a common value of dc link voltage for both the series and shunt active filters. The series APF consists of T-connected injection transformer connected in series with the line for injecting the required compensation voltage during voltage unbalances. This voltage is generated by the three leg series inverter connected across the dc link. The shunt APF injects current at the point of common coupling through inductor filter to mitigate the current harmonics and to maintain a constant voltage across the dc-link.

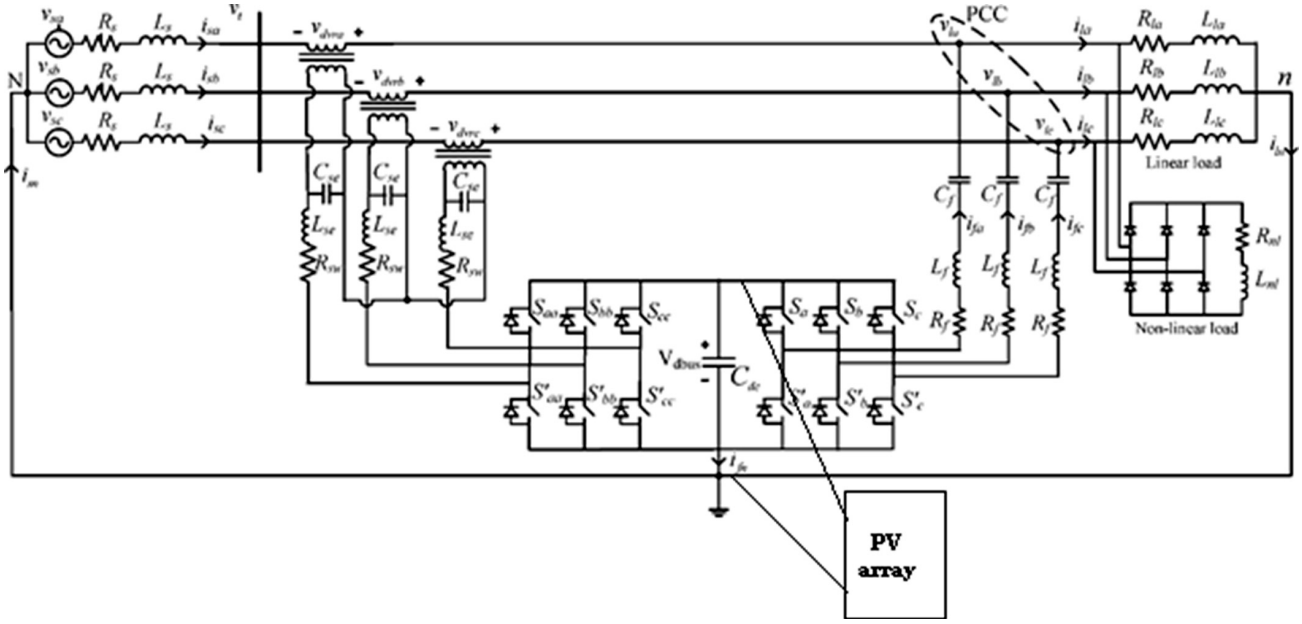

Figure 2: Circuit diagram of proposed PV-UPQC topology

3. DESIGN OF UPQC PARAMETERS

I. Shunt AFP Parameters

Let an X kVA system connects the APF which has a capability to operate in a marginal range of (0.5-2)X kVA under transient conditions for *n* cycles. Differential energy across C_{dc} is given by

$$\Delta E_c = \frac{C_{dc}[(1.123\,V_{dc})^2 - (0.875\,V_{dc})^2}{2} \tag{1}$$

The change in system energy is given as

$$\Delta E_s = \left(2X - \frac{X}{2}\right) nT \tag{2}$$

On solving equations (1) and (2) C_{dc} value can be obtained. The dc link capacitor is given by

$$C_{dc} = \frac{2\left(2X - \frac{X}{2}\right) nT}{(1.125\,V_{dc})^2 - (0.875\,V_{dc})^2} \tag{3}$$

II. Series APF parameters

For making the series APF a first order system, a series resistor referred as switching band resistor (R_{sw}) is added.

The DVR voltage and current of the capacitor are given by

$$V_{dvr} = \sqrt{V_{\text{ref}}^2 + V_{sw}^2} \tag{4}$$

$$V_{dvr} = \sqrt{I_{se1}^2 + I_{sw}^2} \tag{5}$$

$$V_{dvr} = I_{sw}R_{sw} = \frac{h_2}{\sqrt{3}} \tag{6}$$

$$V_{\text{ref1}} = I_{se1}X_{se1} \tag{7}$$

4. SYSTEM PARAMETERS

Table 1
System parameters

System parameters	*Experimental values*
System voltages	230 V (line to neutral), 50 cycles/sec
Feeder impedance	$R_s = 1\ \Omega$; $L_s = 10$ mH
Non-linear load	3-ϕ full bridge R-L load 150 Ω and 300 mH
Shunt APF parameters	$C_{dc} = 2200\ \mu F$, $L_f = 26$ mH, $R_f = 1\ \Omega$
Series APF parameters	$C_{se} = 80\ \mu F$, $L_{se} = 5$ mH and $R_{sw} = 1.5\ \Omega$
Injection transformer rating	1:1, 100 V and 700 V
PI controller gains	$k_p = 6$, $k_i = 5.5$
Hysteresis band parameters	$h_1 = \pm 0.5$ A, $h_2 = \pm 6.9$ V

The value of the shunt filter capacitor (C_f) can be calculated from the equation

$$\frac{V_{l1}X_l}{R_l^2+X_l^2}=\frac{V_{inv1}-V_{l1}}{(X_{lf}-X_{cf})^2}(X_{1f}-X_{cf}) \tag{8}$$

Fundamental component of series inverter voltage regarding dc link voltage is given below

$$V_{inv1}=\frac{0.612\,V_{dc}}{2\sqrt{3}} \tag{9}$$

5. REFERENCE COMPENSATOR CURRENTS UNDER UNBALANCED AND DISTORTED VOLTAGES

In this proposed topology the load currents are unbalanced and distorted initially because of the presence of the non-linear load. These currents flow through the feeder impedance and make the voltage at the terminal unbalanced and distorted. The series active filter makes the voltages balanced and sinusoidal at the point of common coupling. If the terminal voltages are used for generating the shunt filter current references, the shunting algorithm greatly affects the compensation performance. To overcome this limitation fundamental positive sequence voltages from PCC voltages are extracted. These positive sequence voltages are used in the control algorithm

$$\left.\begin{aligned} i_{af}^{*}&=i_{al}-i_{as}=i_{al}-\frac{v_{al1}+\gamma(v_{bl1}-v_{cl1})}{\Delta_1}(P_{lavg}+P_{loss})\\ i_{bf}^{*}&=i_{bl}-i_{bs}=i_{bl}-\frac{v_{bl1}+\gamma(v_{cl1}-v_{al1})}{\Delta_1}(P_{lavg}+P_{loss})\\ i_{cf}^{*}&=i_{cl}-i_{cs}=i_{cl}-\frac{v_{cl1}+\gamma(v_{al1}-v_{bl1})}{\Delta_1}(P_{lavg}+P_{loss}) \end{aligned}\right\} \tag{10}$$

where, $\Delta=\sum_{j=a,b,c}(v_{jl1})^2$, $\gamma=\tan(\phi/\sqrt{3})$ (11)

The above equations give balanced source currents after compensation irrespective of unbalanced and distorted supply. The reference voltages for series active filter are given

$$\begin{aligned} v_{dvri}^{*}&=v_{li}^{*}-v_{ti}\\ i&=a,b,c \end{aligned} \tag{12}$$

where, i_{af}^{*}, i_{bf}^{*}, i_{cf}^{*} are the reference compensator currents under unbalanced and distorted voltages.

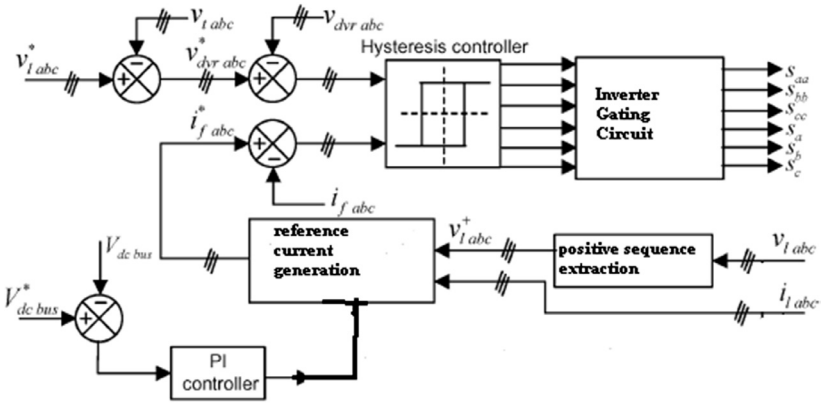

Figure 3: Control block diagram for UPQC

The switching commands for the VSI switches are generated from the hysteresis band current control method [11]. Hysteresis current controller is based on a feedback loop with two-level comparators. The switching commands are issued whenever the error limit exceeds a specified tolerance band "$\pm h$". The hysteresis controller has the advantages of peak current limiting capability, extremely good dynamic performance, and easiness in implementation and independence from load parameter variations. The major disadvantage of the hysteresis band controller is the converter switching frequency is highly dependent on the AC voltage and varies with it.

The switching control strategy for shunt active filter is done as follows

If $i_{af} \geq i_{af}^{*} + h_1$ bottom switch is turned ON and top switch is turned OFF

If $i_{af} \leq i_{af}^{*} - h_1$ then top switch is turned ON and the bottom switches are turned OFF

Similarly, the switching command for the series active filter is carried out as follows

If $v_{dvra} \geq v_{dvra}^{*} + h_2$ then bottom switch is turned ON and top switch is turned OFF

If $v_{dvra} \leq v_{dvra}^{*} - h_2$ then top switch is turned OFF and bottom switch is turned ON

6. SIMULATION CIRCUIT OF THE PROPOSED UPQC

A three-phase four-wire supply with a neutral clamped topology is connected to several non-linear loads such as DC motor, induction motor, three-leg diode bridge rectifier and three-leg RL-load. Series and shunt APF are triggered using hysteresis controller. The hysteresis controller senses unbalances in the source voltage and injects the required voltage in phase or out of phase. Corresponding output voltage and current waveforms are plotted.

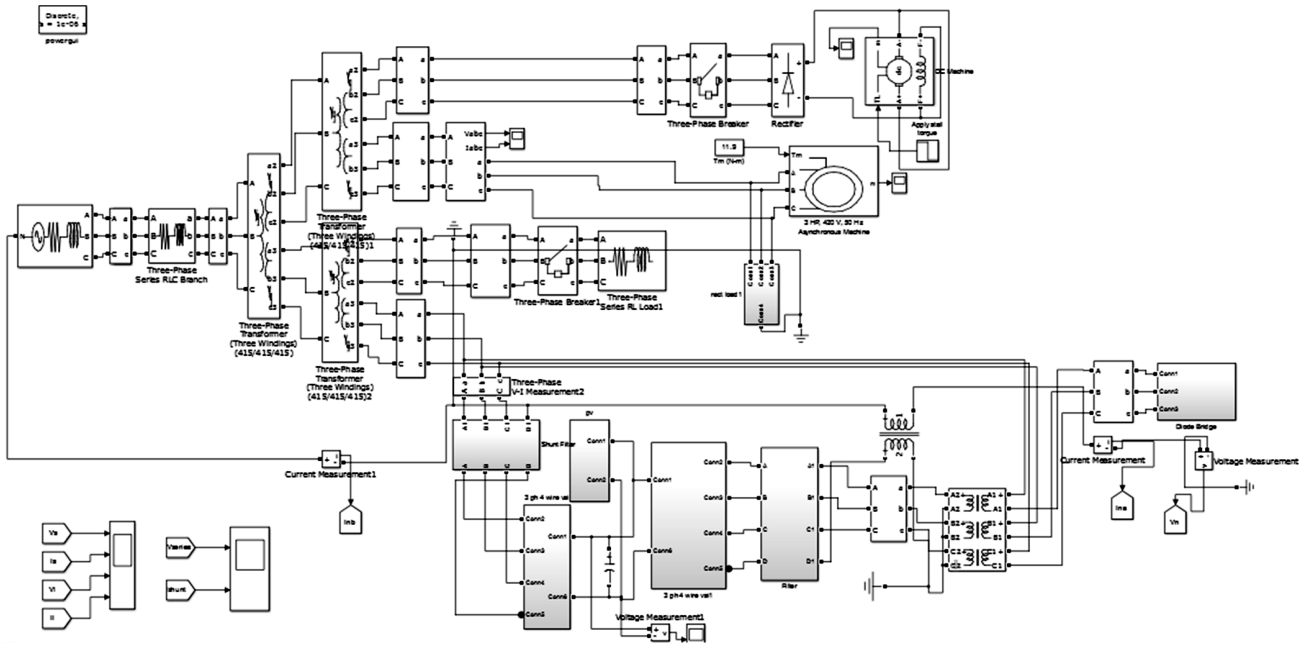

Figure 4: Simulation circuit of the proposed UPQC topology

The FigShows PV panels connected in series forming a PV module. Several PV modules are connected in series for forming a PV array. In this way the DC link voltage has been reduced from 1060v to 720v by following the modified topology.

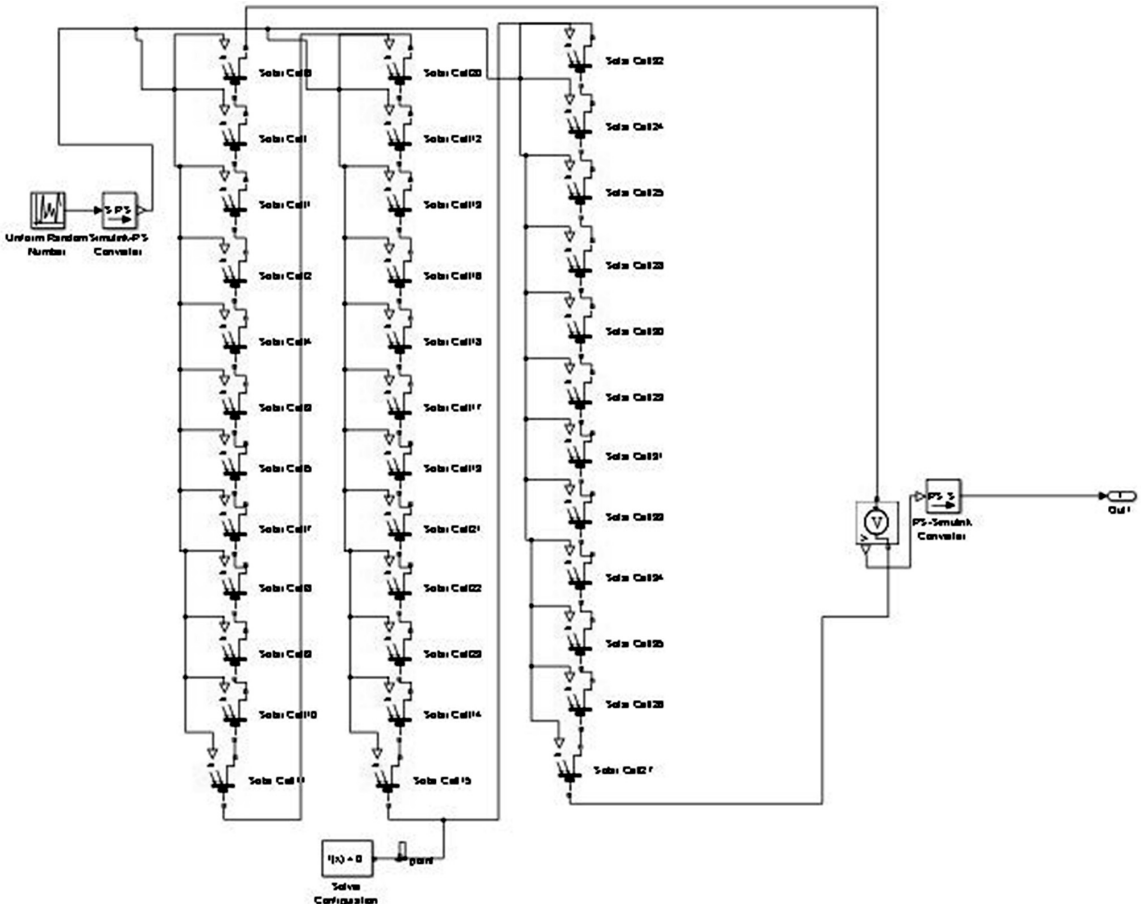

Figure 5: Simulation circuit of series connected PV panels

7. SIMULATION RESULTS

In the above Figure voltage unbalance occurred during the interval of 0.1 msec to 0.15 msec due to the sudden switching of the non-linear loads.

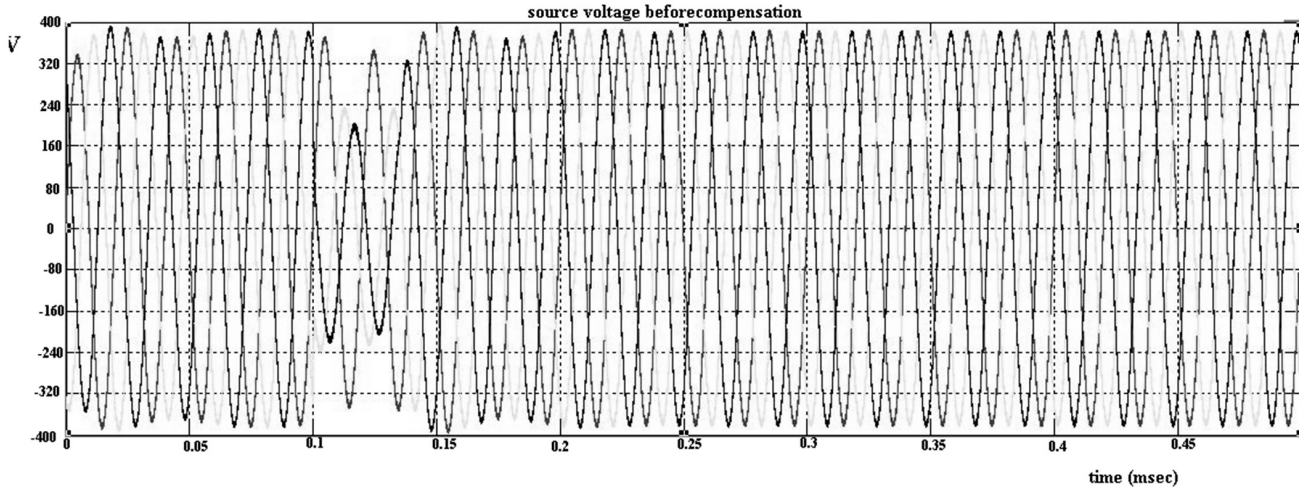

Figure 6: Shows source voltage waveform before compensation

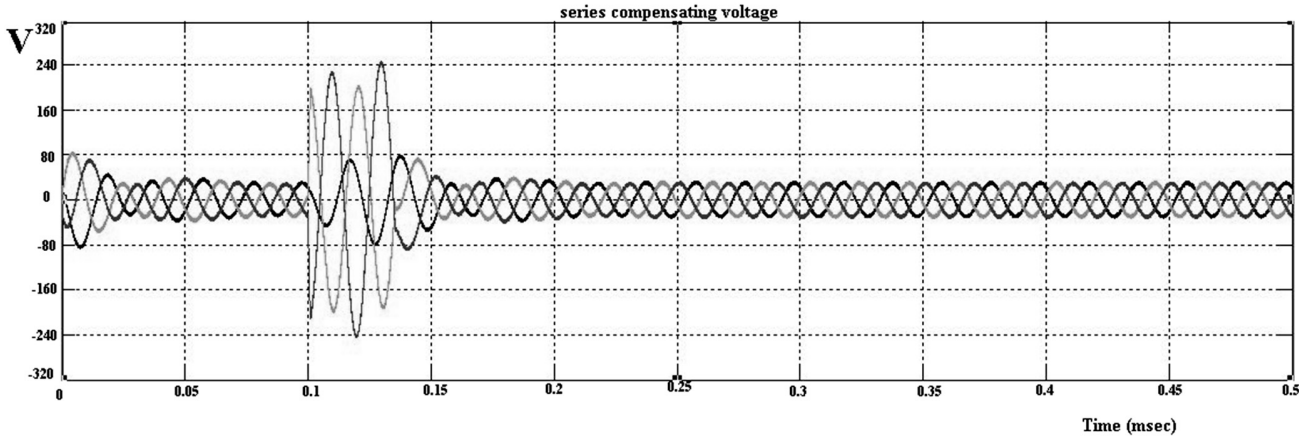

Figure 7: Shows series injecting voltage waveform

In the above Figure the required voltage for compensating the unbalanced voltages is injected during the interval of 0.1 msec to 0.15 msec.

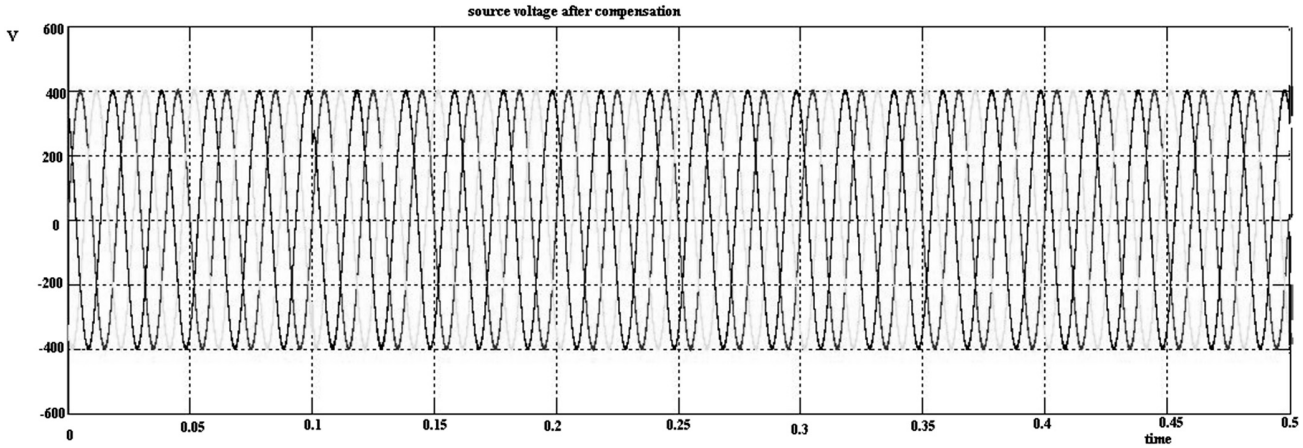

Figure 8: Shows the waveforms of compensated source voltage waveform

In the above Figure the source voltage after compensation is shown.

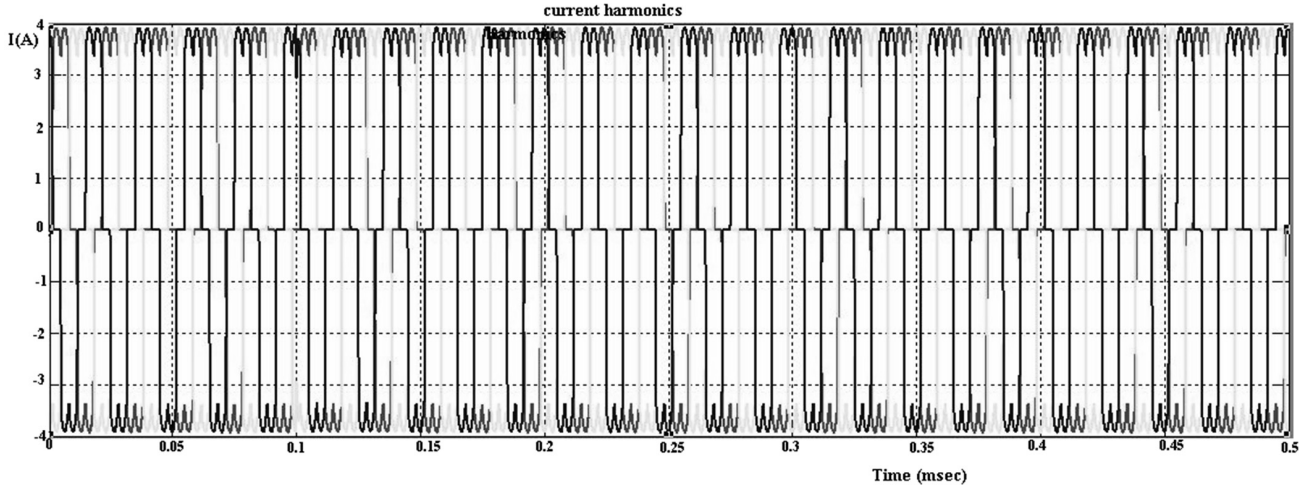

Figure 9: Harmonic currents waveform

In the above figure three-phase harmonic current waveforms are shown.

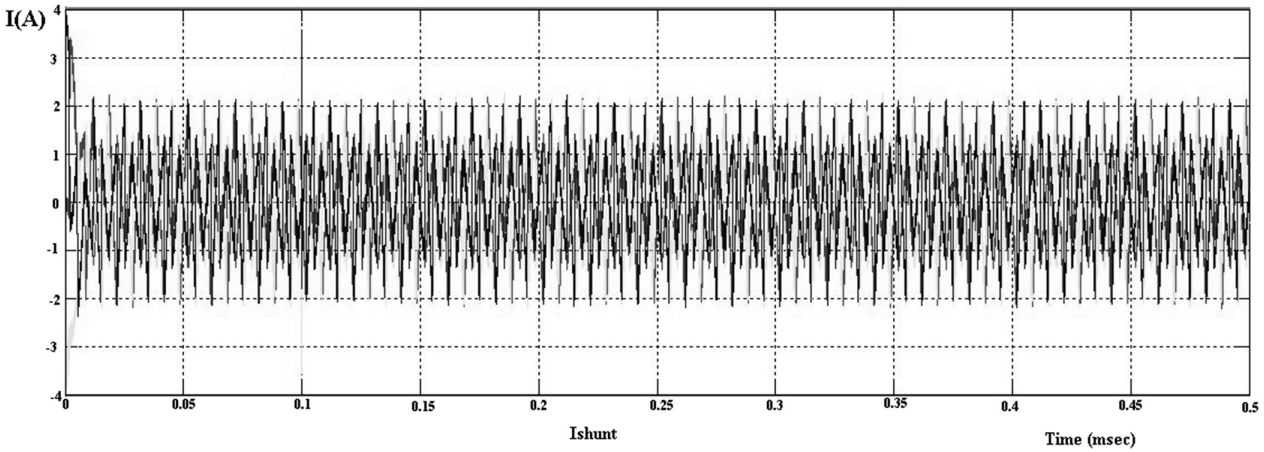

Figure 10: Shunt current waveform

In the above figure the shunt current from the shunt APF is shown

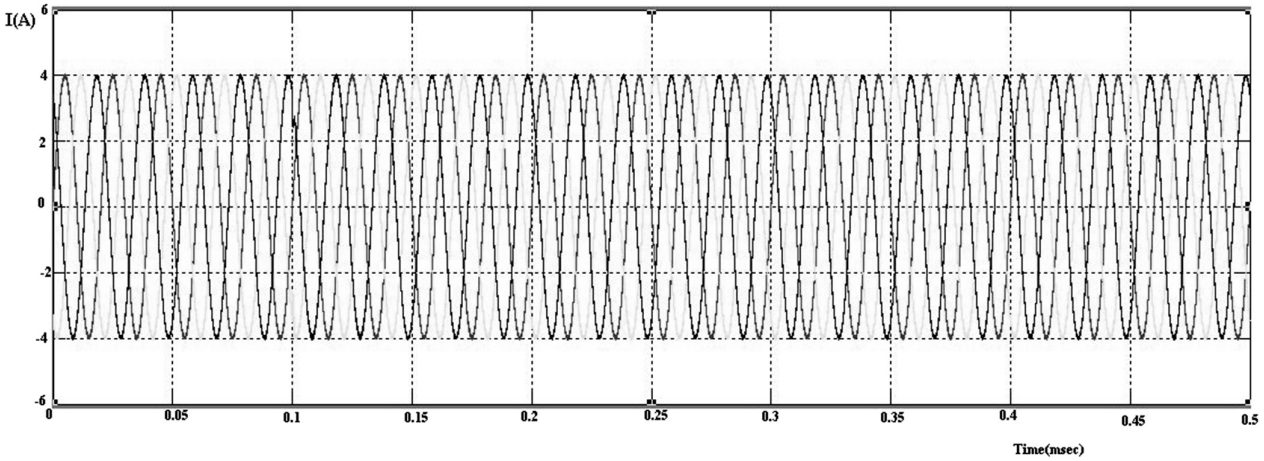

Figure 11: Source current waveform after the elimination of harmonics

In the above figure the source current free from harmonics is shown.

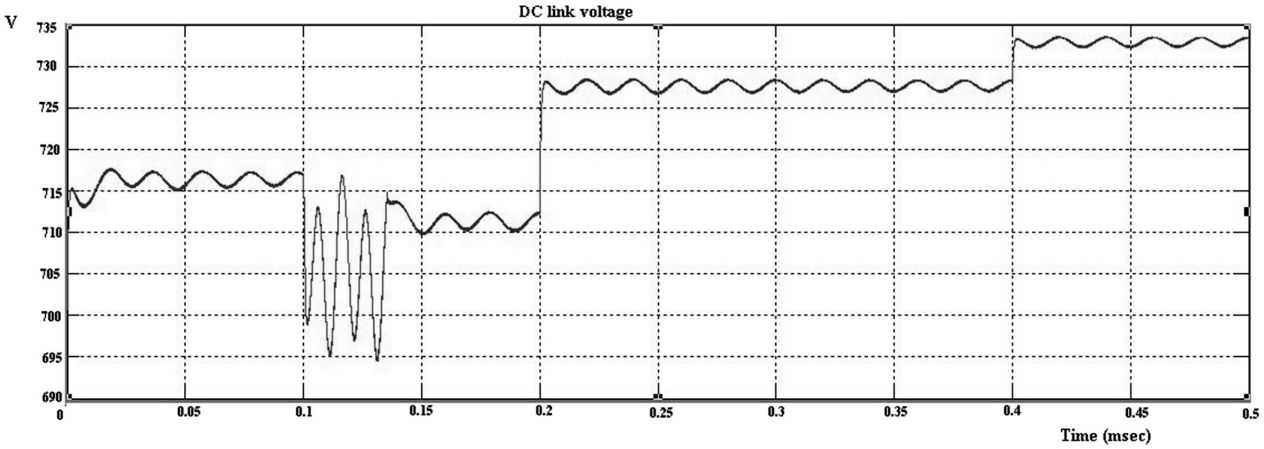

Figure 12: DC link voltage waveform

In the above Figure the reduced DC-link voltage rating is shown.

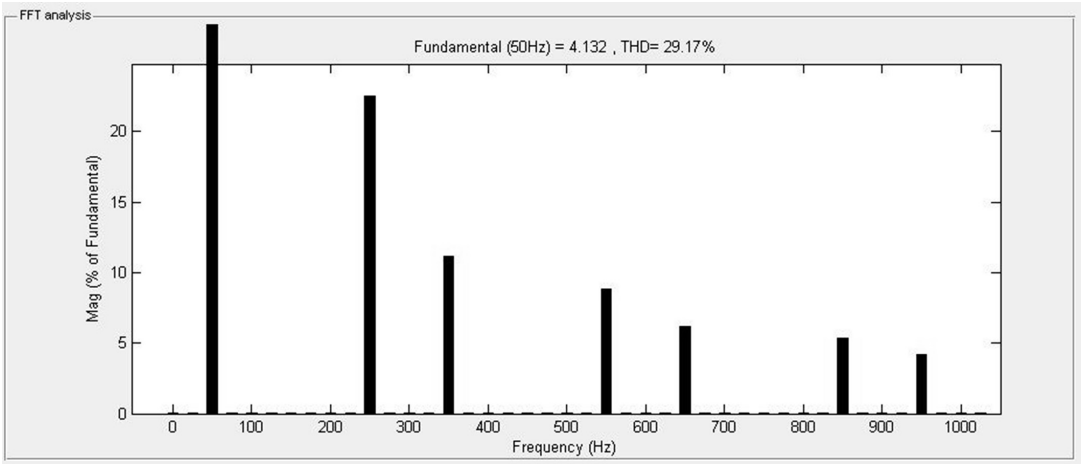

Figure 13: THD of current waveform before elimination of harmonics in load current

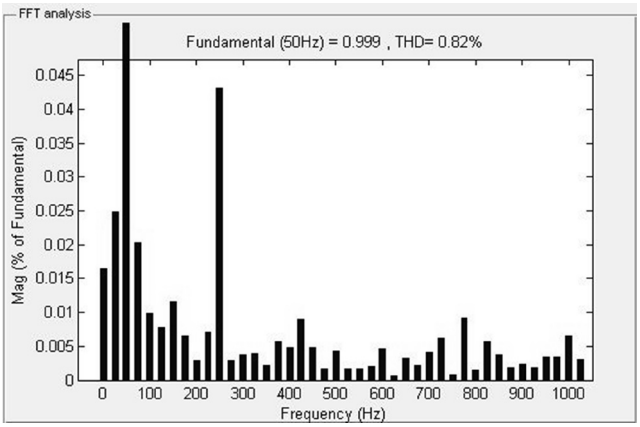

Figure 14: THD of current waveform after elimination of harmonics in load current

Figure 13 and 14 shows the total harmonic distortion of current waveforms before and after the elimination of harmonics.

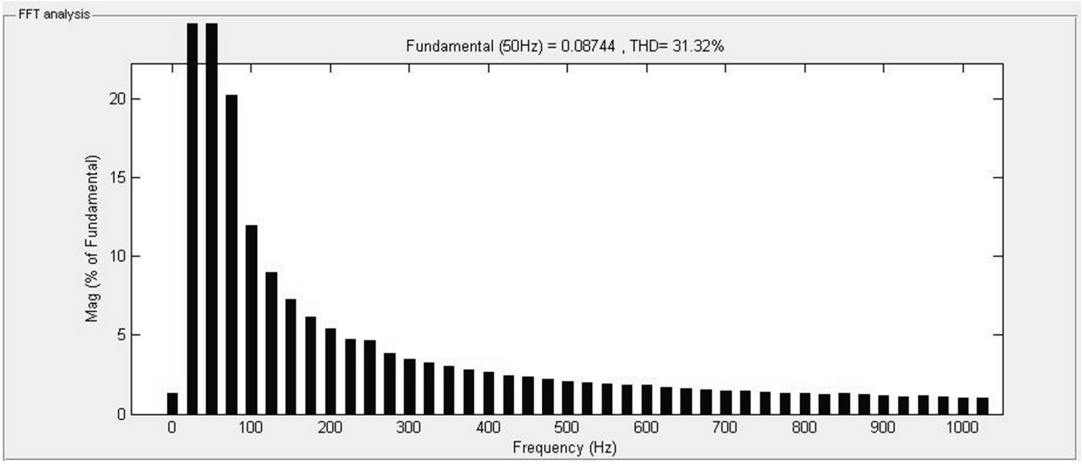

Figure 15: THD of voltage waveform before compensation of unbalances in source voltage

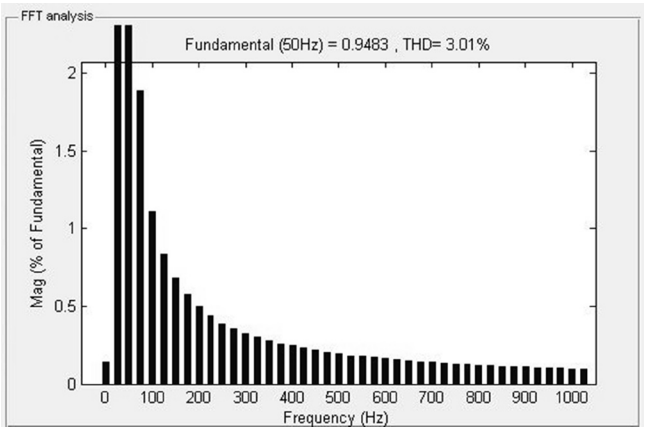

Figure 16: THD of voltage waveform after compensation of unbalances in source voltage

Figure 15 and 16 shows the total harmonic distortion of voltage waveforms before and after compensation of unbalances in source voltage.

8. CONCLUSION

In this paper, the proposed UPQC topology with PV integration is capable of compensating the deviations in source voltage at a lower rating of conventional UPQC topology. The designing of C_f, which avoids in maintaining a common value for dc link voltage for both series and shunt APF is discussed with the integration of PV array to the proposed UPQC system results in the improvement of the voltage unbalance compensation capability for a longer duration of time. A three-phase four -wire system with neutral clamped topology has been employed so that an independent operation of the active filters is achieved. Total harmonic distortion for source currents and load voltages are calculated and results are validated through Matlab Simulink.

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