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HARMONIC OPTIMIZATION AND OUTPUT ENHANCEMENT IN CASCADED MULTI-LEVEL INVERTER BY CONSIDERING MULTICARRIER PWM TECHNIQUE

Neelesh Yadav[*] and Viqar Yousuf[**]

Abstract: This paper presents different types of modulation techniques for cascaded MLI to reduce harmonics presence in output voltage of the inverter. The paper starts by generating multilevel inverter reference waveforms that are sinusoidal and triangular in nature. In this paper, different multicarrier PWM techniques have been used and at load side a low pass filter is also introduced to get less harmonic contents. This paper includes APOD technique along with SPWM and modified-SPWM technique. In this I'm proposing a new technique Modified PODPWM which gives less THD than PODPWM and magnitude is also more than that of PODPWM for keeping MI same. The all strategies have been confirmed by MATLAB simulation using a cascaded five-level inverter with different type of loads.

Key Words: PWM, SPWM, PODPWM, Modified-PODPWM, IGBT, THD.

1. INTRODUCTION

Quality of an output voltage (or current) waveform can be increase by decreasing in ripple content which is achieved by leveling in output voltage. To achieve this multilevel inverter is uses. MLI gives an output which have different number of voltage level so that power rating of the inverter can be increase. By increasing in level of voltage THD reduces and more output can be obtain. MLI can be classified as Diode-clamped MLI, Flying-capacitor MLIs, Cascaded MLI [3], [4].

In CMLI, desire output voltage synthesizes from several separate dc sources. Series connection of single-phase full bridge (H-bridge) makes a cascaded MLI. Each H-bridge contain a dc source. The cascaded inverter doesn't require any voltage balancing capacitors or voltage clamping diodes. Though this inverter uses separate input dc sources so it is well applicable for renewable source like fuel cell, biomass, photovoltaic etc. [5].

Cascaded H-Bridge (CHB) configuration has become more popular in adjustable-speed drive and high power application. For industrial application purpose three-phase CMLI is very useful because all three-phase drives like 3-phase induction machine, BLDC drive etc. can run from CMLI at high efficiency. A low Pass filter (LC) is used to eliminate higher order harmonics from output of the inverter [9].

[*] Department of Electrical and Electronics Engineering Lovely Professional University, Phagwara, Punjab, India
neeleshyadav12@gmail.com
[**] Department of Electrical and Electronics Engineering Lovely Professional University, Phagwara, Punjab, India
viqaryousuf@gmail.com

As increase in level of output harmonics reduces so that total harmonic distortion (THD) reduces. In three-phase 9-level (peak-to-peak) CMLI 48 semiconductor switches like GTOs, IGBTs and MOSFETs are uses. Each phase has 16 switches and 4 separate dc sources of same voltage.

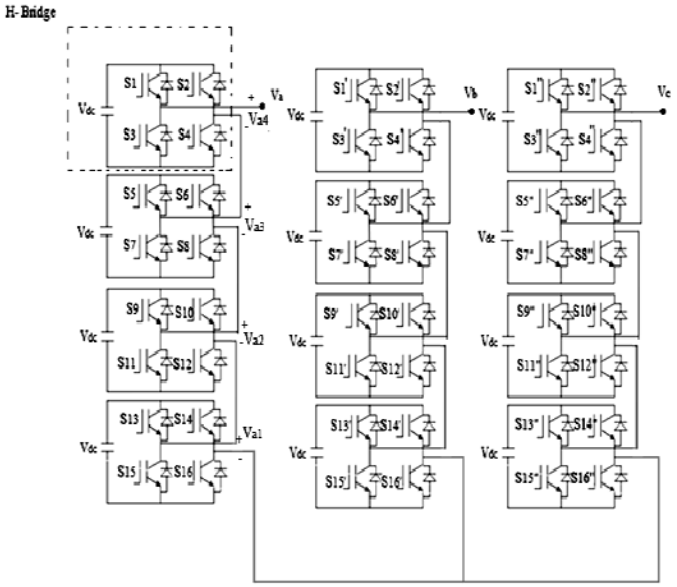

Figure 1. Single-phase five-level cascaded MLI

2. CONTROL STRATEGIES

In drive system or industrial purpose output of an inverter should be controllable so depending of application desire inverter can provide necessary magnitude of output. In practice different-different technique is uses to control output i.e. by

1. Regulate the output voltage of inverters,
2. Changing magnitude of input dc voltage, and
3. Vary the inverter gain

The most efficient method of controlling the output voltage and gain is PWM control within the inverters. In this method, a controllable output voltage is obtained by adjusting the period of turn on and turn off of the inverter switches which are semiconductors. By applying or removing the gate pulse to the semiconductor device, switching operation can achieve. This method is called *pulse-width-modulation* (PWM) control [1].

PWM technique are characterized by constant amplitude pulses. The width of these pulses is modulated to reduce harmonic content of the inverter output voltage. Different PWM techniques are:

Single-pulse-width modulation, Multiple-pulse-width modulation, Sinusoidal pulse-width modulation, Modified sinusoidal pulse-width modulation, Phase-displacement control, Space vector control etc. [2].

2.1 Multiple carrier pulse width modulation

This is a carrier-based implementation, in which more than one carrier signals are used to compare with reference signal to get multiple pulses. This process is known as multiple carrier PWM. In this, one sinusoidal wave as reference signal and more than one triangular wave as carrier signal is used [5].

Different strategies:

1. Phase Disposition PWM(PDPWM)
2. Phase Opposition Disposition PWM(PODPWM)
3. Alternate Phase Opposition Disposition PWM(APODPWM)
4. Phase Shift PWM

3. PHASE OPPOSITION DISPOSITION PWM TECHNIQUE (PODPWM)

In all of the disposition techniques PODPWM has advantages over the others. In this Total harmonic distortion becomes low and magnitude of the fundamental component increases. To get m-level of the output voltage waveform, (m-1) number of carrier signals is required. The signal sinusoidal waveform has peak-to-peak amplitude of V_r and f_r frequency. The multiple carrier signals (triangular wave) have same peak-to-peak magnitude V_c and f_c frequency.

In PODPWM technique the carrier signals, above the zero reference line are in the phase and below reference line the carrier signal also are in phase, but 180-degree phase shifted from those above zero.

During the comparison process, if the magnitude of the reference signal is greater than a carrier signal, then the pulse generates and corresponding semiconductor switch turned on. Otherwise the switched is turned off.

Modulation index (M_a) of PODPWM is given by

For m-level (peak-to-peak)

$$Ma = \frac{2Vr}{(m-1)Vc} \tag{1}$$

For example, m = 9

$$Ma = \frac{Vr}{4Vc}$$

Number of required carrier signals are (m-1) = (9-1) = 8.

Fig. 4.7 and 4.8 are shows the comparison process of PODPWM. These generated pulses are applied to 9-level CMLI so that harmonics can be reduces (nearly THD < 15%) and using normal LC filter THD get reduces (THD<13%) more magnitude of the output voltage is achieved.

By varying modulation index magnitude of output can get change so that we can control easily.

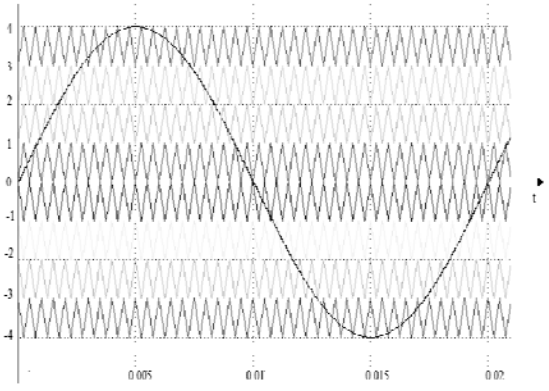

Figure 2: Carrier arrangement for PODPMW

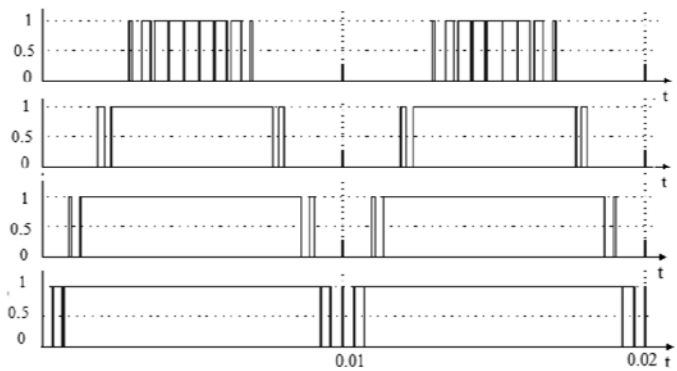

Figure 3: Gate signal for 9-level using PODPWM technique

4. MODIFIED PHASE OPPOSITION DISPOSITION PWM TECHNIQUE (MPODPWM)

This technique named as Modified PODPWM. It is an advance method which comprising PODPWM and Modified SPWM (60˚-SPWM) technique. In PODPWM all carrier wave has same magnitude and are in phase to each other. But in modified PODPWM upper carrier signal [*m*-1] and lower carrier [-(*m*-1)] signal have also same magnitude but for a certain time period magnitude becomes zero so that by comparing process a wide pulse width can get.

Though in SPWM the width of pulses near the peak value is nearly same so it can be treat as wide pulse.

By doing this, the magnitude of the output voltage can increase as well as THD is also becomes less than PODPWM or other technique. Figure 4 shows modified PODPWM technique.

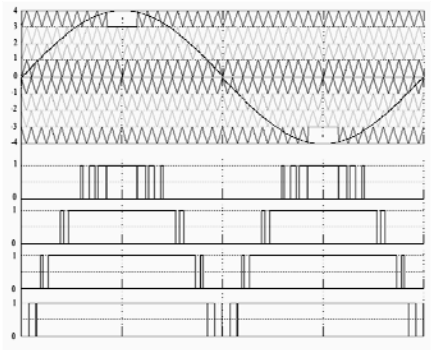

Figure 4. Modified PODPWM Result Using SPWM technique

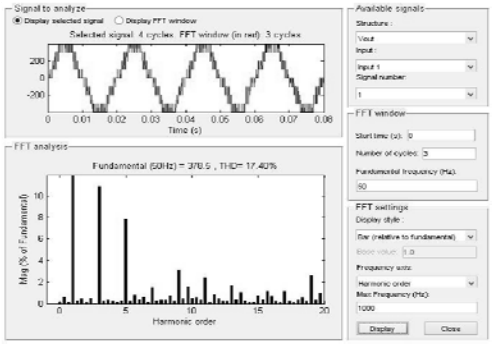

Figure 5. FFT plot of 9-level output voltage waveform of CMLI (without filter) [THD = 17.40%]

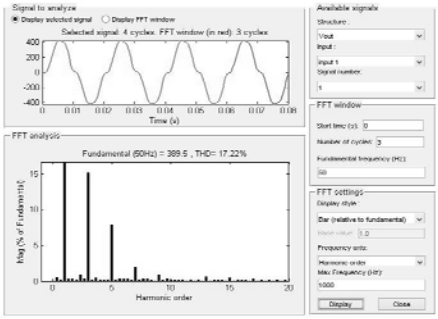

Figure 6. FFT plot of 9-level output voltage waveform of CMLI (with filter) [THD = 17.27%] Using PODPWM technique

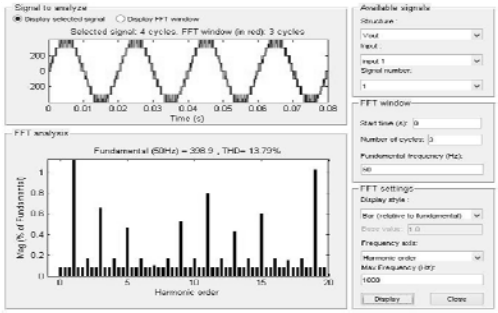

Figure 7. FFT plot of 9-level output voltage waveform of CMLI (without filter) [THD = 13.79%]

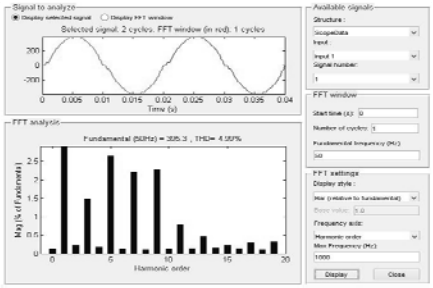

Figure 8. FFT plot of 9-level output voltage waveform of CMLI (with filter) [THD = 4.99%] Using MODIFIED PODPWM technique

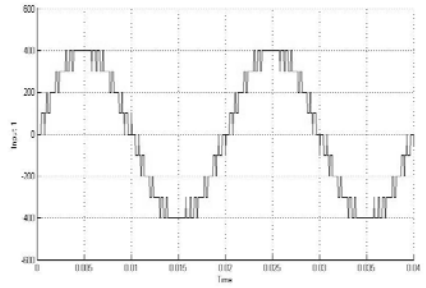

Figure 9. Simulated 9-level output voltage waveform of CMLI (without filter) using Modified PODPWM

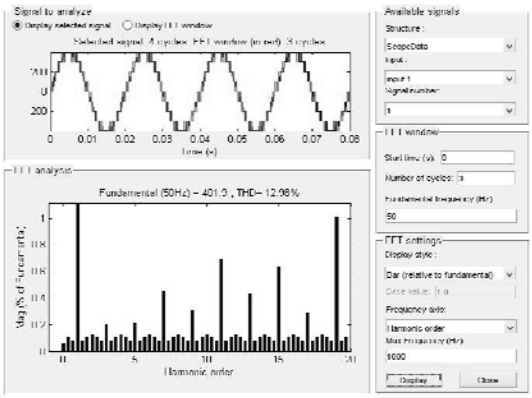

Figure 10. FFT plot of 9-level output voltage waveform of CMLI (without filter) [THD = 12.98%]

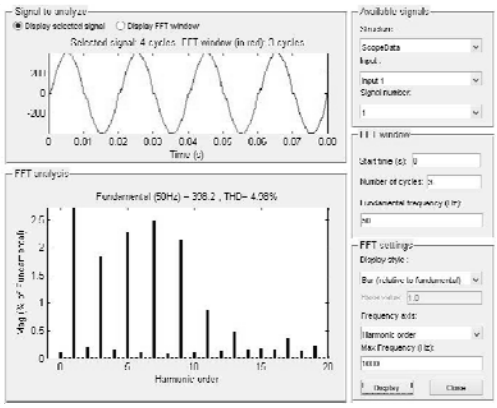

Figure 11. FFT plot of 9-level output voltage waveform of CMLI (with filter) [THD = 4.98%]

Comparison between all techniques is shown in Table 1. For different value of modulation index inverter gives different output and different THD. From all simulation it is clear that Modified-PODPWM technique gives less THD with greater fundamental component than other for same modulation index.

Table 1
Comparison between all techniques

Techniques	*Modulation Index (MI)*	*Without filter*		*With filter*	
		THD (%)	*V_{o1} (volts)*	*THD (%)*	*V_{o1} (volts)*
SPWM	0.9	17.40	378.5	16.52	380.3
	1	17.63	387.5	17.22	389.5
	1.1	17.98	390.6	17.36	392.28
PODPWM	0.9	16.94	356.6	5.59	358.2
	1	13.79	398.9	3.92	402.1
	1.1	11.83	424.8	3.93	429.5
Modified-PODPWM	0.9	15.47	371.5	7.52	373.3
	1	12.98	401.9	4.01	405.1
	1.1	11.76	424.8	429.5	3.97

5. CONCLUSION

The work done, started with study of literature. After studying about inverters and harmonic distortion, I have designed the three phase CMLI with different harmonic reduction techniques. Work done so far can be summarized in following points:

Three phase CMLI circuit was designed which contained H-Bridge circuits with star connected load.

Simple inverters have very THD levels and low fundamental output.

SPWM technique reduces the THD in the systems.

Phase opposition disposition PWM technique reduced more harmonics.

60 degree SPWM was used with the previous technique as modified technique, this reduced the level of harmonics more and the fundamental component was boosted up.

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