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Prediction of Trapezoidal Variable Amplitude PWM Techniques for Three Phase Trinary Source Nine Level Inverter

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ABSTRACT

This paper presents the functional analysis of various Bipolar Variable Amplitude Pulse Width Modulation (BVAPWM) techniques with Trapezoidal reference for three phase trinary source nine level cascaded inverter. Various new schemes adopting the constant switching frequency and also variable switching frequency multicarrier based on control freedom degree combination concepts are developed and simulated for the chosen three phase cascaded trinary source inverter using MATLAB-SIMULINK. In this paper, various bipolar variable amplitude PWM techniques such as PDPWM, PODPWM, APODPWM and COPWM using Trapezoidal reference are developed. The variation of fundamental RMS output voltage (V_{RMS}), total harmonic distortion (% THD) are observed and Distortion Factor (DF) of output voltage is calculated for various modulation indices ranging from 0.8- 1 and the results are tabulated, presented and analyzed. It is inferred that PODPWM technique provide minimum THD and COPWM technique provides higher fundamental V_{RMS} output voltage.

Keywords: CMLI, THD, BVAMCPWM, BVAPDPWM, BVAPODPWM, BVAAPODPWM, BVACOPWM, Trapezoidal PWM

1. INTRODUCTION

In progress years, a group of occupation has been done in expansion of trinary source inverters using BVAPWM techniques. Among the various topologies of trinary source inverters cascaded H-bridge inverter is preferred here. It is an effective solution for increasing the number of levels in output waveform with reduced DC sources and switching elements, thereby dramatically reduces harmonics without increasing the switching frequency. It has emerged as an important alternative in the area of high power and medium level voltage control. This paper focuses on cascaded H-bridge multilevel inverter using two unequal DC sources in order to produce a nine level output voltage.

Therefore, the overall cost and complexity are greatly reduced particularly for higher output voltage levels. This topology is able to increase the number of output voltage levels by using a lower number of power electronic devices such as switches, power diodes, driver circuits and DC voltage sources that lead to reduction in installation space and cost of the inverter. A great perfection in voltage levels with minimum switching devices has been obtained in asymmetric modes.

Balamurugan et al approached for advanced references and carriers based PWM in asymmetrical multilevel inverter and designed control techniques for various bipolar PWM strategies of three phase five level cascaded Inverter and evaluated the design of new multilevel inverter topology for various unipolar triangular carrier PWM strategies in [1, 2, 7]. Espinosa et al [3] introduced a new modulation method for a

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13-level asymmetric inverter toward minimum THD. Masaoud et al [4] predicted a new three-phase multilevel inverter with reduced number of power electronic components. Ataollah Mokhberdoran et al [5] carried out symmetric and asymmetric design and implementation of new cascaded multilevel inverter. Ebrahim Babaei et al [6] developed cascaded multilevel inverter with connection of novel H-bridge basic units. Josephine et al [8] presented PWM control for hybrid clamped multilevel inverters. Belkamel et al [9] proposed a novel three-phase asymmetrical cascaded multilevel Voltage Source Inverter. Prathiba et al [10] reveals the performance analysis of symmetrical and asymmetrical cascaded H-bridge inverter. PWM control for hybrid clamped multilevel inverters is developed in [11]. A generalized cascaded multilevel inverter using series connection of submultilevel inverters is discussed in [12].

Trapezoidal Inverted Sine PWM techniques for fundamental fortification in PV fed multilevel inverters were presented in [13]. Cascaded and hybrid multilevel inverters with reduced number of switches for induction motor is analysed and compared in [14]. A new topology of multilevel inverter is designed and implemented in [15]. A multilevel voltage source inverter topologies and control schemes are reviewed in [16]. A comparative study on carrier overlapping PWM strategies for five level Diode Clamped Inverter is performed in [17]. Multicarrier Trapezoidal PWM techniques based on Control Freedom Degree for MSM is proposed in [18].

Various modulation methods are available for trinary source inverter, but this paper emphasis on BVAPWM techniques with Trapezoidal reference as carrier. The performance evaluation of the proposed PWM techniques for three-phase trinary source inverter is done using MATLAB and Total Harmonic Distortion (%THD), fundamental RMS output voltage (V_{RMS}), is observed and Distortion Factor (DF) of output voltage is determined.

2. THREE PHASE NINE LEVEL TRINARY SOURCE CASCADED MULTILEVEL INVERTER

The fundamental H-bridge cascaded topology increases the number of components required, which in turn makes the design complexity and increases the cost. It is also to be establishing that the maximum output

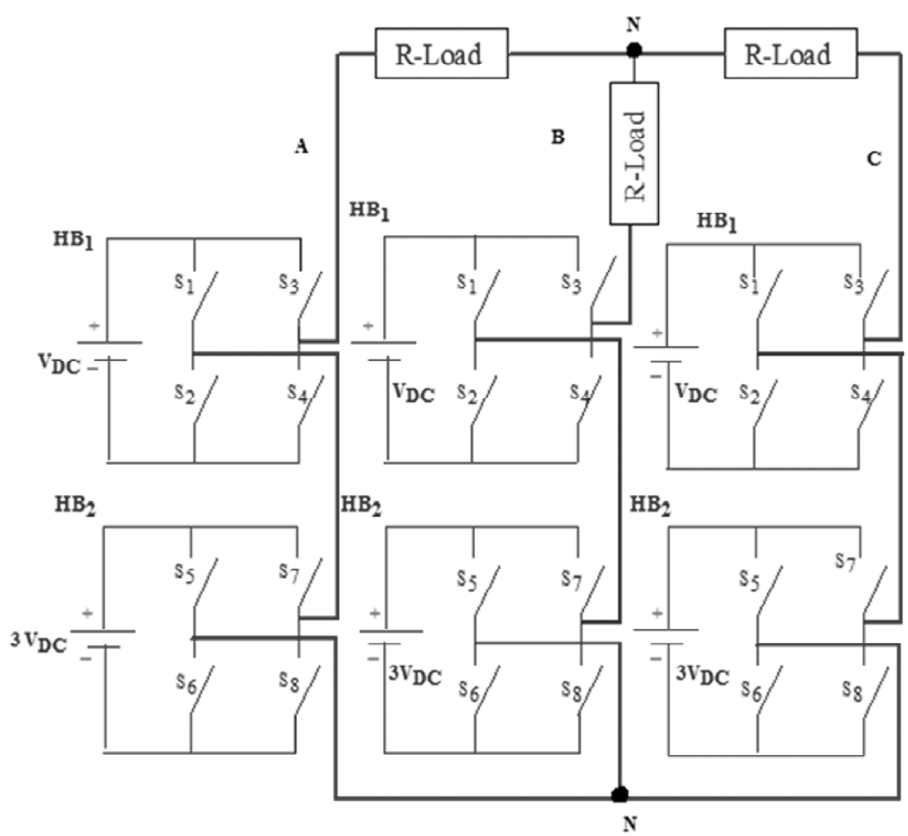

Figure 1: Three Phase Nine Level Trinary Source Cascaded Inverter

voltage cannot go beyond the sum of voltage of individual sources which becomes the most important setback of this topology. Because of the foresaid reason in an application which requires high output voltage from low voltage level, it needs H-bridge module in addition or step-up transformers. To overcome that a new topology proposed is shown in Fig. 1 to reduce the component count.

Fig. 1 shows the topology of the proposed three phase nine level cascaded trinary DC source multilevel inverter. It views like a conventional cascaded H-bridge multilevel inverter apart from input DC sources. The topology comprises of floating input DC sources connected through power switches. The structure requires lesser active switches as compared with conventional cascaded H-bridge topology with much reduced switching losses. By using V_{DC} and $3V_{DC}$, it can synthesize nine output levels; $-4V_{DC}$, $-3V_{DC}$, $-2V_{DC}$, $-V_{DC}$, 0, V_{DC}, $2V_{DC}$, $3V_{DC}$ and $4V_{DC}$. The lower inverter generates an elementary output voltage with three levels and then the upper inverter adds or subtracts one level from the fundamental wave to synthesize stepped waves. At this point, the final output voltage level becomes the sum of each terminal voltage of H-bridge [1] and it is given as

$$V_{out} = V_{HB1} + V_{HB2} \tag{1}$$

In the proposed circuit design, suppose the number of H-bridge component has self-governing DC sources in sequence of the power of 3, a predictable output voltage level is given as

$$V_n = 3^n,\ n = 1, 2, 3, \dots\dots\dots \tag{2}$$

where, n is number of H bridges.

Waveforms of output voltage are denoted as (V_{out}), upper terminal voltage is (V_{HB1}) and the lower voltage is (V_{HB2}) inverter in sequence.

The output voltage has nine levels include zero level. Though it is close to a sinusoidal wave, it has lower order harmonics. So it needs more H-bridge modules or output filter to obtain high quality output voltages. Advantage of the proposed multilevel inverter scheme is the elimination of transformer in the main power stage. However, each cell of the proposed multilevel inverter requires its own isolated power supply. The provision of these isolated supplies is the main limitation in the power electronic circuit design. So the proposed multilevel inverter is suitable for photovoltaic power generating systems equipped with distributed power sources.

3. BIPOLAR VARIABLE AMPLITUDE TRAPEZOIDAL PULSE WIDTH MODULATION TECHNIQUES

The most popular method of controlling the output voltage is by incorporating PWM control within the inverters. In this paper four different modulation techniques were tried in order to increase the output voltage and also to reduce the THD. It is generally recognized that, increasing the switching frequency of the PWM pattern results in reducing lower frequency harmonics. This paper includes reference waveform as trapezoidal and 8 triangular carriers. To synthesize multilevel output AC voltage using different levels of DC inputs, semiconductor devices must be switched ON and OFF in such a way that desired fundamental is obtained with minimum harmonic distortion. There are different types of approaches for the selection of switching techniques for the trinary source multilevel inverters.

Among all the PWM methods for trinary source cascaded inverter, carrier based PWM methods and space vector methods are often used but when the number of output levels is more than five, the space vector method will be very complicated with the increase of switching states. So the carrier based PWM strategy is preferred under this condition in trinary source inverters. This paper focuses on carrier based PWM techniques which have been extended for use in trinary inverter by using multiple carriers. Multicarrier based PWM techniques have more than one carrier that can be triangular waves or sawtooth waves and so on. The carrier waves can be either bipolar or unipolar. In this paper, a comprehensive analysis of the aforementioned topology is carried out using Bipolar Variable Amplitude PWM techniques. In this paper, various carrier arrangements like Phase Disposition PWM (PDPWM), Phase Opposition Disposition PWM (PODPWM), Alternative Phase Opposition Disposition PWM (APODPWM) and Carrier Overlapping PWM (COPWM) are used to generate switching pulses for three phase nine level trinary source cascaded inverter.

For an -level inverter using bipolar variable amplitude PWM technique, (m-1) carriers with same frequency f_c and variable peak-to-peak amplitude A_C are used. The reference waveform has amplitude A_m and frequency f_m are placed at zero reference for A-phase, -120 degree reference for B-phase and +120 degree reference for C-phase. The reference wave is continuously compared with each of the carrier signals. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched ON. Otherwise, the device switched OFF. In this paper, the frequency ratio m_f = 40 and modulation index m_a is varied from 0.8 to 1.

$$m_f = \frac{f_c}{f_m} \tag{3}$$

$$m_a = 2A_m / (m-1)Ac \quad \text{except for COPWM} \tag{4}$$

3.1. Bipolar Variable Amplitude Phase Disposition PWM Technique

The PDPWM technique employed in this work uses eight carriers with three modulating waveform. In this all the carriers are in phase and the carriers are disposed so that the bands they occupy are contiguous. The modulation wave is centered in the middle of the carrier set. Fig. 2 shows the carrier arrangement for PDPWM technique for ma = 0.9 and m_f = 40.

3.2. Bipolar Variable Amplitude Phase Opposition Disposition PWM Technique

In the PODPWM technique the carrier waveforms above the zero reference value are in phase. The carrier waveforms below zero are also in phase but are 180° phase shifted from those above zero. Fig. 3 shows the carrier arrangement for PODPWM method for ma = 0.9 and m_f = 40.

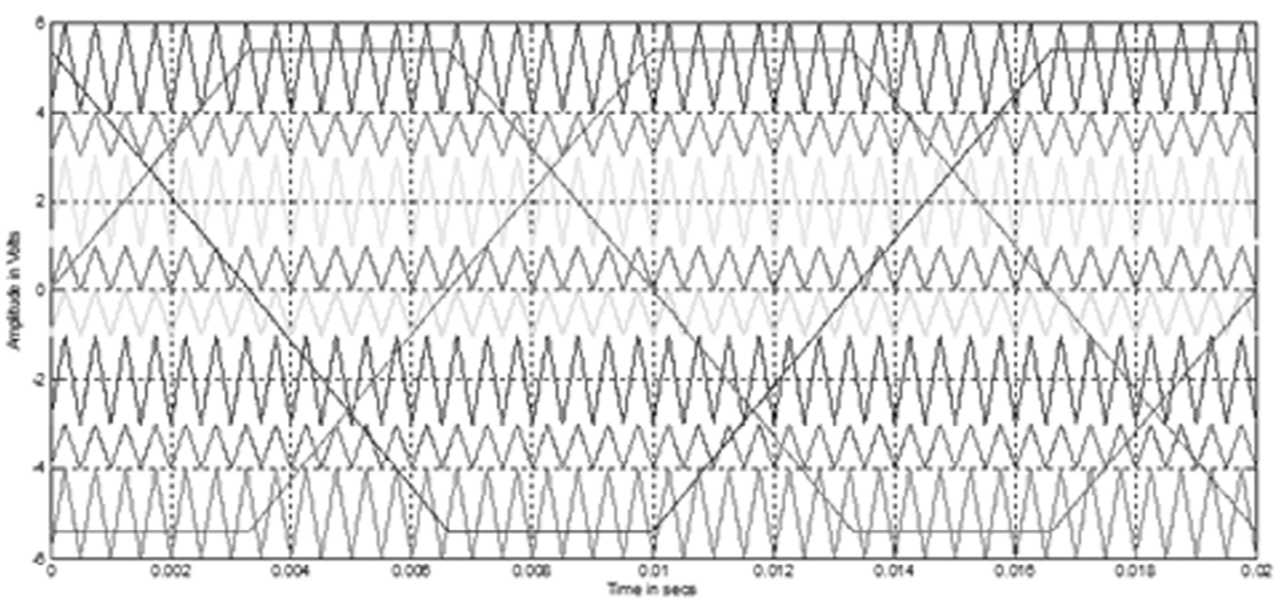

Figure 2: Carrier arrangement for PDPWM technique

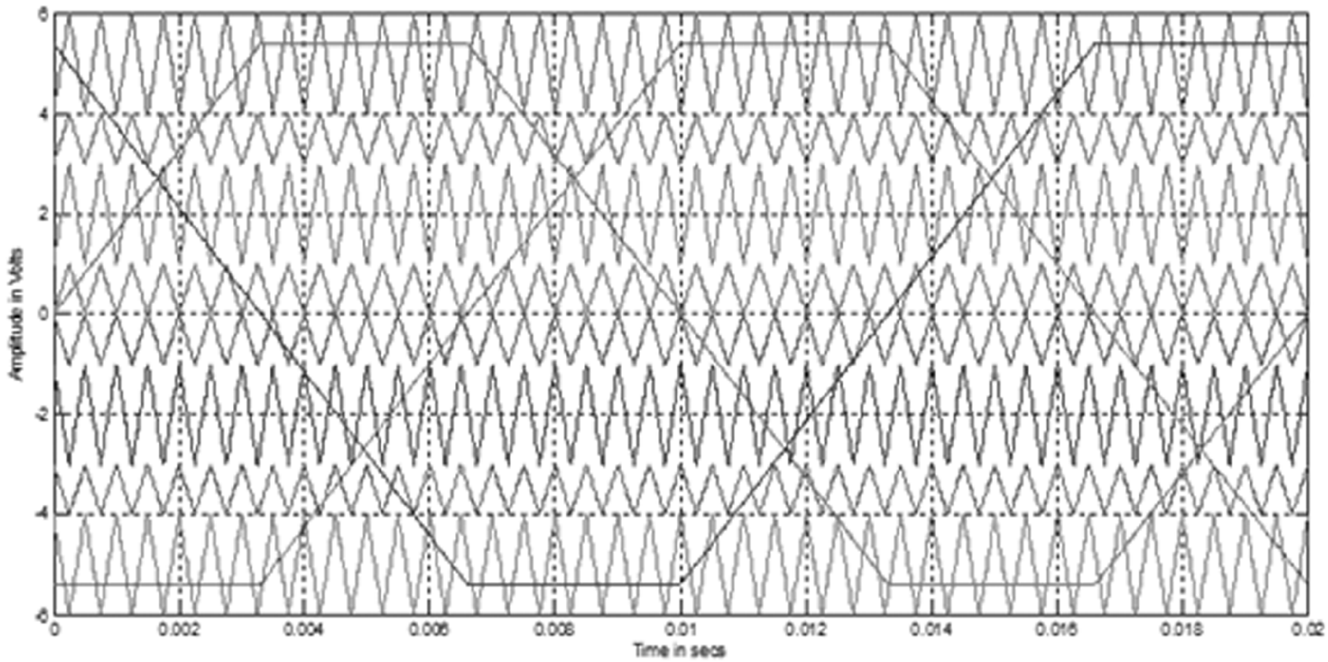

Figure 3: Carrier arrangement for PODPWM technique

3.3. Bipolar Variable Amplitude Alternative Phase Opposition Disposition PWM Technique

This method requires each of the eight carrier waves for a nine level inverter to be phase displaced from each other by 180° alternately. Fig.4 shows the carrier arrangement for APODPWM method for $m_a = 0.9$ and $m_f = 40$.

3.4. Bipolar Variable Amplitude Carrier Overlapping PWM Technique

In Carrier Overlapping technique, m-1 carriers are disposed such that the bands they occupy overlap each other, the overlapping vertical distance between each carrier is $A_C/2$ ($A_C = 1$). The reference waveform is centred in the middle of the carrier signals. The amplitude modulation index m_a is defined as follows:

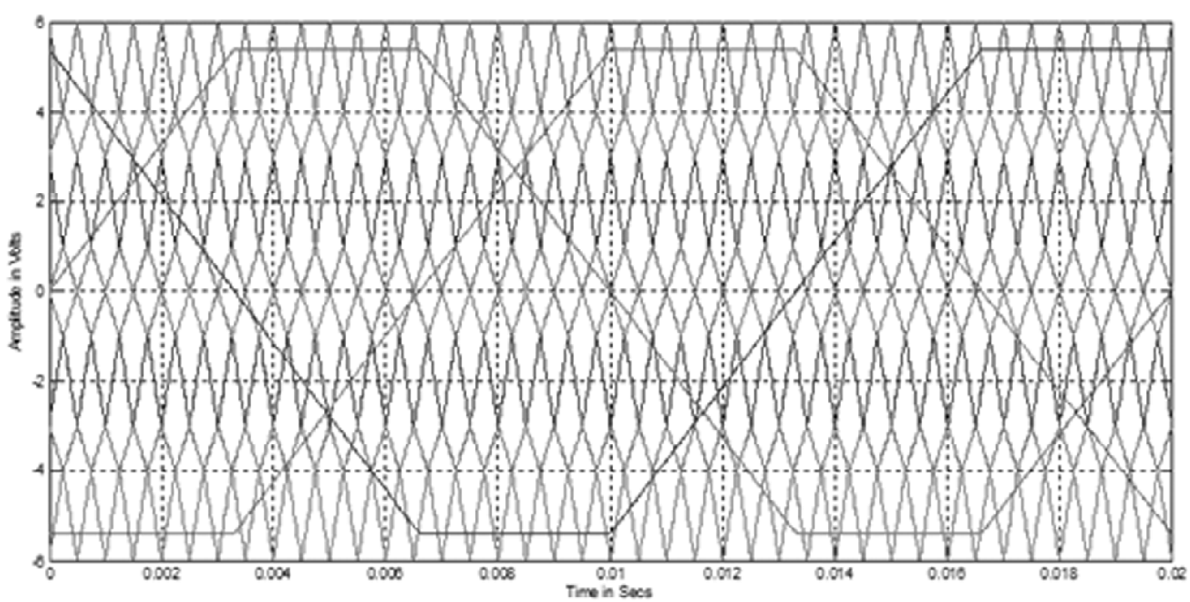

Figure 4: Carrier arrangement for APODPWM technique

$$m_a = \frac{A_m}{(2.5 \times A_c)} \quad (5)$$

The vertical offset of carriers for nine-level inverter with COPWM technique is shown in Fig. 5.

4. SIMULATION RESULTS

The three phase trinary source nine level cascaded inverter is modelled in SIMULINK using Power System block set. Switching signals for three phase trinary source nine level cascaded inverter are developed using bipolar variable amplitude PWM techniques having triangular carrier with Trapezoidal reference. Simulations are performed for different values of m_a ranging from 0.8 –1.

Figs. 6–13 shows the simulated output voltage of three phase trinary source nine level cascaded inverter with their corresponding FFT plots shown for only one sample value of m_a = 0.9 for above said BVAPWM

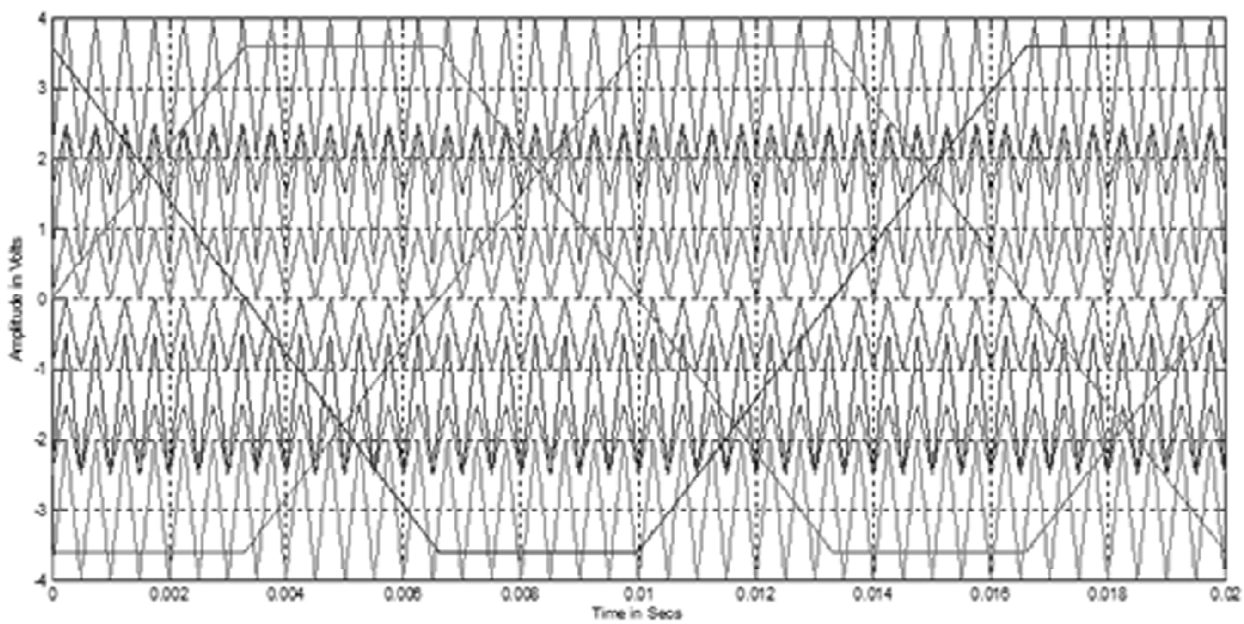

Figure 5: Carrier arrangement for COPWM technique

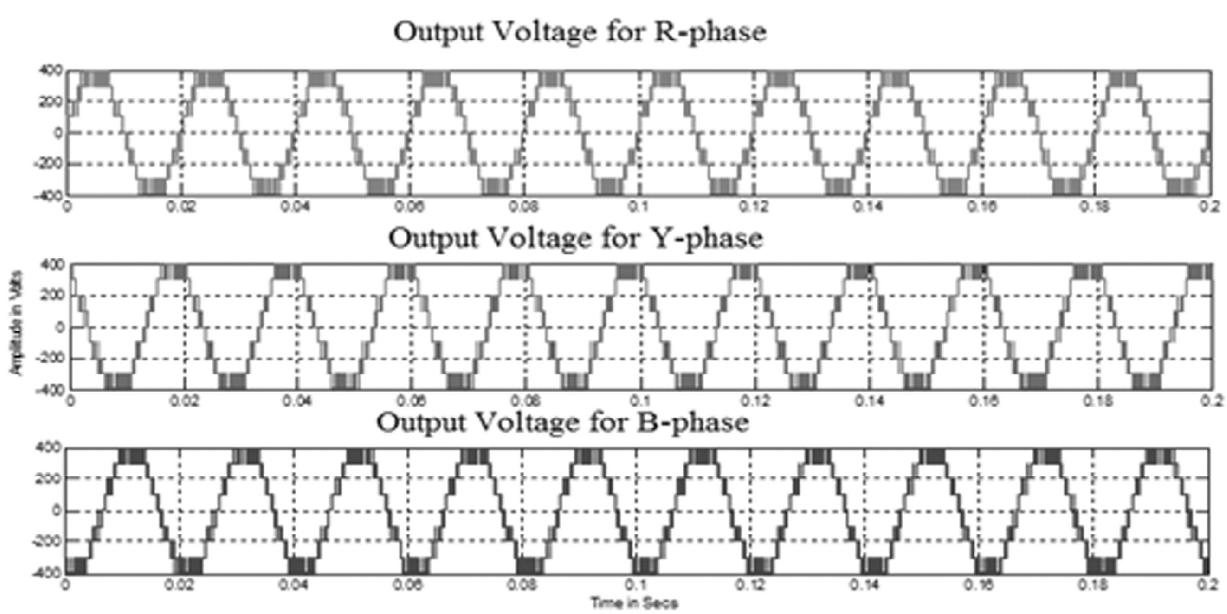

Figure 6: Output Voltage generated by PDPWM Technique

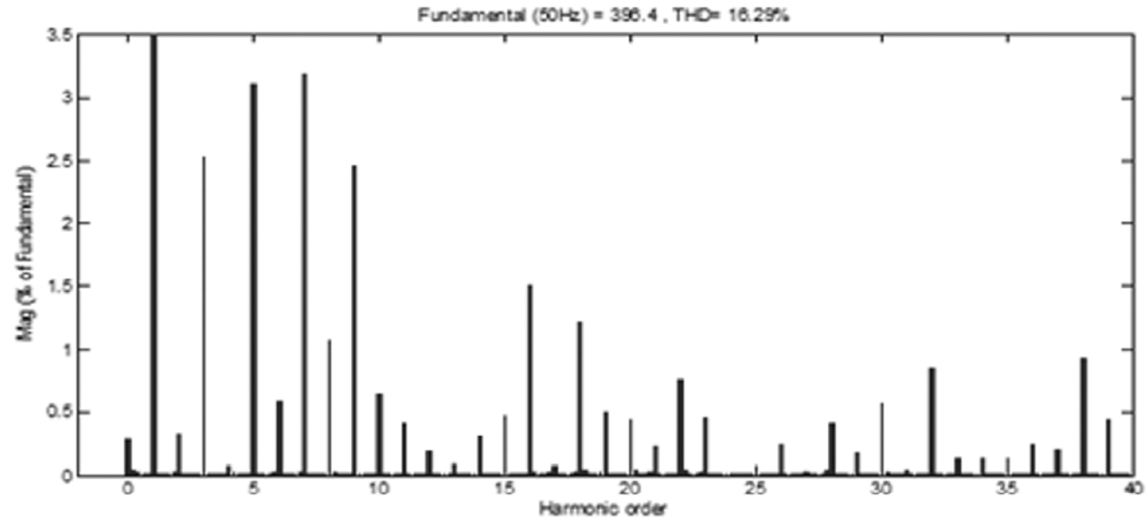

Figure 7: FFT Plot for Output Voltage of PDPWM Technique

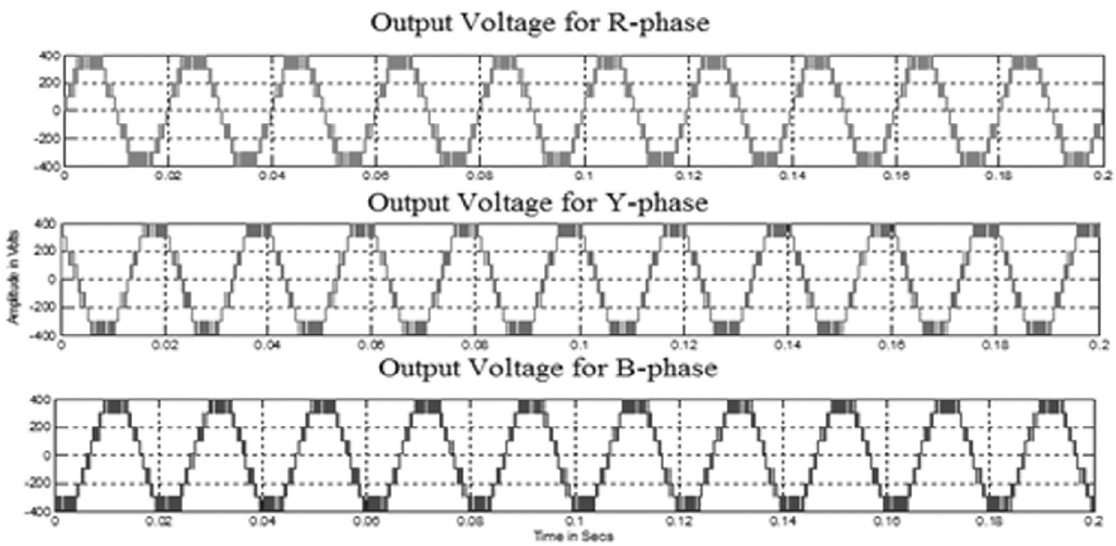

Figure 8: Output Voltage generated by PODPWM Technique

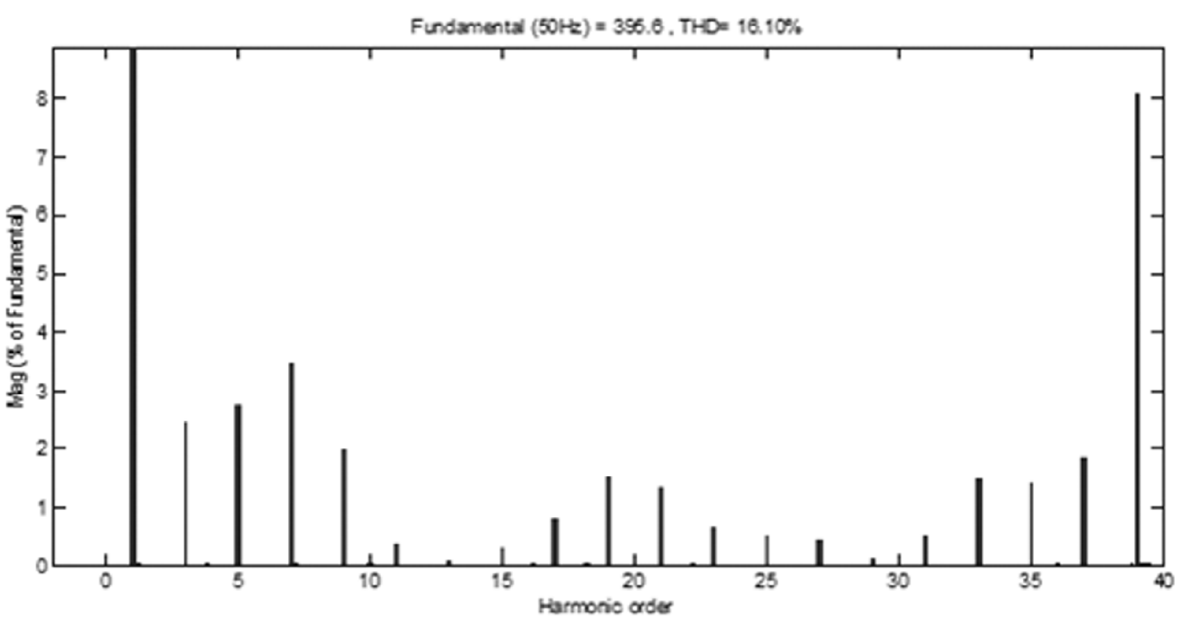

Figure 9: FFT Plot for Output Voltage of PODPWM Technique

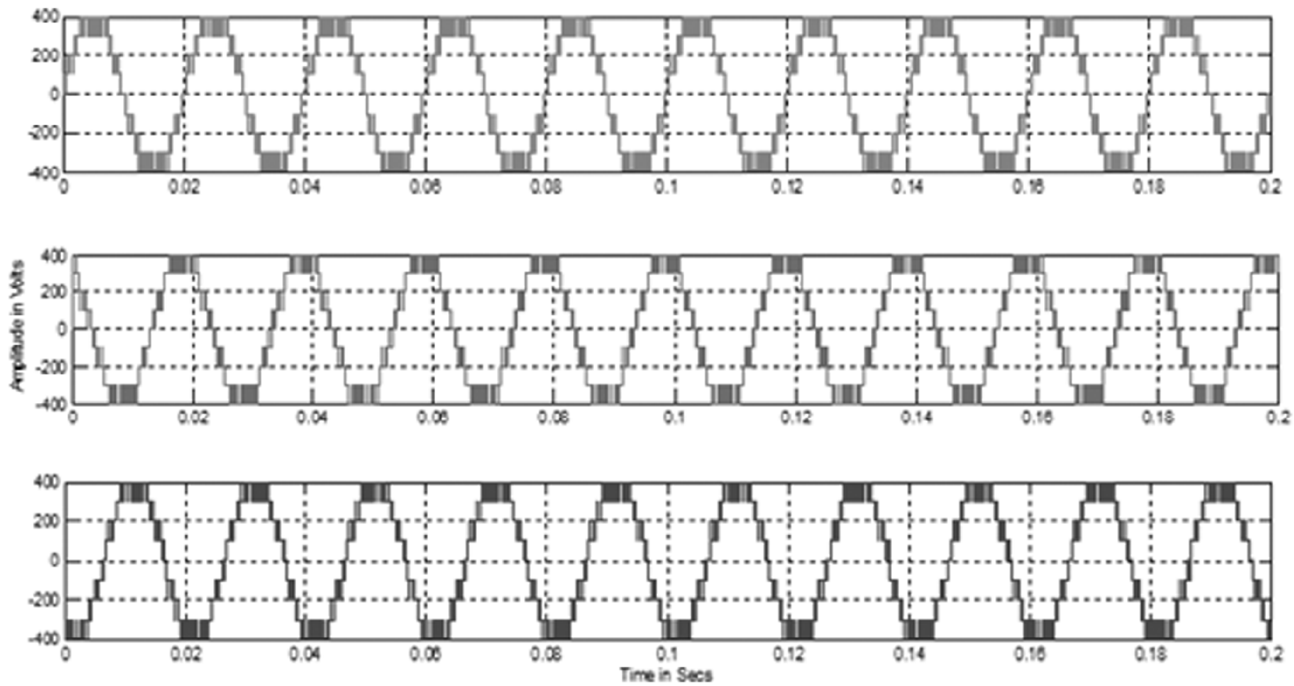

Figure 10: Output Voltage generated by APODPWM Technique

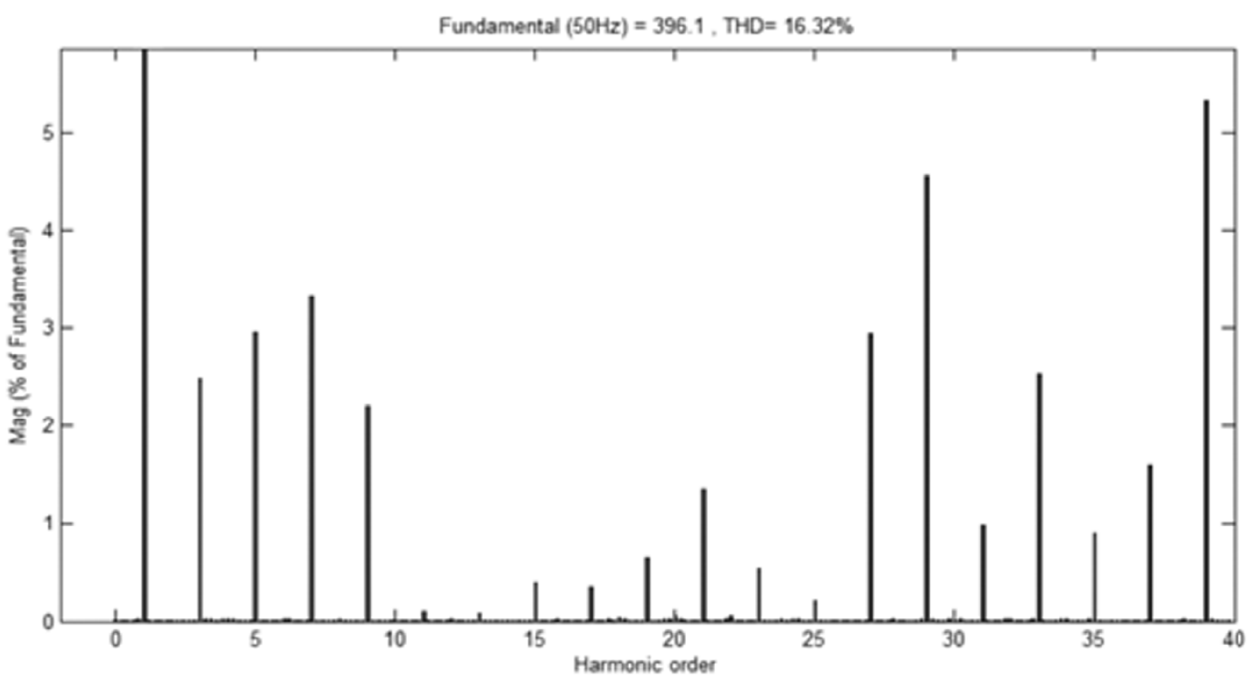

Figure 11: FFT Plot for Output Voltage of APODPWM Technique

techniques. Fig. 14 shows a graphical comparison of %THD of various techniques for different modulation indices.

The corresponding %THD (a measure of closeness in shape between a waveform and its fundamental component) is measured using the FFT block and their values are listed in Table 1. Table 2 shows the Distortion Factor of the output voltage of chosen CMLI. Table 3 displays the V_{RMS} of fundamental output voltage (a measure of DC bus utilization). The following parameter values are used for simulation: V_{DC} = 100V, $3V_{DC}$ = 300V, f_m = 50HZ, f_c = 2000Hz and load (R = 100Ω).

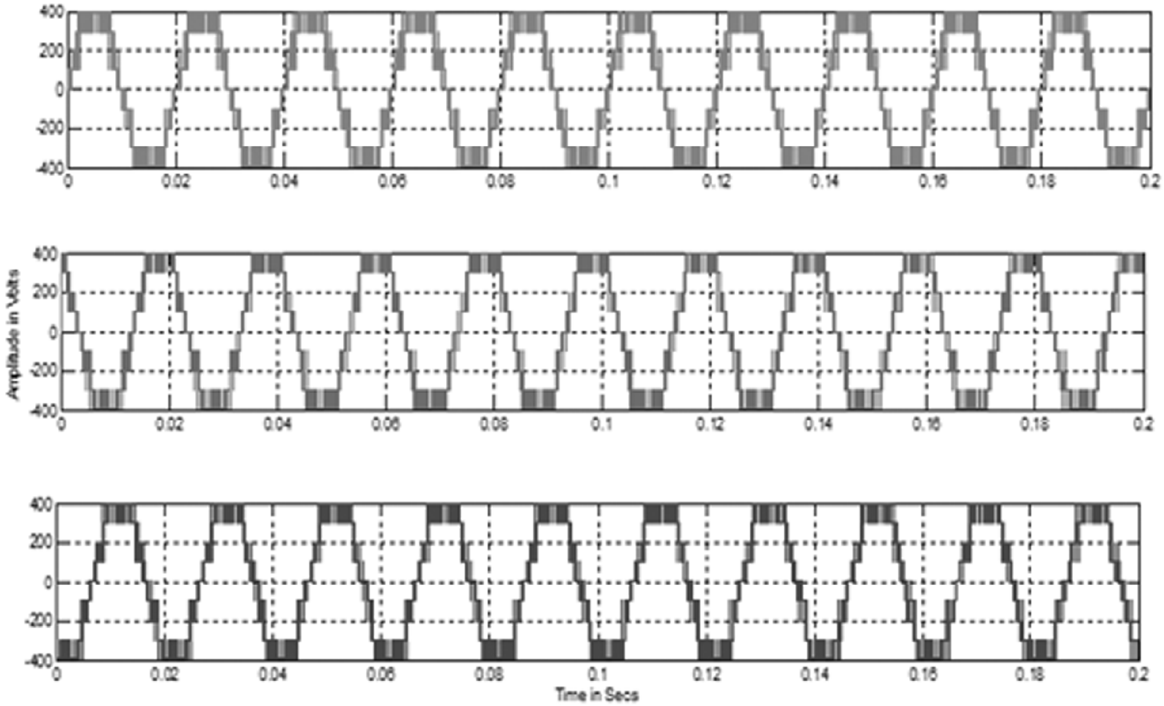

Figure 12: Output Voltage generated by COPWM Technique

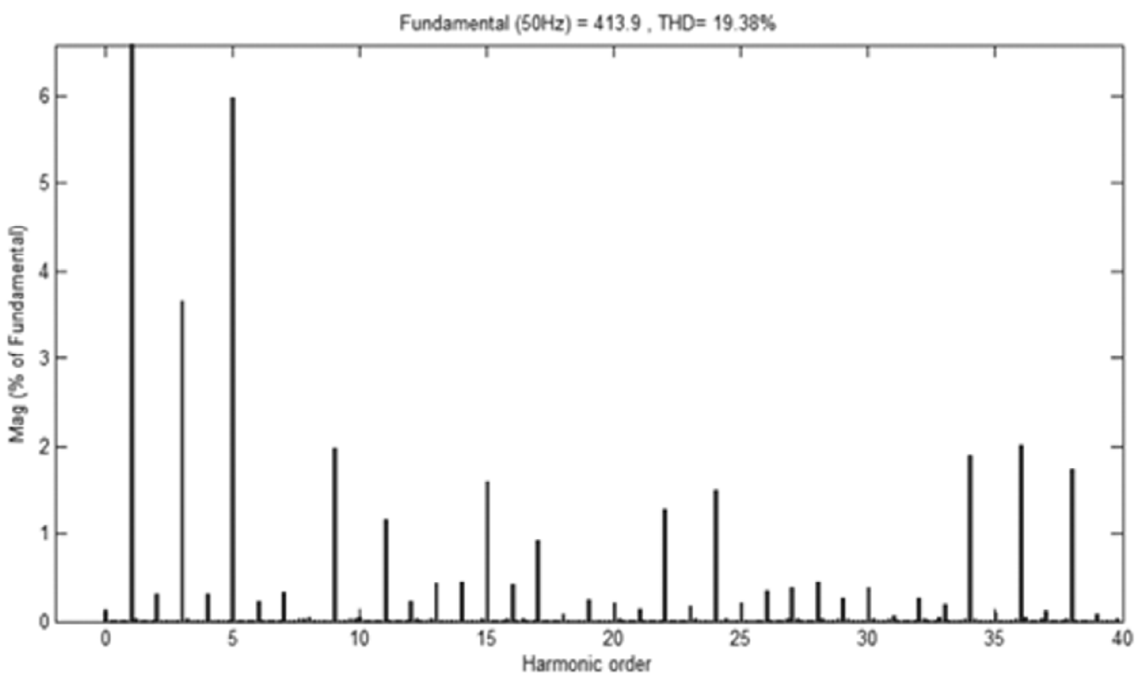

Figure 13: FFT Plot for Output Voltage of COPWM Technique

Table 1
%THD for Different Modulation Indices

m_a	*PDPWM*	*PODPWM*	*APODPWM*	*COPWM*
1	12.25	11.62	11.87	16.62
0.95	14.62	14.40	14.62	18.02
0.9	16.29	16.10	16.32	19.38
0.85	17.35	17.10	16.80	20.41
0.8	17.84	17.51	17.17	21.68

Table 2
%Distortion Factor for Different Modulation Indices

m_a	*PDPWM*	*PODPWM*	*APODPWM*	*COPWM*
1	0.4164	0.4366	0.4062	0.6542
0.95	0.3640	0.3967	0.3654	0.5717
0.9	0.3284	0.3042	0.3097	0.4772
0.85	0.2782	0.2442	0.2572	0.3813
0.8	0.2274	0.2466	0.2329	0.2938

Table 3
V_{RMS} (Fundamental) for Different Modulation Indices

m_a	*PDPWM*	*PODPWM*	*APODPWM*	*COPWM*
1	304.5	305.5	304.8	311.3
0.95	292.3	293.0	292.5	302.2
0.9	280.3	279.8	280.1	292.7
0.85	267.8	267.4	267.7	282.8
0.8	255.4	255.9	255.6	272.4

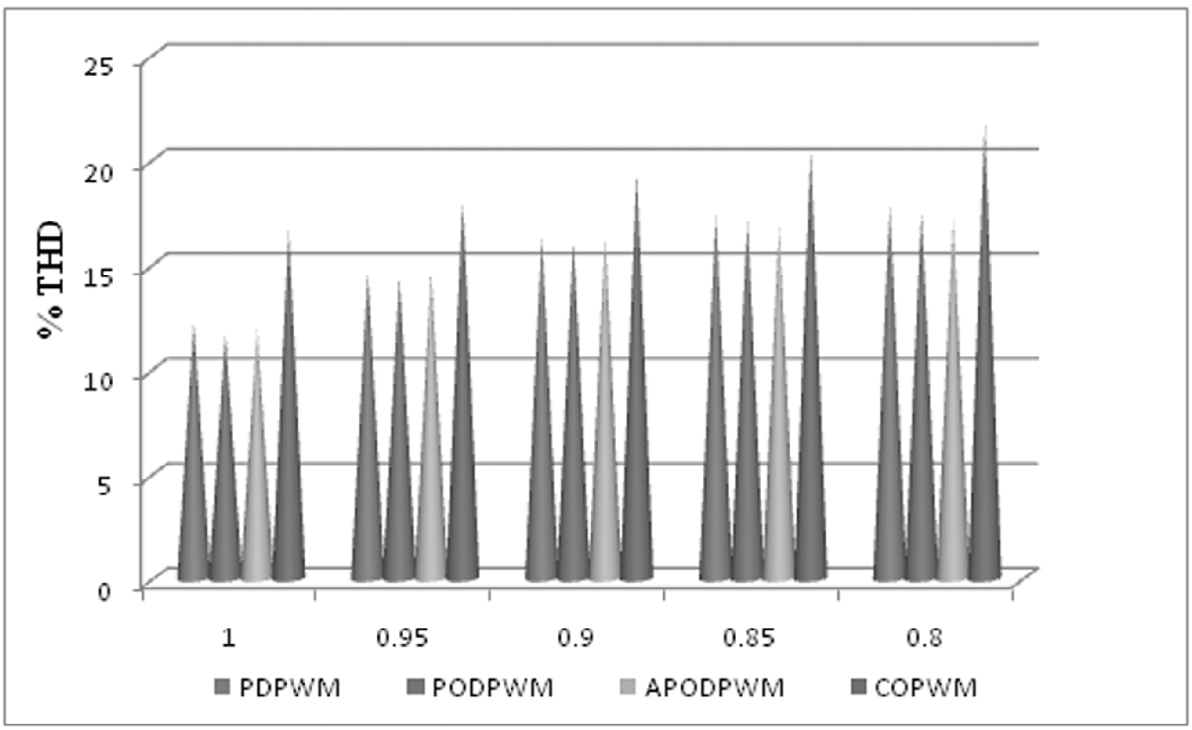

Figure 14: % THD V_s

Various performance factors like %THD, %DF and V_{RMS} of fundamental have been presented and analysed. The following are inferred from the FFT plot: The 3rd order harmonic dominant only in COPWM technique. In APODPWM technique 1st, 5th, 7th, 27th, 29th and 39th order harmonics are dominant. In PODPWM technique the first dominant harmonic appears at ($2m_f$-1). In PDPWM technique 5th and 7th order harmonics are dominant. It is observed from Table 1 that the harmonic content is found to be minimum in PODPWM technique for chosen modulation indices. Table 2 shows that the variation in harmonic content of the output voltage after second order attenuation indicated by %DF is less in APODPWM technique. From Table 3, it is found that the COPWM technique provide higher DC bus utilization.

4. CONCLUSION

In this paper, various bipolar variable amplitude PWM techniques for chosen three phase trinary source nine level cascaded inverter have been developed and simulation results are compared and presented for different modulation indices ranging from 0.8-1. The result indicates that appropriate PWM techniques may be employed depending on the performance measure required in a particular application of three phase trinary source inverter. The proposed PWM method with less THD and higher RMS voltage can be implemented in industrial applications such as AC Power conditioners, Static VAR Compensators, drive systems, etc and also in power generation industries.

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