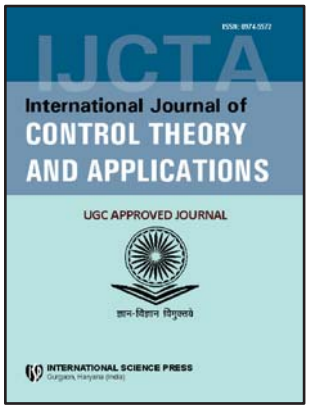

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Combined Effect of Sleep Mode Approach And LECTOR Technique For Reducing Leakage Power

Ayesha Firdous[a] M. Anand[b] and G. Saravana Kumar[c]

[a]*Research Scholar, ECE Department, Dr. M.G.R. Educational and Research Institute University, India*

[b]*Professor, ECE Department, Dr. M.G.R. Educational and Research Institute University, India*

[c]*Dean and Professor, ECE Department, Vel Tech High Tech Dr.Rangarajan Dr.Sagunthala Engineering College*

Abstract: The power consumption could be migrated at different levels such as Layout level, Circuit Level, Architectural level and Fabrication Process Technology Level. The significant method to minimize the level of power usage is to disable part of the circuit when the part is not under operation. By reducing the switching activity of a circuit, the power dissipation could be minimized. Various methods are used to optimize the power such as MTCMOS, Body biasing, Sleep, Zigzag, Leakage Feedback Approach, Dual Threshold Transistor Stacking, etc., In addition consumption of power in the circuit is data dependent. In this paper power reduction is achieved by combining two leakage reduction techniques(Sleep mode approach & LECTOR technique) and the simulation is carried out with and without power reduction technique using HSPICE.

Keywords: *Power consumption, leakage current, sleep mode, LECTOR.*

1. INTRODUCTION

Low power design methodology plays a major role in VLSI circuits. Low power circuit reduces cost of packing, cooling processor technology and development of handy devices are very high and these are depends on various parameters like weight, cost, life time. Sources of power dissipation can be classified as dynamic power and static power. When the circuit is in use and clock is present, power dissipation is called dynamic power. When the circuit is in idle, there will be a power dissipation that is called static power. Glitching power, switching power and short-circuit power are the sources of Dynamic power. Diode leakage current, subthreshold leakage current and gate leakage current are the sources of Static power. Fig.1. illustrates the various components of Leakage current. In Fig.1, subthreshold leakage current, GIDL, channel punchthrough current are occurs in off-state leakage mechanisms, while reverse-bias pn junction leakage current and oxide tunneling current occur in both ON and OFF states. gate current due to hot-carrier injection can occur in the off state[1]. This subthreshold leakage can be minimized by reducing supply voltage, high threshold voltage, longer gate length. The major factors affecting input-output power are voltage supply, capacitive load, output buffer slew rate.

I_1 = Reverse-bias pn junction leakage current
I_2 = Subthreshold leakage current
I_3 = Oxide tunneling current
I_4 = Gate current due to hot-carrier injection
I_5 = GIDL
I_6 = Channel punchthrough current.

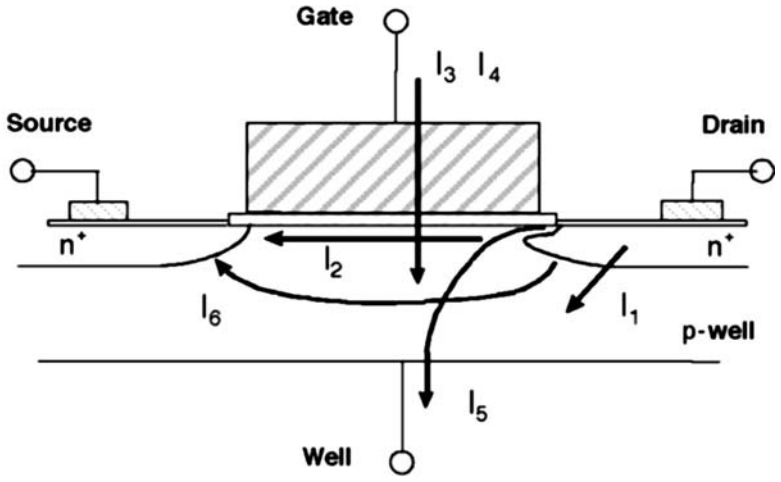

Figure 1: Summary of leakage current mechanisms of deep-submicrometer transistors.[1]

The subthreshold current can be modelled as follows[2].

$$I_{subth} = \mu_{eff} C_{ox} \frac{W}{L} V_2^t \times \exp\left(\frac{V_{GS} - V_{TH}}{nV_t}\right)\left(1 - \exp\left(-\frac{V_{DS}}{V_t}\right)\right)$$

Where V_t is the thermal voltage and it is written as $V_t = kT/q$. n is the subthreshold parameter

Leakage power ($P_{leak)}$ can be written as

$$P_{leak} = V_{DD} I_{leak}$$

When $V_{GS} = 0$,

I_{leak} corresponds to the subthreshold current

$$I_{ds,\,leak} = \mu_{eff} C_{ox} \frac{W}{L}(n-1)V_t^2 e^{-V_{Th}/V_t}$$

There are various methods to control leakage current. Each method has its own advantage and disadvantage.

This paper is organized as follows. Section II explains about the previous work in leakage power reduction, Proposed power reduction technique is explained in Section III . Results and Discussion is in Section IV. Finally, the conclusion of the paper appears in Section V.

2. PREVIOUS WORK

Reducing the supply voltage is one way to reduce the power dissipation of CMOS circuit but this leads to reduce transistor threshold voltages to maintain performance and noise margins. Reducing threshold voltage leads to an increase in the subthreshold leakage current of PMOS and NMOS, which starts to offset the power savings obtained from power supply reduction. Reducing the threshold voltage further leads to focus many factors in future technology.a design technique should be identified to reduce leakage current and power that can be used in a logic design. [5]

In sleepy keeper approach PMOS, NMOS transistors are added in between VDD to Pull-Up network and Pull-Down network to GND [3]. In stack approach, The leakage current is reduced when more than one transistor of the stack is turned OFF. In sleepy stack approach, the sleep and stack approaches are combined. In the stack approach, stack effect is introduced by breaking down an existing transistor into two half size transistors [6, 7, 8].

In [9] a method to design and optimize low voltage dual-Vth CMOS circuits. In order to minimize leakage power under performance constraints, starting with a single low Vth circuit, an optimal high threshold voltage is proposed for selecting an assigning a heuristic algorithms. Multithreshold Voltage CMOS (MTCMOS) circuit technology was proposed to minimize the leakage current by adding high threshold devices in the circuit [10].

In MOSFET, reducing the threshold voltages leads to increase in leakage power dissipation caused by subthreshold condition. The leakage power cannot be neglected for low threshold voltage device [11]. LECTOR stack state retention with sleepy transmission approach is presented in [12]

3. PROPOSED POWER REDUCTION TECHNIQUE

3.1. Sleep Mode Approach

In sleep mode approach, PMOS transistor is placed between supply voltage to pull up network and NMOS transistor is placed in between pull down network and GND. Sleep transistor is turned on when the circuit is in active mode. Sleep transistor is turned off when it is in standby mode. To prevent high leakage current threshold voltage of sleep transistor is kept high. Fig.2 shows the block diagram of sleep mode approach. The proposed work takes an advantage of sleep mode approach. Number of transistor needed to design a circuit in this approach is 2+2N. Where N is the number of transistor. Compare to CMOS technology, sleep mode approach uses two more transistor in addition to the normal circuit.

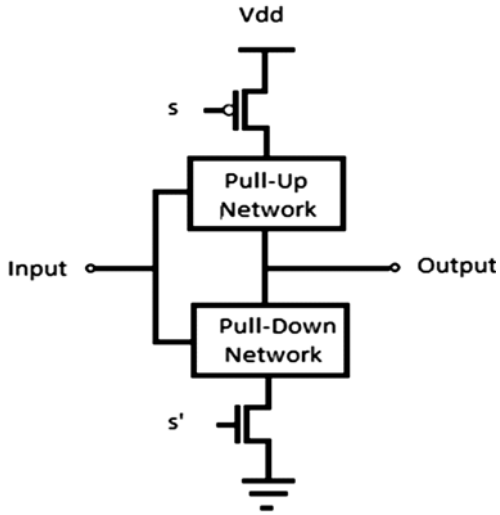

Figure 2: Sleep Mode Approach

3.2. LECTOR Approach

The noteworthy feature of LECTOR is that it works good in both active and idle states of the circuit, this leads in better leakage reduction [4]. In this approach NMOS and PMOS transistors are added in between pull up network and pull down network. Gate terminal of PMOS, NMOS transistors are controlled by source of the other. LECTOR method is more effective in both active and standby mode. The block diagram of LECTOR approach is shown in Fig.3.

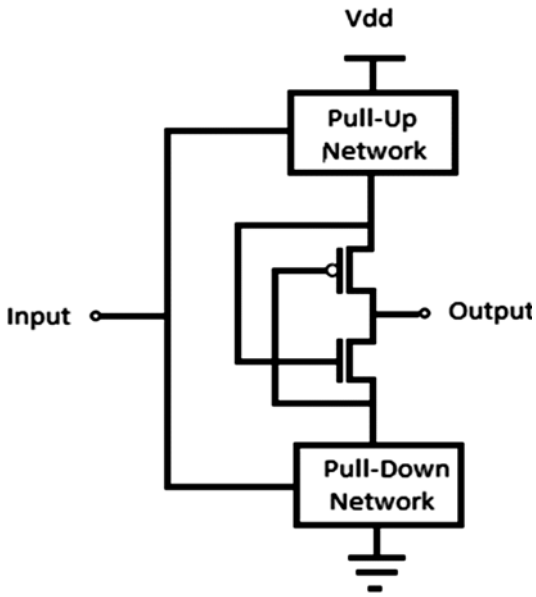

Figure 3: LECTOR Approach

3.3. Proposed Method

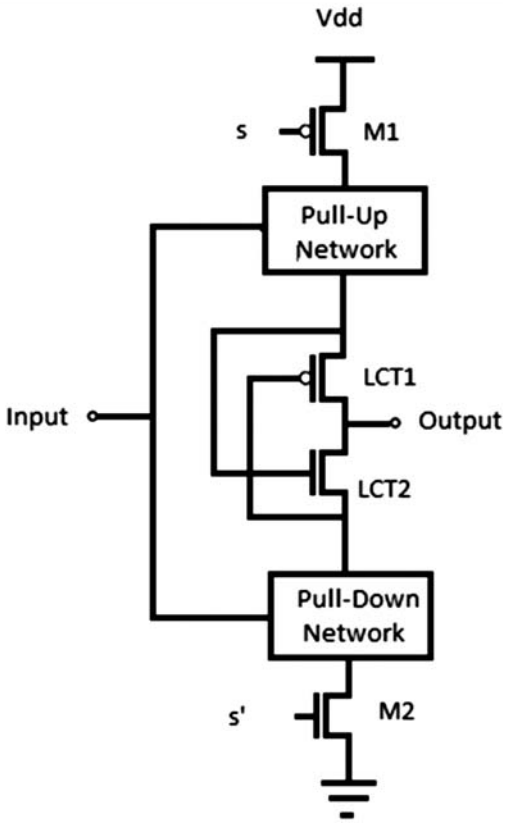

Figure 4: Proposed Circuit

In the proposed circuit (Fig. 4), when $s = 0$, NMOS transistor M2 is off, pull-down path is disabled and static current will not flow in the circuit. When $s = 1$, PMOS transistor M1 is off and NMOS transistor M2 is turned on. Based on the input values and pull down topology circuit output is conditionally discharged. LCT1 and LCT2 are Leakage control transistors it is controlled by source of the other. This ensures that one of the Leakage control transistor always operates in its near cutoff region. From supply voltage to ground, If more than one transistor is OFF in a path the leakage current of the circuit will be less compare to only one transistor OFF in the path from supply to ground.

3.4. Design Example

Fig. 5. Shows the design of two input NAND. To design this circuit 4 + 2N transistors are needed. Here N represents the number of inputs. 8 transistors are needed to design the circuit. In LECTOR and sleep mode approach, 6 transistors are needed to design two input NAND gate but the proposed technique reduces leakage current. Table 1 shows the comparison of transistor needed in different techniques

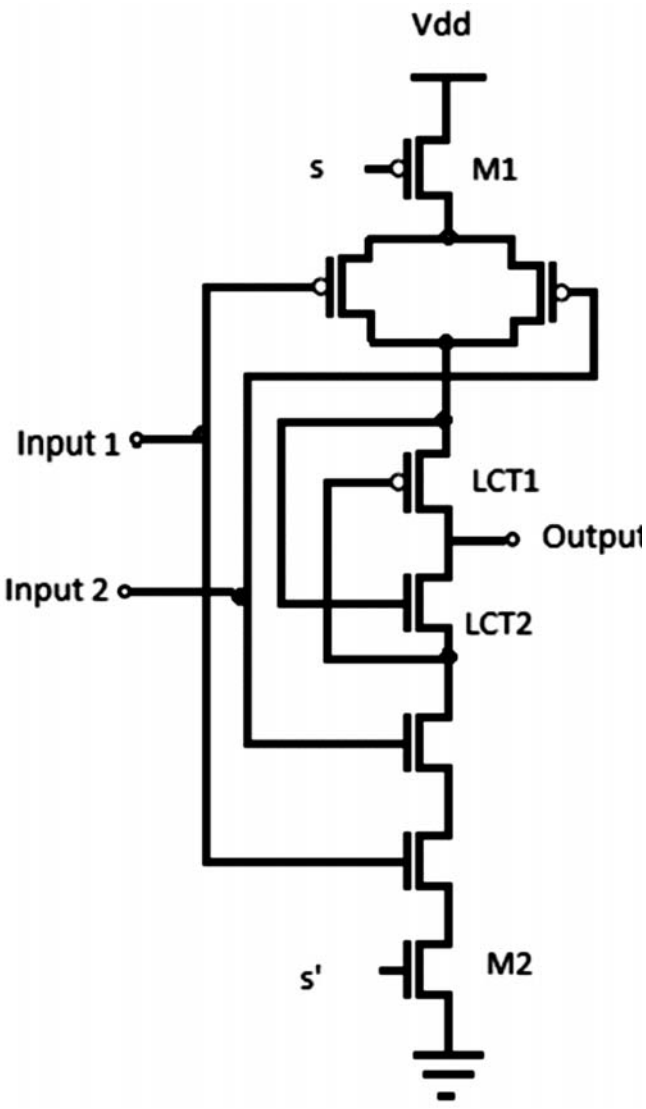

Figure 5: Proposed two input NAND gate

Table 1
Comparision of Transistors Needed in Different Techniques

	Technique			
	CMOS	*LECTOR*	*Sleep Mode*	*Proposed Technique*
Number of Transistors	2N	2 + 2N	2 + 2N	4 + 2N

4. RESULTS AND DISCUSSIONS

In this work two input NAND is designed by combining sleep mode approach and LECTOR technique. It is implemented in 90nm CMOS technology. The simulation is carried out with and without power reduction technique using HSPICE with a supply voltage of 1volt and temperature of 27ºC. Table 2 provides the comparison of leakage power dissipation of two input NAND gate.

Table 2
Comparison of Leakage Power for two Input Nand Gate

Leakage Power Dissipation in Watts	
Sleep Mode	3.153E-09
LECTOR	4.34E-09
Sleep Mode + LECTOR	2.95E-09

Figure 6 shows the leakage power of two input NAND gate with different techniques

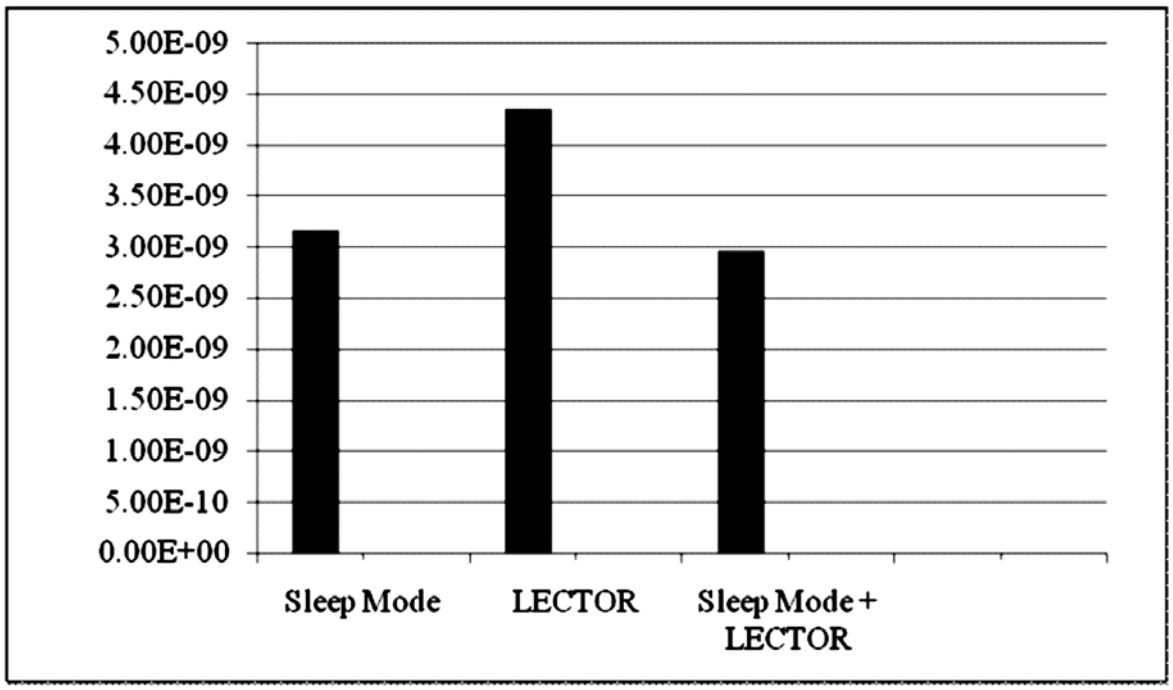

Figure 5: Comparision of Leakage Power

5. CONCLUSION

This paper evaluates power reduction technique for VLSI circuits. Compared to CMOS, LECTOR and Sleep mode approach, the number of transistor is higher in proposed circuit. It would appear proposed logic presents a major advantage in power reduction and this method is more effective on both active and standby region.

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