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Comparative Simulation Analysis of Harmonics in Line-Line Output Voltage of Multilevel Inverters for Different Modulation Indices

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Abstract: The cascaded H-Bridge (CHB) 3-level and 5-level inverter is intending to compare the line-line output voltage harmonics under inductive load. The sine wave as reference with multiple triangular carriers is used to on-off the control device. An Insulated Gate Bipolar Transistors (IGBTs) is used as control device in the proposed inverter. The simulation result of harmonics in line-line output voltage is compared with diode clamped and capacitor clamped of 3-level and 5-level inverter. The proposed work is implemented using simulation software.

Keywords: Multilevel Inverter, Multicarrier PWM Technique and Total Harmonic Distortion.

1. INTRODUCTION

The utilization of non-linear loads degrades the quality of power transfer. In general LC filters are implemented to make quality of power due to low cost [1-2]. This type of LC filters suffers from resonance [2]. To avoid above disadvantage an Active Power Filter (APF) is a substitute solution to mitigate problems in power quality. An APF may be adopting near the load or at middle of the line so called at the point of common coupling (PCC) [3]. APFs are usually voltage controlled based or Current-controlled based inverters to provide the required compensation voltages/ currents in [4]. In [5]–[6], presented the development of APFs to overcome the drawbacks of passive filters. The concept of different types of multilevel inverter principles, significance and their applications is presented in [7].

The concept of cascade H-bridge (CHB) inverter is presented in [7] due to its structure, feasibility and consistency compare to all other multilevel inverters. The connection of separated dc source for each H-bridge circuit is considered in [8]. The CHBs are usually considered for an industrial application due to good performance and efficiency [9]. Advantages of multilevel inverters compare to conventional inverters for high power-high voltage or medium voltage is discussed in [10]. An overcome of electromagnetic interference issues due to high frequency is explained in [11]. The CHB inverter is proposed due to all above advantages to analyze the harmonic spectrum of line-line output voltage under inductive load.

2. MULTILEVEL INVERTERS

In this paper, three different types of multilevel inverters are considered to analyze harmonic spectrum in load voltage and hierarchical chart is shown in Figure 1(a).

The generalized schematic diagram of multilevel diode clamped inverter is shown in Figure 1 (b). The capacitor-clamped configuration fed high voltage *dc*-*dc* is explained in [12]. The *dc* voltage balancing methodology is presented in [12], [13]. However, the drawback of capacitor clamping floating in each leg

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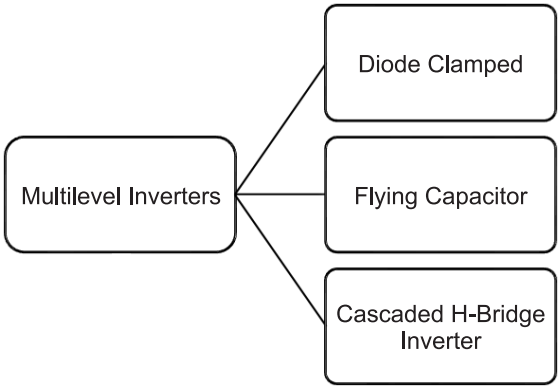
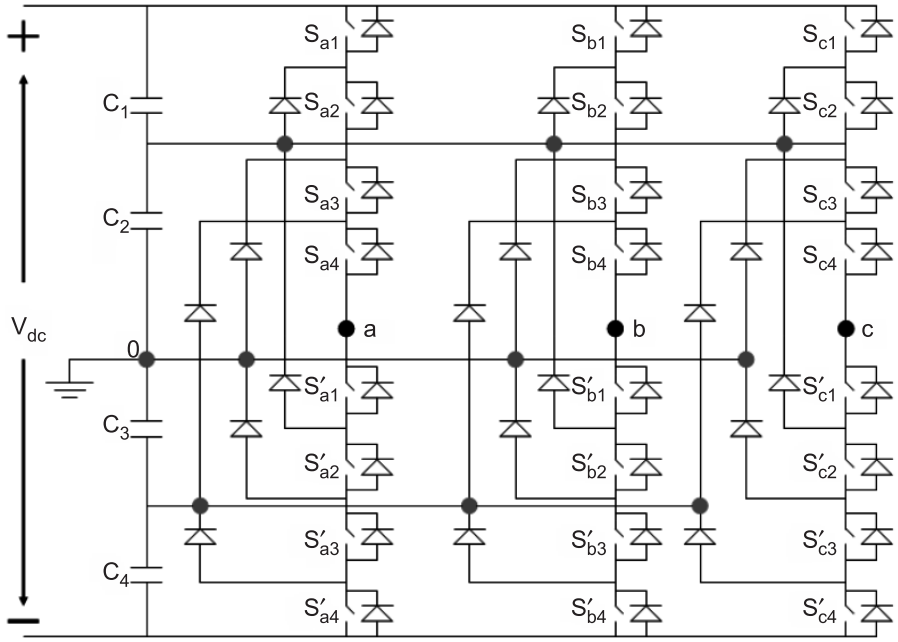


(a)



(b)

Figure 1: (a) Types of multilevel inverters and (b) 3-phase 3 leg Five-level diode clamped inverter [19]

is discussed in [7]. The structure of multilevel capacitor clamped inverter is shown in Figure 2 (a). Initially the CHB inverter is applied for an application of motor drive [9]. However, a different type of applications of CHB inverter includes the power quality, adjustable speed drives, reactive power compensation and shunt active power filters presented in [7], [15], [16], [19]. The schematic diagram of *m*-level CHB inverter is shown in Figure 2(b).

The total number of clamping diodes required for each phase of diode clamped inverter is expressed in eqn. (1) and the clamping diodes are not required for the rest of two multilevel inverters.

$$N_{CD} = (m-1) \times (m-2) \tag{1}$$

The total number of main diodes required for each phase of diode clamped, capacitor clamped and cascaded H-bridge inverter is expressed in eqn. (2).

$$N_{MD} = (m-1) \times 2 \tag{2}$$

The total number of main switching diodes required for each phase of 3 multilevel inverters are same and expressed in eqn. (3).

$$N_{MS} = (m-1) \times 2 \tag{3}$$

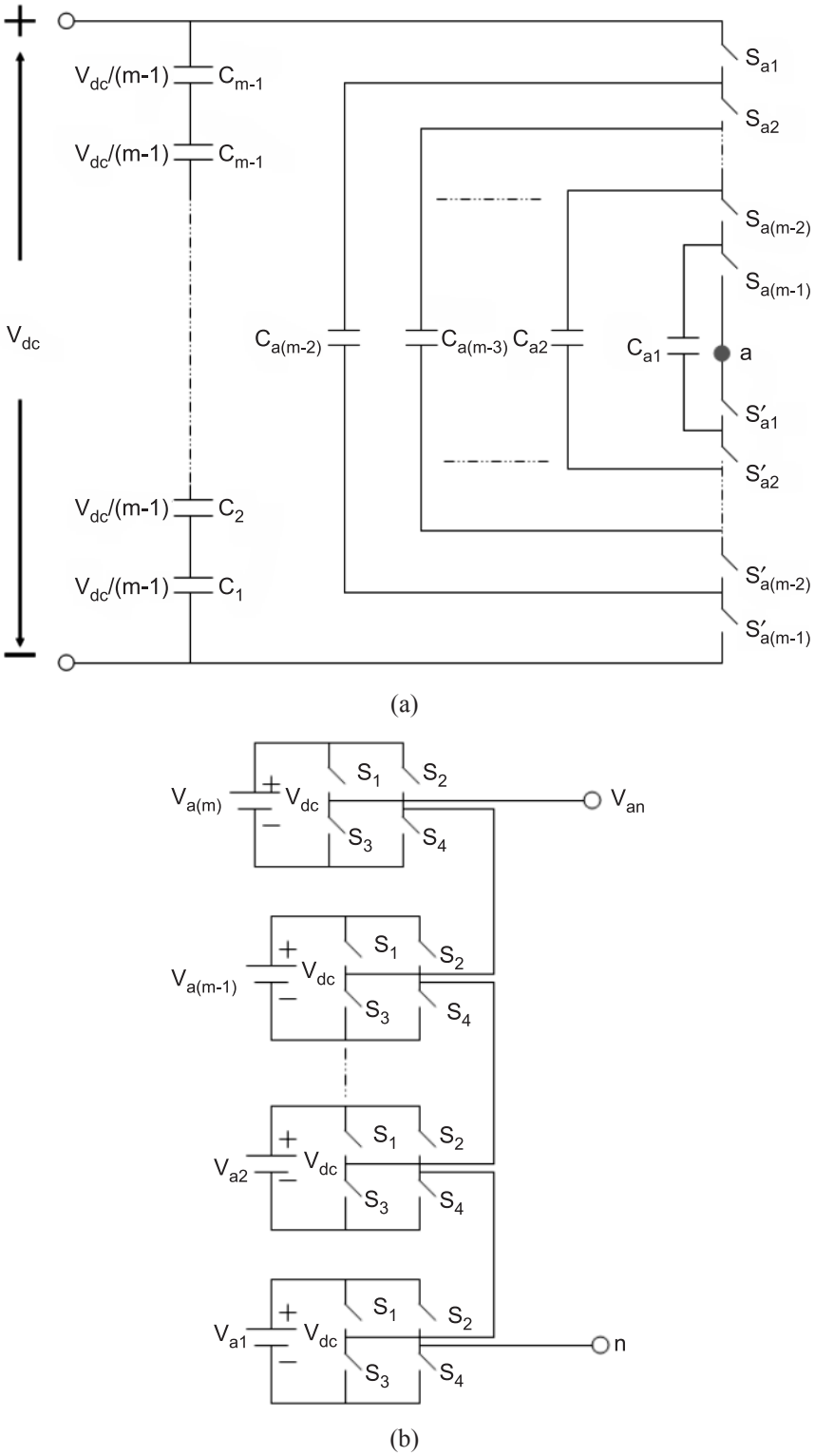


Figure 2: Generalized schematic diagram of (a) capacitor-clamped inverter and (b) CHB inverter [19]

The total number of DC bus capacitors required for each phase of diode clamped and capacitor clamped multilevel inverters is same and expressed in eqn. (4)

$$N_C = (m - 1) \tag{4}$$

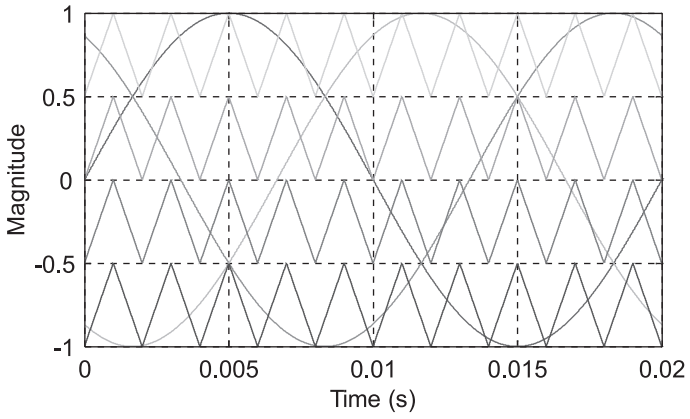
The total number of DC bus capacitors required for each phase of cascaded H-bridge multilevel inverter is expressed in eqn. (5)

$$N_{CH} = N_{CH} = \frac{(m-1)}{2} \quad (5)$$

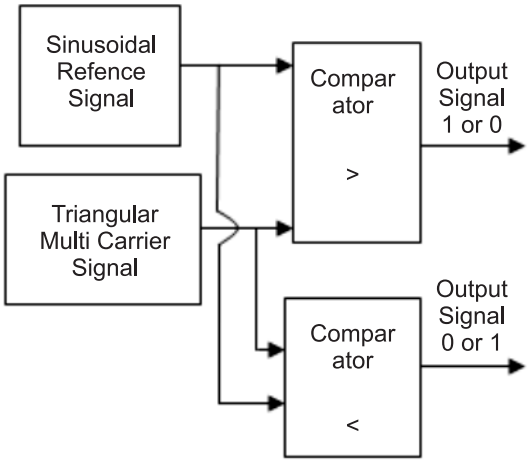
The balancing capacitors are not required for the diode clamped and cascaded H-Bridge multilevel inverters. However, it is required for the capacitor clamped multilevel inverter and it is expressed in eqn. (6)

$$N_{BC} = N_{BC} = \frac{(m-1)\,x\,(m-2)}{2} \quad (6)$$

3. MULTI CARRIER PWM TECHNIQUE



(a)



(b)

Figure 3: (a) Generation of gate pulses with triangular carriers and (b) controller block diagram using SPWM

In this paper, the level shift multicarrier SPWM technique is considered for analyzing the harmonic spectrum of load voltage using simulation results of diode clamped inverter, capacitor clamped inverter and CHB inverter. The phase disposition sinusoidal pulse width modulation technique is considered to study the simulation results [17], [18]. The level shift multicarrier along with sinusoidal reference signal is shown in Figure 3(a) and the controller block diagram is shown in Figure 3(b).

4. SIMULATION RESULT ANALYSIS

In this Section, the simulation results are analyzed with RL load for various types of multilevel inverters with different modulation indices. An IGBT controlled switching devices are used in all the types of multilevel inverters. The simulation block diagram is shown in Figure 4. All the inverters are simulated and presented for various modulation index values. Simulation parameters are listed in Table 1.

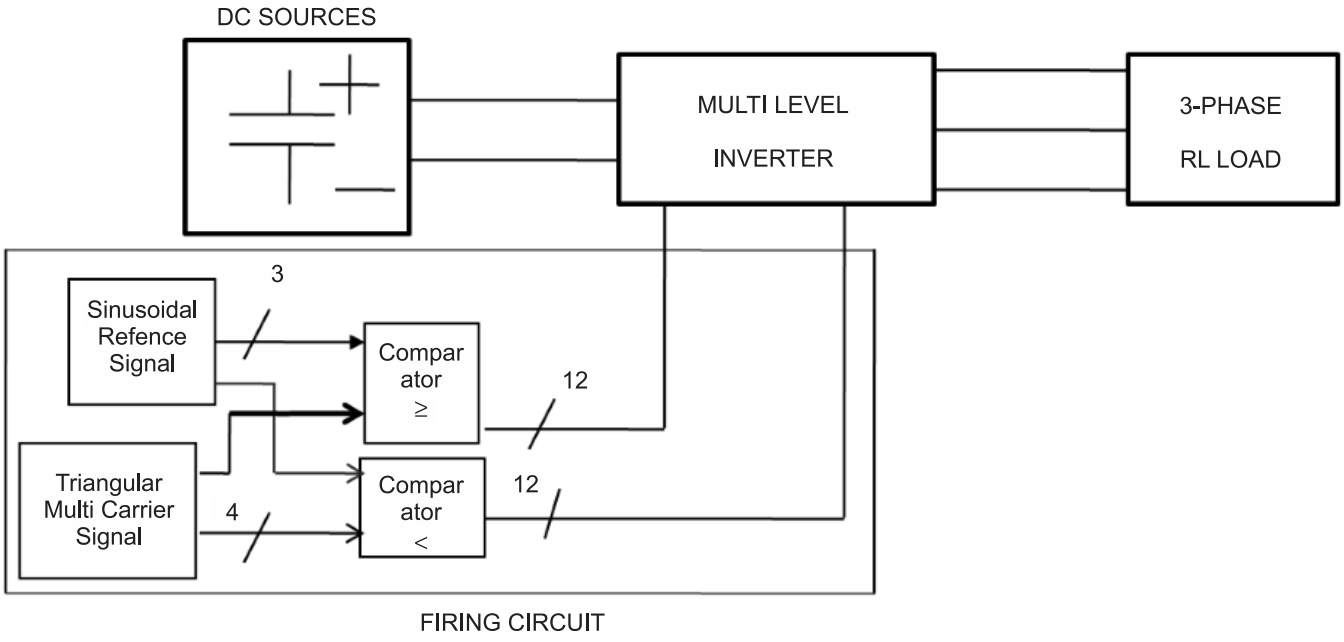


Figure 4: Complete simulation block diagram for five-level inverter

Table 1
Simulation parameters

S.No.	*Parameter*	*Values*
1.	RL load	R = 50 Ω, L = 110 mH
2.	Switching frequency	10kHz
3.	Supply frequency	50Hz
4.	DC Voltage	400V
5.	Controlled Switches	IGBTs

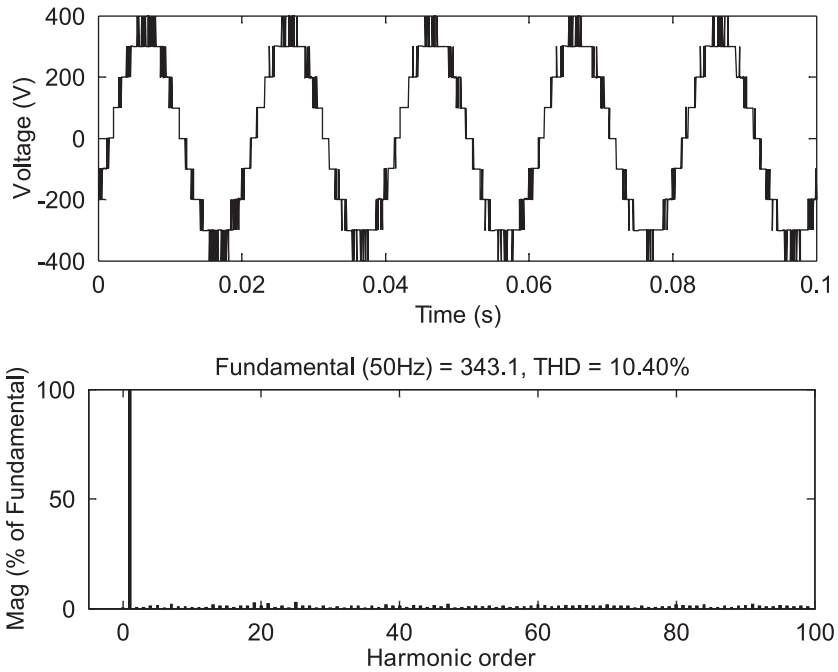


Figure 5: Line-Line Voltage and Harmonic Spectrum of 5-level Diode Clamped inverter

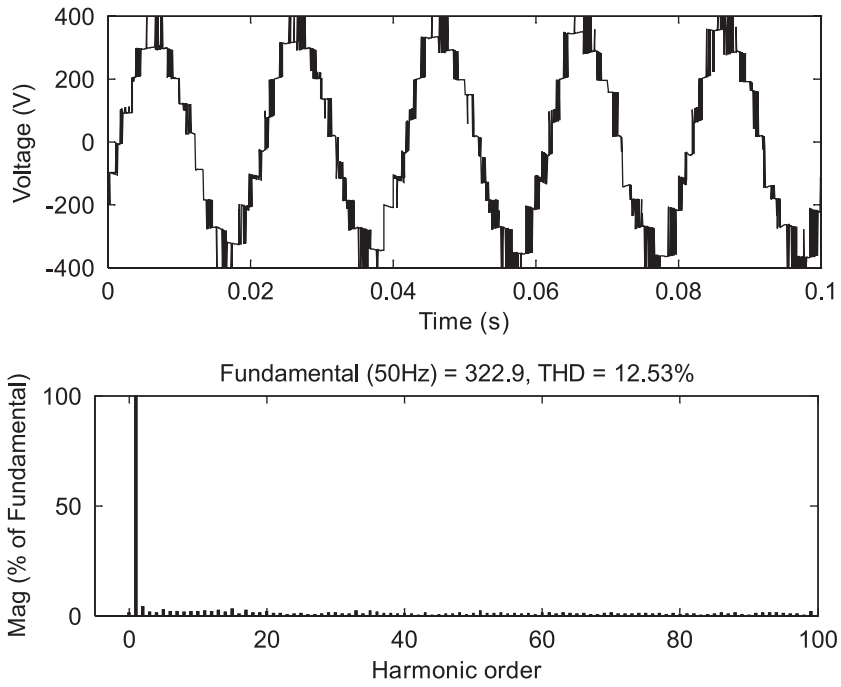


Figure 6: Line-Line Voltage and Harmonic Spectrum of 5-level Capacitor Clamped inverter

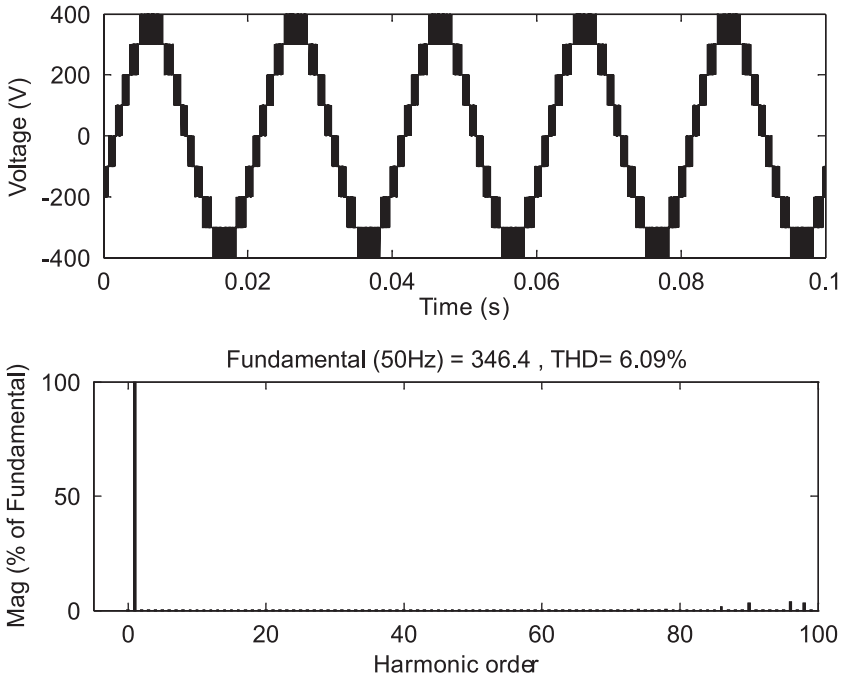


Figure 7: Line-Line Voltage and Harmonic Spectrum of 5-level Cascade H-Bridge Inverter

All the 5-level inverters are simulated for various modulation indices and the best modulation index results is presented. The line-line voltage and harmonic spectrum of diode clamped 5- level inverter is shown in Figure 5, capacitor clamped 5-level inverter is illustrated in Figure 6 and cascaded 5-level inverter is presented in Figure 7. The total harmonic distortion of 5-level diode clamped, capacitor clamped and CHB inverters are 10.40%, 12.53% and 6.10% respectively. A summary of THD for 3-level and 5-level diode clamped, flying capacitor and CHB inverters are tabulated in Table 2. The %THD of output voltage for various multilevel inverters for different values of modulation indices are illustrated in Figure 8 respectively. It is required to reduce the harmonics for improving the inverter performance.

Table 2
% THD comparison of 3-level and 5-level inverter for diode clamped, capacitor clamped and CHB

Modulation Index (M)	*Diode Clamped Inverter*				*Capacitor Clamped Inverter*				*Cascade H-Bridge Inverter*			
	3 level		*5 level*		*3 level*		*5 level*		*3 level*		*5 level*	
	Voltage (V)	*%THD*	*Voltage (V)*	*%THD*	*Voltage (V)*	*%THD*	*Voltage (V)*	*%THD*	*Voltage (V)*	*%THD*	*Voltage (V)*	*%THD*
M = 1	285	32.12	343.1	10.40	340.8	24.83	324.1	13.12	300.9	17.23	346.4	6.09
M = 0.9	220.2	27.46	308.5	10.80	271.9	30.33	306.6	12.67	292.7	15.81	311.7	5.31
M = 0.8	219.5	23.25	282.7	13.66	246.4	30.40	271.1	15.39	282.5	15.76	277.1	8.28
M = 0.7	217.2	21.28	238.6	13.77	231.4	29.50	226.2	20.56	264.1	18.82	242.5	8.48

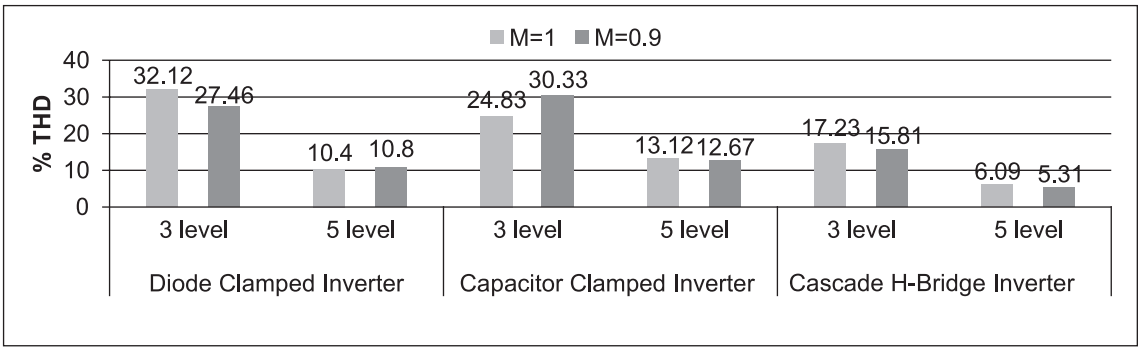


Figure 8: Illustration of % THD comparison of Voltage for (a) 3-level and (b) 5-level inverters

5. CONCLUSION

The simulation results of percentage total harmonic distortion for diode clamped, flying capacitor and CHB inverters is discussed. From simulation result analysis, the cascaded 5-level inverter has less total harmonic distortion of 6.10% (modulation index = 1) and 5.31% (modulation index = 0.9) when compared to diode clamped and flying capacitor inverters.

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