I J C T A, 9(13) 2016, pp. 5893-5899

Area and Delay Optimization using Various Multiple Constant Multiplication Techniques for FIR Filter

[1]P. Radhika, [2]A. V. Sunil, and [3]T. Vigneswaran

ABSTRACT

An exact Filter Design Optimization (FDO) algorithm that can guarantee the minimum design complexity, but can only be applied to filters with a small number of coefficients. Then introduce multiple constant multiplications and using exact and approximate algorithm that can handle filters with a large number of coefficients using less computational resources than the exact FDO algorithm and find better solutions than existing FDO heuristics. These algorithms can be modified to handle a delay constraint in the shift-adds designs of the multiplier blocks and to target different filter constraints and filter forms. Experimental results show the effectiveness of the proposed algorithms with respect to prominent FDO algorithms. In this FDO technique there are three type of FIR technique we use to implement the graph based, common sub-expression elimination, digit based recording algorithms and compare the area and delay

Index Terms: Multiple constant multiplications digit based recording algorithm, common subexpression algorithm,graph based algorithm, digit size

1. INTRODUCTION

Multiple Constant Multiplication is involved to produce constant multiplication in Digital Signal Processing systems, and Multiple Input Multiple Output systems, Error correcting codes, Frequency multiplication, Graphics and Control applications. In such applications full term of multipliers are not needed. Since coefficients are constant to produce constant multiplication. Once the MCM architecture is constructed, it can be called as many times it required. Constant multiplication can be done by digit parallel design and digit serial design. Digit parallel design of constant multiplier needs external wire for shifting and it requires more area in implementation takes place in Field Programmable gate array. Hence digit serial design overcomes area constrain with acceptable delay timing. Multiplication with constant is called constant multiplication. This process is used in filter operation. There are two types of constant multiplication. One is Single Constant Multiplication and second one is Multiple Constant Multiplication. Input is multiplied with single specific coefficient to produce output is called SCM. Canonical Signed Digit number representation is used to implement SCM multipliers. Input is multiplied with multiple numbers of specific coefficients to produce multiple outputs is called Multiple Constant Multiplication.

Multiplication is the process of shifting and addition operation. Constant multiplier consists of number of adders, subtractors and shifter according to the coefficient pair FIR filter output can be obtained by multiplication of input and impulse response. FIR filter has two forms one is direct form and transposed form. Multiplication operation takes place in multiplier block. In transposed form multiplier blocks in FIR filter will replace by MCM architecture also known as shift and add architecture. FIR filter gives guaranteed feed forward, stable and linear phase response.

[1] Assistant Professor, SRM University,
[2] M.Tech VLSI Design, SRM University,
[3] Professor, VIT University.

For FIR filter impulse response is equal to the number of coefficients. But it is not the case in Infinite Impulse Response filters. Hence this FIR filter implementation is sometimes called as multiplierless digit based recoding method. The complexity of the FIR filter design is dominated by the multiplication of filter coefficients by the time-shifted versions of the filter input, i.e., the constant array-vector multiplication block in the direct form of Fig. 1(a) or by the multiplication of filter coefficients by the filter input, and the multiple constant multiplications block is shown in Fig. 1(b).

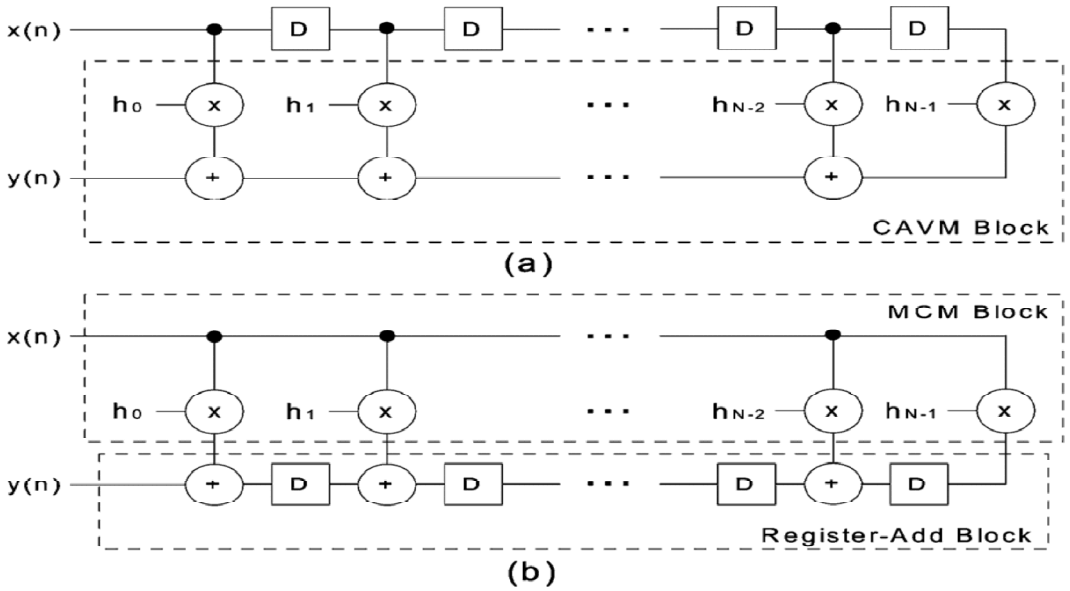

Figure 1: Different forms of an -tap FIR filter: (a) direct (b) transposed

1.1. Objective

Main objective is to eliminate multiplier block and introducing Multiple Constant Multiplication architecture in digit serial FIR filter and the reduction of multiplication in the form of shift and add operations.

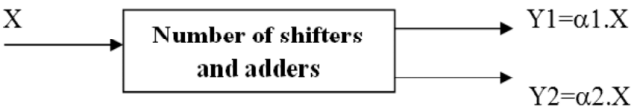

Figure 1.1: MCM operation

In Fig.1 X denotes input, $\alpha 1$ and $\alpha 2$ are filter coefficients, Y1 and Y2 are the outputs.

II. EXISTING METHOD

The existing MCM algorithms can be divided into four general classes:

i. Digit-based recording;
ii. Common sub expression elimination
iii. Graph-based algorithms

Digit-based recoding: It includes simple methods like CSD and the binary method. They generate the decomposition directly from the digit representation of the constant. Digit based recording methods are the fastest and the worst performing however, a recent approach uses different numbers systems to yield considerably better solutions. The main advantage of digit-based recording is their low computational cost, typically linear in the number of bits. Consequence, these methods can be easily applied to constants with

thousands of bits. For their shift-adds designs, the digit-based recording technique first defines the constants under a number representation, e.g., binary or canonical signed digit. Second, for the nonzero digits in the representations of constants it shifts the variables according to the digit positions and adds/subtracts the shifted variables with respect to the digit values. As an example, consider h0=21and h1=53 and suppose that the CSD representation is used. The decomposition of the linear transform y=21x0+53x1 as follows.

$$\begin{aligned} y &= 21x_0 + 53x_1 \\ &= (10101)_{CSD}\, x_0 + (10\bar{1}0101)_{CSD}\, x_1 \\ &= x_0 << 4 + x_0 << 2 + x_0 + x_1 << 6 - x_1 << 4 + x_1 << 2 + x_1 \end{aligned} \quad (1)$$

Where 6 operations are required for this CAVM block as shown infig2(a) and 5 operations in fig. 2(b).

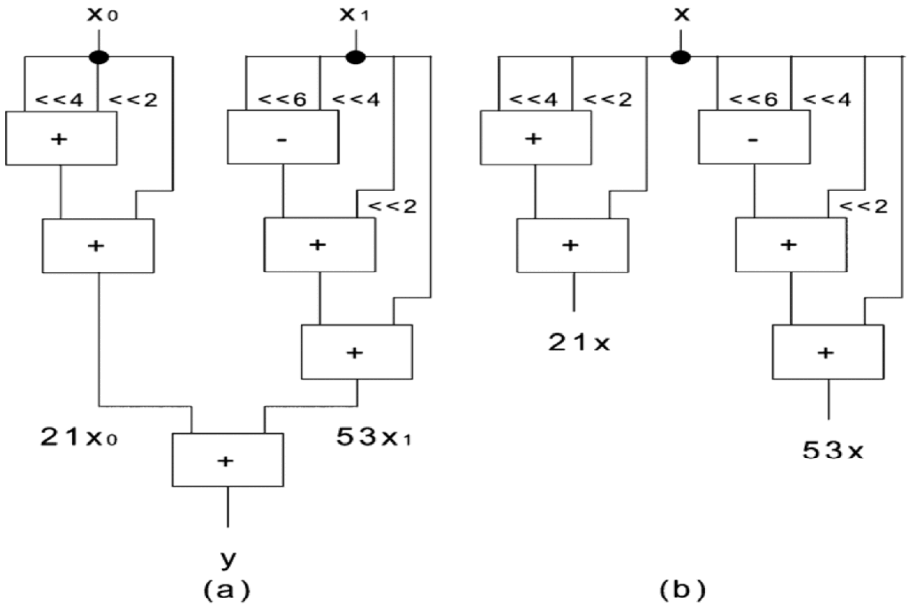

Figure 2: Constant multiplications using the DBR technique (a) 21x0+53x1 (b) 21x0 and 53x1

Common sub expression elimination algorithms: are direct descendants of digit-based recoding methods. The basic idea is to find common sub patterns in the representations of the constants after the constants are converted to a convenient number system such as CSD. Examples for this method include. The disadvantage, however, is that the performance of these algorithms depends on the number representation. Further, even though the considered CSE problem is NP-complete Further, even though the considered CSE problem is NP-complete its optimal solution does in general not provide the optimal MCM solution.

The CSE methods initially define the constants under a particular number representation. Then, they consider possible sub expressions, that can be extracted from the nonzero digits in the constant representations, and choose the “best” sub expression, generally the most common, to be shared among the constant multiplications .Their main drawback is their dependency on a number representation.For our MCM example in Fig. 2(b), the exact CSE algorithm obtains a minimum solution with 4 operations by finding the most common sub expression 5x= (101) csdx.

Graph-based algorithms: are bottom-up methods that iteratively construct the graph representing the multiplier block. The graph construction is guided by a heuristic that determines the next graph vertex to add to the graph.Graph-based algorithms offer more degrees of freedom by not being restricted to a particular representation of the coefficients, or a predefined graph topology.The GB methods are not restricted to any particular number representation and aim to find intermediate sub expressions that enable the realization of

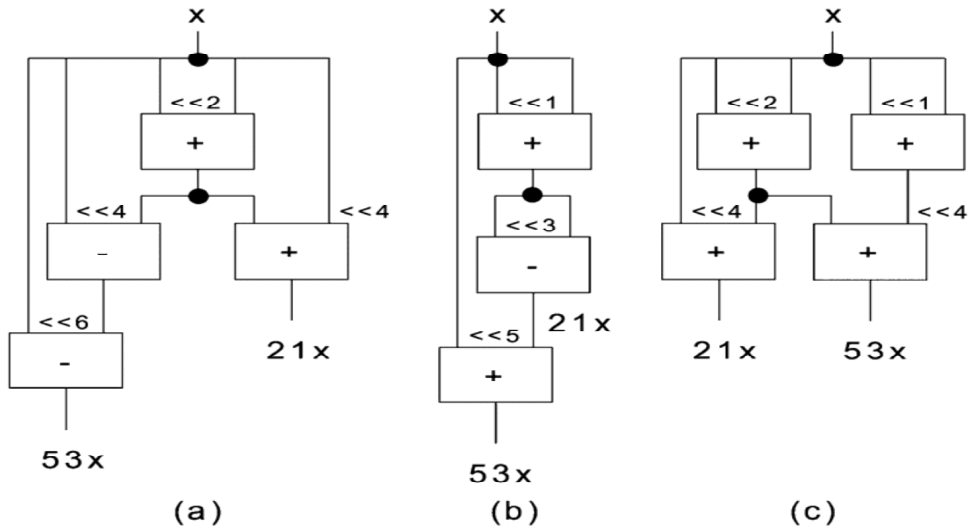

Figure 3: Constant multiplications (a) exact CSE algorithm (b) exact GB algorithm (c) approximate GB algorithm modified to handle a delay constraint

constant multiplications with the minimum number of operations. They consider a larger number of realizations of a constant and obtain better solutions than the CSE methods, but require more computational resources due to a larger search space. The approximate algorithm modified to handle a delay constraint finds a solution with 4 operations.

III. PROPOSED METHOD

Multiplier less Design of the CAVM Operation:

The algorithm called ECHO, consists of two main parts. In its first part, the shift-adds realizations of constants in the CAVM operation are found using an MCM algorithm. In its second part, the constants in the linear transform are replaced with their realizations in the MCM solution and the common sub expressions are extracted iteratively using a set of transformations. ECHO has two variations, ECHO-A and ECHO-D, that target the optimization of area and delay of the CAVM operation, respectively. ECHO-A uses the exact MCM algorithm and considers some area optimizations .ECHO-D is equipped with the approximate MCM algorithm modified to handle a delay constraint and considers some delay optimizations. Algorithms ensure to obtain a solution.

For our CAVM example in Fig. 2(a), ECHO-A finds a solution with 4 operations and 4 adder-steps (Fig. 4(a)) that was obtained based on the MCM solution in Fig. 3(b). Also, the solution of echo-d includes 5 operations and 3 adder-steps (Fig. 4(b)) that was obtained based on the MCM solution in Fig. 3(c). Then example shown in the direct impact of the MCM solution on the number of operations and adder-steps of the CAVM design. The minimum adder-steps of both design can be obtained. The approximate algorithm modified to handle a delay constraint finds a solution with 4 operations. The solution of the exact GB algorithm in Fig. 3(b), its solution has one more operation, but one less adder-step.GB algorithm can be applied for any coefficient pair combinations. Hence Graph Based algorithm is used to the number of operation is reduced drastically than other algorithms. Graph based requires computational resource due to large searchspace.

IV. SIMULATION RESULTS

The design proposed in this paper has been developed using model simulator tool.

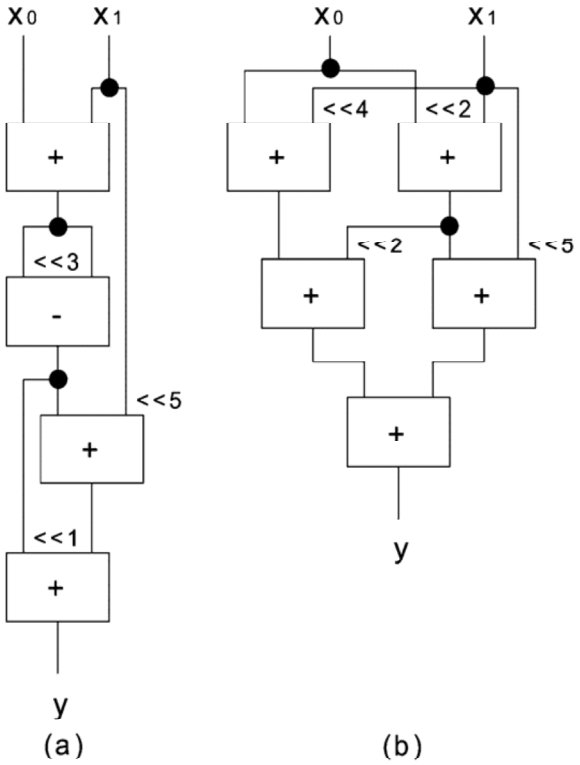

Figure 4: Shift-adds design of (a) ECHO-A (b) ECHO-D

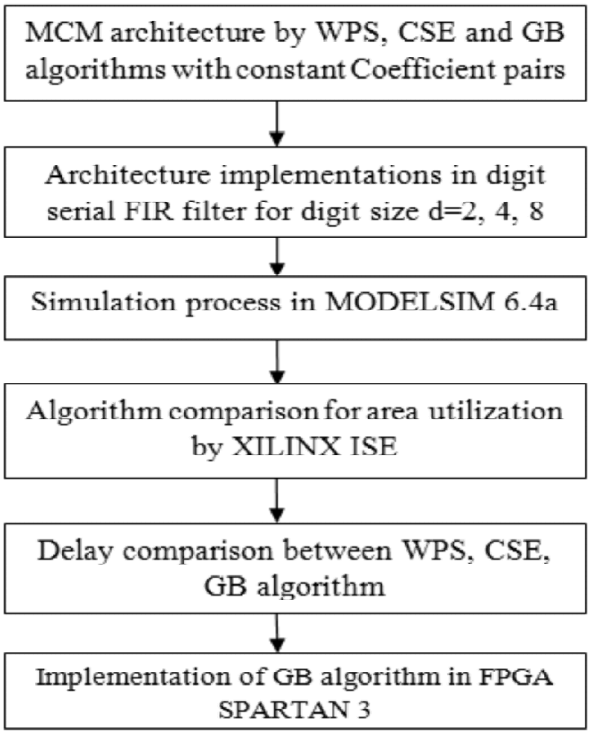

Figure 5: Flow map for proposed design

Table 1
Comparsion of Algorithms

Technique	*Area Comparison*	*Delay Comparison*
Fir with Dbr	542	11.773 Ns
Fir with Exact Cse	542	11.773 Ns
Fir with Echo-a	346	11.698 Ns

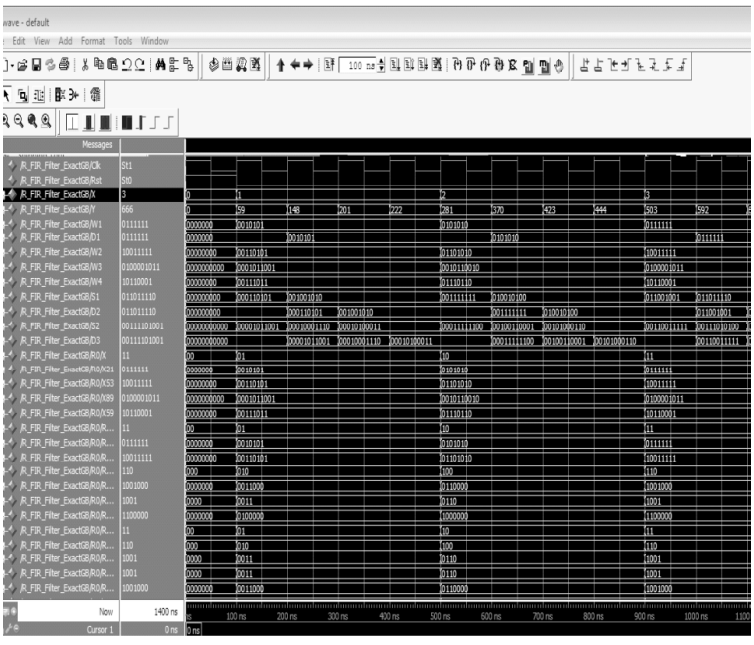

Figure 6: Output of FIR FILTER USING DIGIT BASED RECORDING

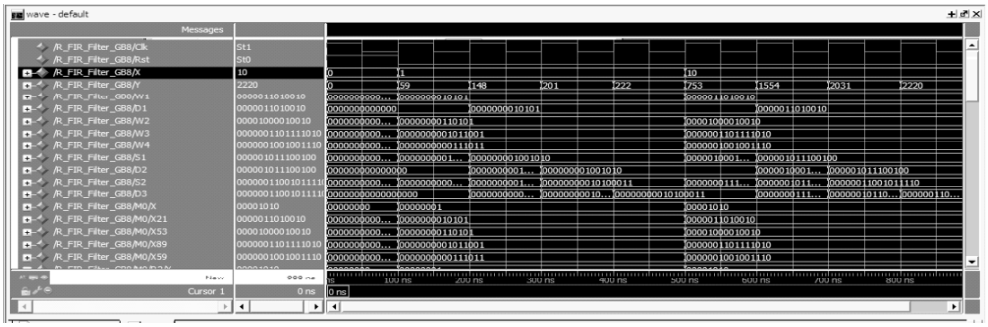

Figure 7: Output of FIR FILTER USING CS Ealgorithm

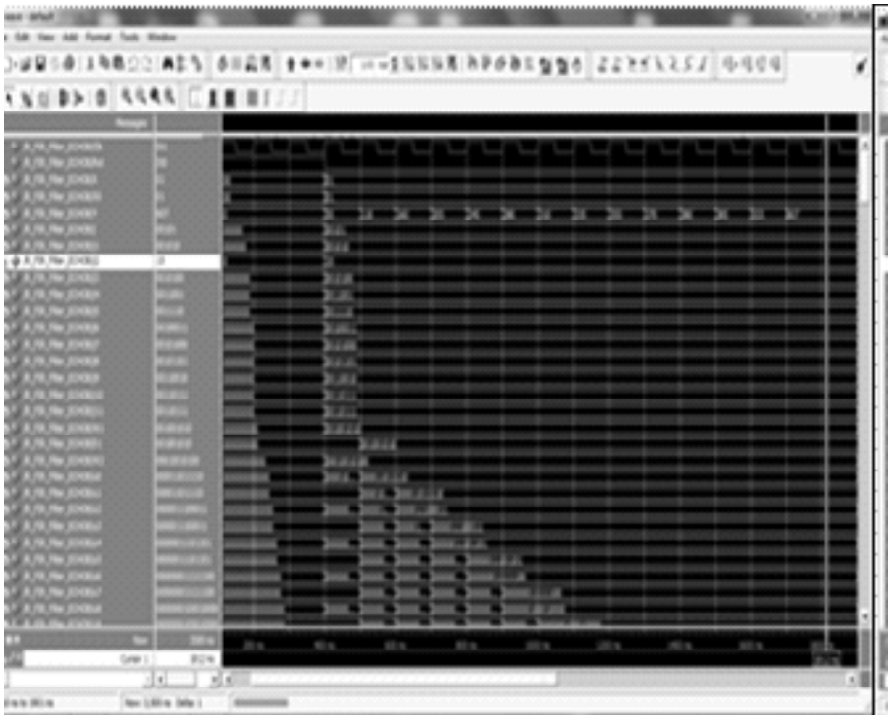

Figure 8: Output of FIR FILTER USING ECHO-AREA

V. CONCLSUION

Thus the implementation of digit serial FIR filter was implemented with low complexity MCM architectures . Device utilization and delay values are compared for hardware implementation. Hence this MCM approach drastically reduces the system complexity, area and delay and FPGA hardware real time implementation has performed with spartan3 version. Future enhancement of this paper is to design MCM architecture with more coefficient pairs for FIR filter implementation

REFERENCE

[1] Kenny Johansson, Oscar Gustafsson, Andrew G. D., and Lars Wanhammar, “Algorithm to reduce the number of shifts and additions in multiplier blocks using serial arithmetic” IEEE MELECON, pp. 197-200, 2004.

[2] Levent Aksoy, Cristiano Lazzari, Eduardo Costa,Paulo Flores, José Monteiro., “Efficient shift-adds design of digit-serial multiple constant multiplications” GLSVLSI’11,2011.

[3] Levent Aksoy, Cristiano Lazzari Eduardo Costa,Paulo Flores, José Monteiro, “Design of digit-serial FIR filters: algorithms, architectures, and a CAD tool” IEEE Trans. on Very Large Scale Integration (VLSI) Systems, Vol. 21, No. 3, pp 498-511, 2013.

[4] Levent Aksoy, Eduardo.D.Costa, Paulo Flores, José Monteiro., "Exact and approximate algorithms for the optimization of area and delay in multiple constant multiplications" IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 27, No. 6, pp. 1013-1026, 2008.

[5] Miodrag potkonjak, Mani.B.S., Anantha.P.C.,"Multiple constant multiplications efficient and versatile framework and algorithms for exploring common subexpression elimination" IEEE Trans. Computer Aided-Design of Integrated Circuits and Systems, VOL.15,NO.2, pp 151-165, 1996.

[6] Yuen H.A.H., Chi U.L., Hing-K.K.,Ngai Wong, "Global optimization of common subexpressions for multiplierless synthesis of multiple constant multiplications" IEEE Explore,pp.119-124, 2008.

[7] R. Hartley, "Subexpression sharing in filters using canonic signed digit multipliers," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 43, no. 10,pp. 677–688, Oct. 1996.

[8] I.-C. Park and H.-J. Kang, "Digital filter synthesis based on minimal signed digit representation," in Proc. DAC, pp. 468–473, 2001.

[9] A. Dempster, M. Macleod, "Use of minimum-adder multiplier blocks in FIR digital filters," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 42, no. 9, pp. 569–577, Sep. 1995.

[10] L. Aksoy, C. Lazzari, E. Costa, P. Flores, and J. Monteiro, "Efficient shift-adds design of digit-serial multiple constant multiplications," in *Proc. Great Lakes Symp. VLSI*, 2011, pp. 61–66.

[11] P. Flores, J. Monteiro, and E. Costa, "An exact algorithm for the maximal sharing of partial terms in multiple constant multiplications," in *Proc. Int. Conf. Comput.-Aided Design*, Nov. 2005, pp. 13–16.