I J C T A, 10(8), 2017, pp. 543-551 ISSN: 0974-5572

Design and Simulation of 16 Bit Vedic Multiplier using Urdhva Tiryakbhyam Algorithm

Aditya Agarwal[1], Jay Prakash Narayan Verma[2] and Nishant Srivastava[3]

ABSTRACT

It is an old strategy of Indian science as it contains SUTRAS (formulae). A fast complex 16*16 multiplier outline by utilizing Urdhva Tiryakbhyam sutra is displayed in this paper. By utilizing this sutra the incomplete items and wholes are produced in one stage which decreases the configuration of design in processors. By utilizing this sutra we can decrease the time with high degree when contrast with cluster and corner multiplier. It can be executed in numerous Digital Signal Processing (DSP) applications, for example, convolution, Fast Fourier Transform (FFT) separating and in chip. By utilizing this strategy we decrease the spread postponement in examination with cluster based design and parallel snake based execution which are most usually utilized models .The principle parameters of this paper is proliferation deferral and element power utilization were figured and discovered diminished.

Catchphrases Booth multiplier, FFT, DSP, engendering delay.

1. INTRODUCTION

Augmentation is a basic capacity in number-crunching operations in view of this operations, for example, Multiply and Accumulate (MAC) and internal item are among a portion of the oftentimes utilized Computation-Intensive Arithmetic Functions (CIAF) presently actualized in numerous Digital Signal Processing (DSP) applications, for example, convolution, Fast Fourier Transform (FFT), separating and in chip in its number juggling and rationale unit. Since duplication overwhelms the execution time of most DSP calculations, so there is a need of fast multiplier. Right now, increase time is still the prevailing variable in deciding the direction process duration of a DSP chip. The interest for fast preparing has been expanding as an aftereffect of extending PC and sign handling applications.

Higher throughput number juggling operations are vital to accomplish the fancied execution in some constant flag and picture preparing applications. One of the key math operations in such applications is increase and the advancement of quick multiplier circuit has been a subject of enthusiasm over decades. Decreasing the time defers and control utilization are extremely vital necessities for some applications. This work presents diverse multiplier designs.

In this paper a straightforward 16 bit advanced multiplier is proposed which depends on Urdhva Tiryakbhyam (Vertically and Crosswise) Sutra of the Vedic Math's. Two twofold numbers (16-bit each) are increased with this Sutra. The principle idea of this paper is that the force utilization of the circuit and spread deferral of the proposed design.

2. VEDIC MULTIPLICATION TECHNIQUE

The utilization of Vedic arithmetic is to lessen the common computations in traditional science to extremely straightforward one. Since the Vedic formulae are guaranteed to be founded on the characteristic standards

[1-3] Assistant Professor, Department of Electronics and Communication Engineering, SRM University, *Emails: aditya.a@ncr.srmuniv.ac.in, jayprakashnarayan.v@ncr.srmuniv.ac.in*

on which the human personality works. Vedic Mathematics is a technique of number-crunching decides that permit more proficient rate execution. It likewise gives some successful calculations which can be connected to different branches of building, for example, processing.

2.1. Urdhva Tiryakbhyam Sutra

The proposed Vedic multiplier depends on the "Urdhva Tiryagbhyam" sutra (calculation). These Sutras have been customarily utilized for the augmentation of two numbers in the decimal number framework. In this work, we apply the same thoughts to the parallel number framework to make the proposed calculation good with the computerized equipment.[3] It is a general increase recipe pertinent to all instances of duplication. It truly signifies "Vertically and crosswise".

It depends on a novel idea through which the era of every halfway item should be possible with the simultaneous expansion of these incomplete items. The calculation can be summed up for n x n bit number.[5] Since the fractional items and their entireties are figured in parallel and the multiplier is free of the clock recurrence of the processor. Because of its standard structure, it can be effortlessly format in chip and fashioners can without much of a stretch bypass these issues to stay away from cataclysmic gadget disappointments. The preparing force of multiplier can without much of a stretch be expanded by expanding the info and yield information transport widths since it has an a significant consistent structure. Because of its general structure, it can be effortlessly design in a silicon chip. The Multiplier taking into account this sutra has the favorable position that as the quantity of bits expands, door postponement and zone increments gradually when contrasted with other customary multipliers.

2.2. Multiplication of two decimal numbers 252 × 846

To represent this plan, let us consider the duplication of two decimal numbers 252 x 846 by Urdhva Tiryakbhyam strategy as appeared in Fig. The digits on the both sides of the line are duplicated and included with the convey from the past stride. This produces one of the bits of the outcome and convey. This conveys

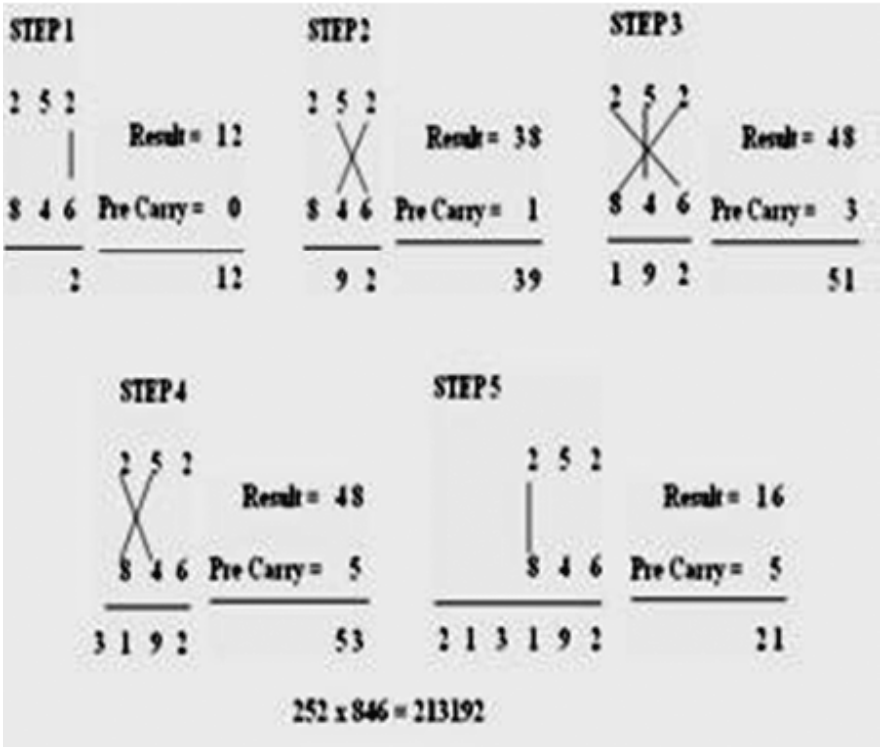


Figure 1: Multiplication of Two Decimal Numbers 252 *846

is included the following stride and henceforth the procedure go on. On the off chance that more than one line are there in one stage, every one of the outcomes are added to the past convey. In every progression, minimum critical piece goes about as the outcome bit and every other piece go about as convey for the following stride. At first the convey is taken to be zero.

3. THE PROPOSED MULTIPLIER ARCHITECTURE

The equipment engineering of 2 × 2, 4 × 4 and 8 × 8 piece Vedic multiplier module are shown in the underneath areas. Here, "Urdhva-Tiryagbhyam" (Vertically and Crosswise) sutra is utilized to propose such design for the increase of two twofold numbers. The magnificence of Vedic multiplier is that halfway item era and augmentations are done simultaneously. Thus, it is very much adjusted to parallel handling. The component makes it more appealing for paired increases. This thusly decreases delay, which is the essential inspiration driving this work.

3.1. Vedic Multiplier for 2 × 2 bit Module

The technique is clarified underneath for two, 2 bit numbers An and B where A = a1a0 and B = b1b0 as appeared in Fig. Firstly, the minimum noteworthy bits are increased which gives the slightest critical piece of the last item (vertical). At that point, the LSB of the multiplicand is duplicated with the following higher piece of the multiplier and included with, the result of LSB of multiplier and next higher piece of the multiplicand (across). The entirety gives second piece of the last item and the convey is included with the halfway item gotten by duplicating the most noteworthy bits to give the whole and convey. The total is the third comparing bit and conveys turns into the fourth piece of the last item

$$s0 = a0b0; \quad (1)$$

$$c1s1 = a1b0 + a0b1; \quad (2)$$

$$c2s2 = c1 + a1b1; \quad (3)$$

The final result will be c2s2s1s0. This multiplication method is applicable for all the cases.

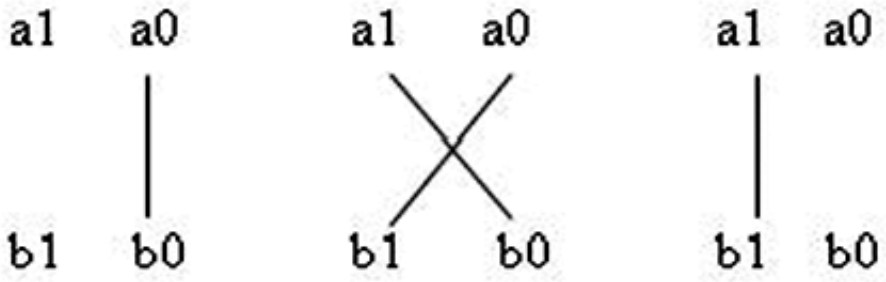


Figure 2: The Vedic Multiplication Method for Two 2 Bit Binary Numbers

The 2 × 2 Vedic multiplier module is executed utilizing four information AND doors and two half-adders which is shown in its square graph in Fig. It is found that the equipment engineering of 2 × 2 piece Vedic multiplier is same as the equipment design of 2 × 2 piece traditional Array Multiplier .Hence it is reasoned that augmentation of 2 bit parallel numbers by Vedic strategy does not made huge impact in change of the multiplier's productivity.

Precisely we can express that the aggregate postponement is just 2-half viper delays, after definite piece items are produced, which is fundamentally the same as Array multiplier. So we change over to the execution of 4 × 4 piece Vedic multiplier which utilizes the 2 × 2 piece multiplier as an essential building square. The same technique can be reached out for information bits 4 and 8. Be that as it may, for higher no. of bits in information, little alteration is required.

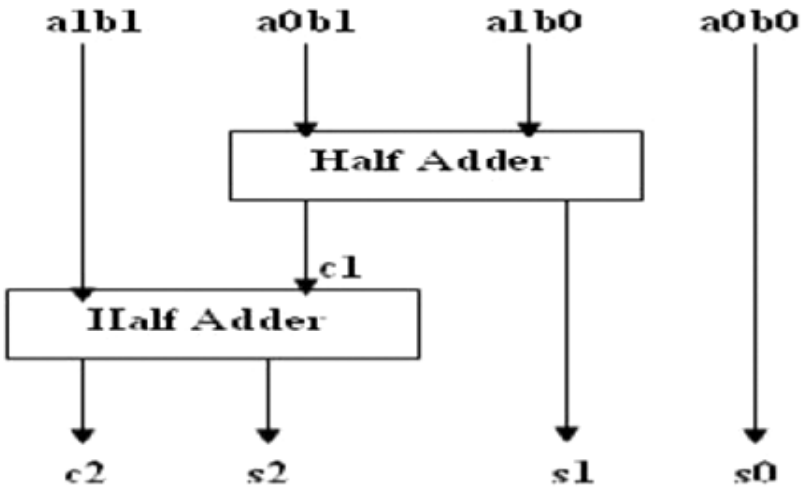


Figure 3: Block Diagram of 2 × 2 Bit Vedic Multiplier

3.2. Vedic Multiplier for 4 × 4 bit Module

The 4 × 4 piece Vedic multiplier module is executed utilizing four 2 × 2 piece Vedic multiplier modules as talked about in Fig. 3

How about we dissect 4x4 increases, say A = A3 A2 A1 A0 and B = B3 B2 B1 B0. The yield line for the duplication result is – S7 S6 S5 S4 S3 S2 S1 S0. Let's partition An and B into two sections, say A3A2 and A1 A0 for An and B3 B2 and B1B0 for B. Utilizing the principal of Vedic increase, taking good for nothing at once and utilizing 2 bit multiplier square, we can have the accompanying structure for duplication as appeared in Fig. 4.

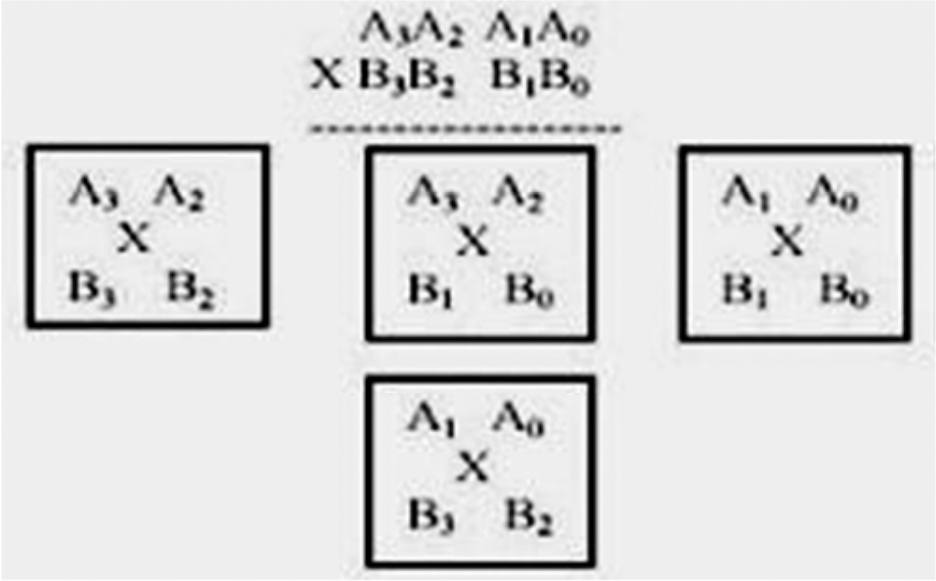


Figure 4: Sample Presentation For 4 × 4 Bit Vedic Multiplication

Every square as appeared above is 2 × 2 piece vedic multiplier. Initial 2 × 2 piece multiplier inputs are A1A0 and B1B0. The last square is 2 × 2 piece multiplier with inputs A3 A2 and B3 B2. The center one shows two 2 × 2 piece multiplier with inputs A3 A2 and B1B0 and A1A0 and B3 B2. So the last after effect of duplication, which is of 8 bit, S7 S6 S5 S4 S3 S2 S1 S0. To comprehend the idea, the Block graph of 4 × 4 piece Vedic multiplier is appeared in Fig. 4. To get last item (S7 S6 S5 S4 S3 S2 S1 S0), four 2 × 2 piece Vedic multiplier (Fig. 2) and three 4-bit Ripple-Carry (RC) Adders are required. The proposed Vedic

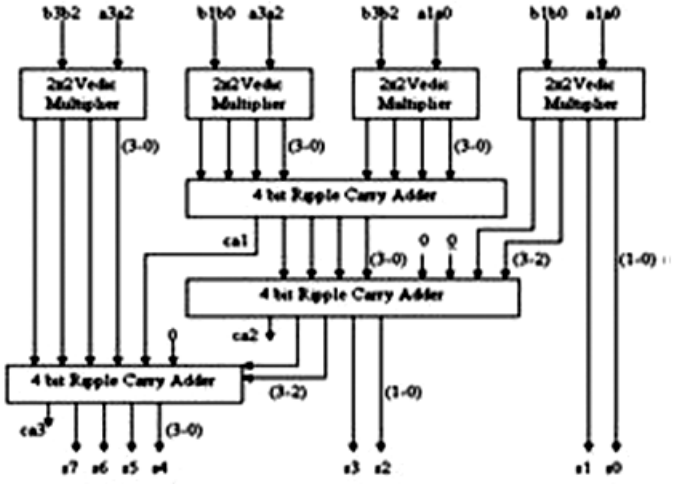


Figure 5: Block Diagram of 4*4 bit Vedic Multiplier

multiplier can be utilized to lessen delay. Early writing talks about Vedic multipliers in light of exhibit multiplier structures. Then again, we proposed engineering, which is effective as far as rate. The courses of action of swell convey Adders appeared helps us to lessen delay and 8 × 8 Vedic multiplier modules are executed effectively by utilizing four 4 × 4 multiplier modules.

3.3. Vedic Multiplier for 8 × 8 bit Module

The 8 × 8 bit Vedic multiplier module as appeared in the square graph in Fig. 6 can be effectively executed by utilizing four 4 × 4 piece Vedic multiplier modules as talked about in the past segment. How about we break down 8 × 8 augmentations, say A = A7 A6 A5 A4A3 A2 A1 A0 and B = B7 B6 B5 B4 B3 B2 B1 B0. The yield line for the increase result will be of 16 bits as – S15 S14 S13 S12 S11 S10 S9 S8 S7 S6 S5 S4 S3 S2 S1 S0. How about we partition A and B into two sections, say the 8 bit multiplicand A can be deteriorated into pair of 4 bits AH-AL.

Likewise multiplicand B can be decayed into BH-BL. The 16 bit item can be composed as: P = A × B = (AH-AL) × (BH-BL) = AH × BH + (AH × BL + AL × BH) + AL × BL Using the principal of Vedic

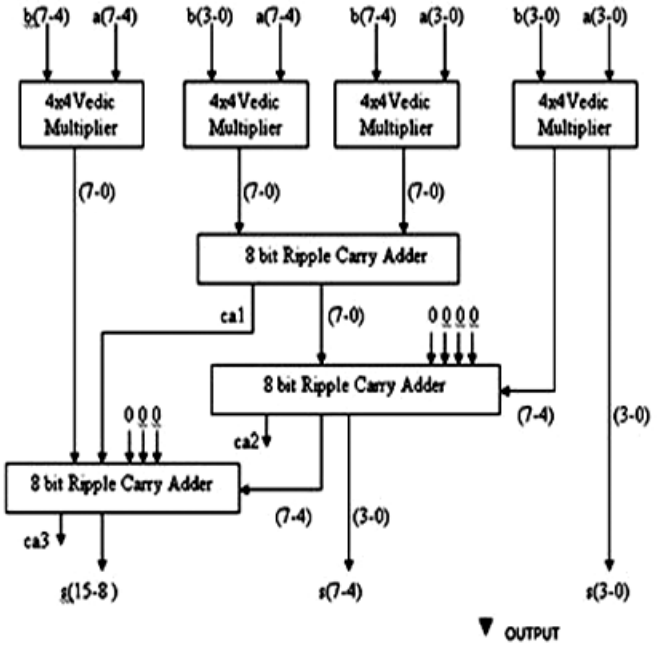


Figure 6: Block Diagram of 8 × 8 Bit Vedic Multiplier

augmentation, taking four bits at once and utilizing 4 bit multiplier hinder as examined we can play out the duplication. The yields of 4 × 4 piece multipliers are added as needs be to acquire the last item. Here aggregate three 8 bit Ripple-Carry Adders are required as appeared in Fig. 6.

3.4. Vedic Multiplier for 16x16 bit Module

The configuration of 16 × 16 piece is a comparable course of action of 8 × 8 squares in a streamlined way. The initial phase in the outline of 16 × 16 piece will amass the 8 bit (byte) of every 16 bit information. These lower and upper bytes sets of two inputs will frame vertical and across item terms. Every info byte is taken care of by a different 8 × 8 Vedic multiplier to create sixteen fractional item pushes. These fractional items lines are included a 16-bit convey look ahead snake ideally to create last item bits. The schematic of a 16 × 16 piece composed utilizing 8 × 8 squares. The fractional items speak to the Urdhva vertical and cross item terms. At that point utilizing or and half snake get together to locate the last item. Power dissemination of this multiplier is 0.18mW and spread postponement is 16ns.[8]

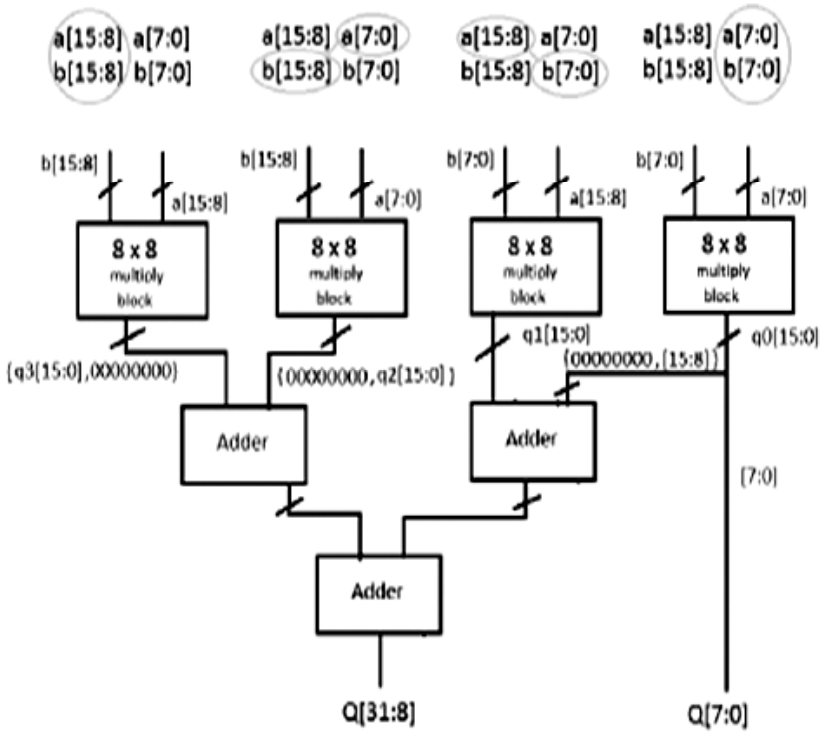


Figure 7: Block Diagram Of 16 × 16 Bit Vedic Multiplier

4. IMPLEMENTATION IN XILINX 13.2

In this work, 16 × 16 bit Vedic multiplier is composed in Verilog (Very High Speed Integrated Circuits Hardware Description Language). Rationale combination and recreation was done in XilinxISE13.2i - Project Navigator and ISim test system incorporated in the Xilinx bundle. The execution of circuit is assessed on the Xilinx gadget family Spartan3, bundle vq100 and speed grade - 4. The RTL schematic of 16 × 16 piece Vedic multiplier in Fig. 8.

"vedic_multi_struct16 × 16" contains four 8 × 8 piece Vedic multiplier "vedic_multi_struct4 × 4_1" - vm1, vm2, vm3, vm4 and three 7-bit Ripple Carry Adder "rc_adder_8" - r1, r2, r3 has appeared in Fig. while the reproduction results got are appeared. In behavioral reenactment we have tried for the accompanying information bits: a) For 16 × 16 piece Vedic multiplier include, the multiplier a=" 1111000011110000" (decimal number framework) and multiplicand b="0000111100001111" (decimal number framework) and we get 16-bit yield p="00000111000101100001011100001000" (decimal number framework).

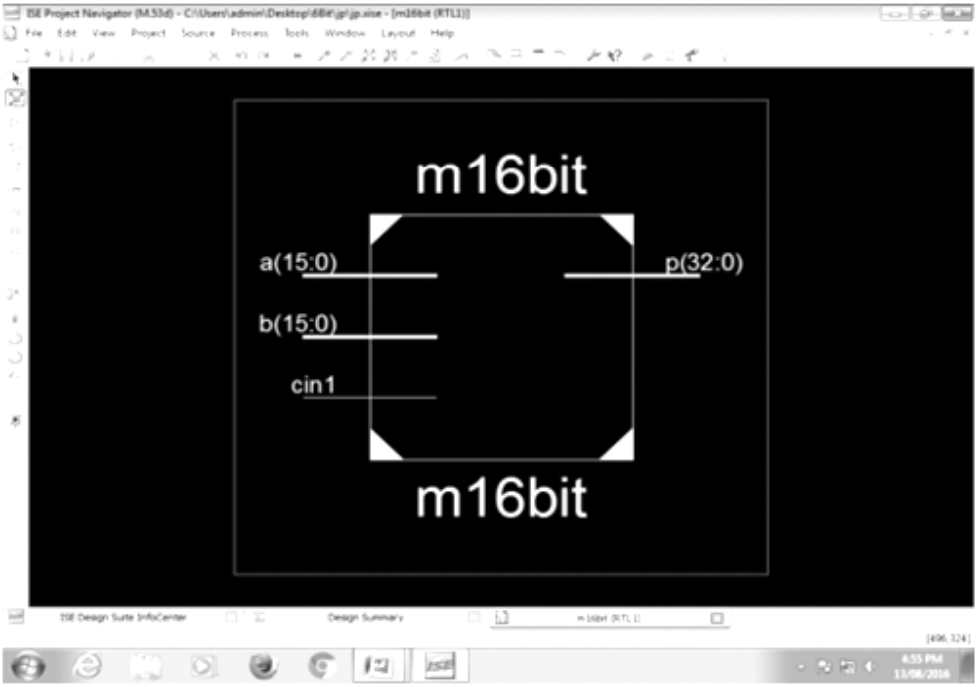


Figure 8: RTL Schematic of 16 × 16 Bit Vedic Multiplier

5. EXPERIMENTAL RESULT

Table 3 analyzes the consequence of Area, Delay speed and force of Booth and Urdhava Tiryakbhyam multiplier. The outcome demonstrates that Urdhava Tiryakbhyam multiplier is the best multiplier contrast with Booth multiplier regarding Area, defer and control utilizations.

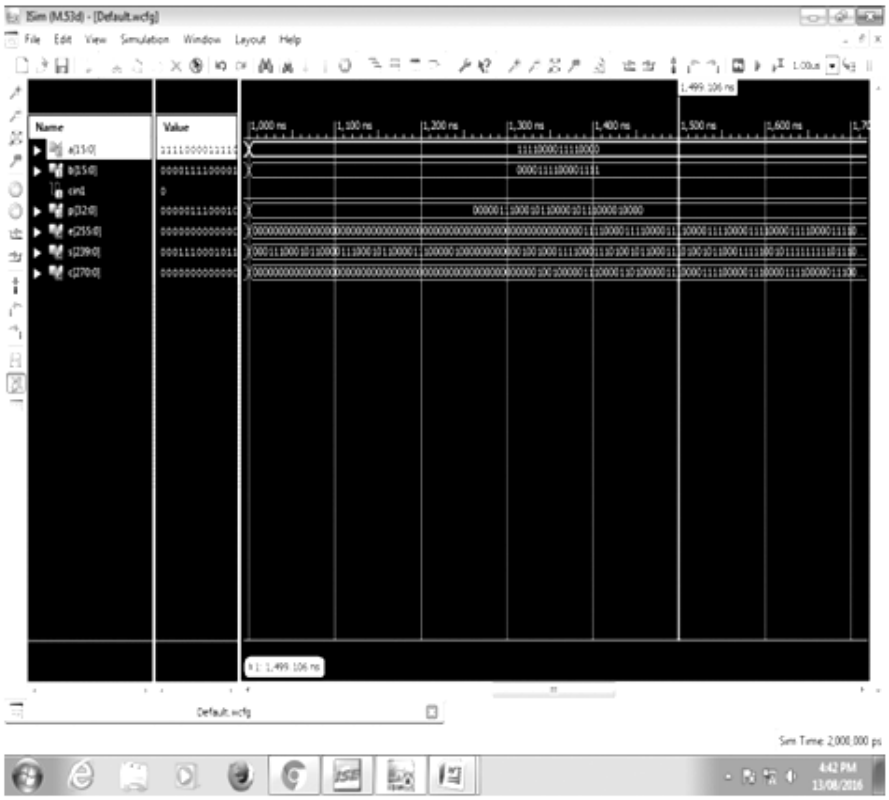
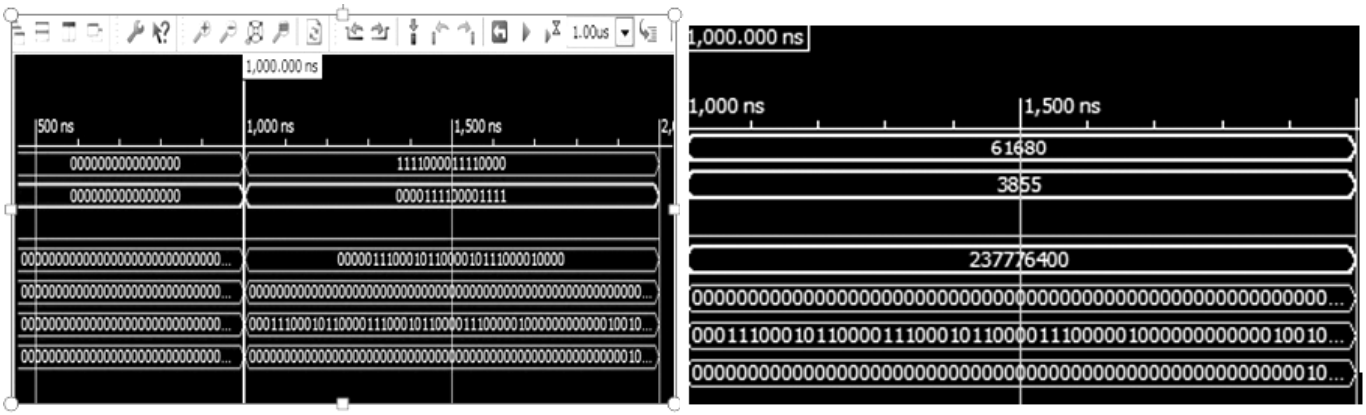


Figure 9: Simulation Result of 16x16 Bit Vedic Multiplier
(Xreg: 61680, Yreg: 3855, P: 237776400)



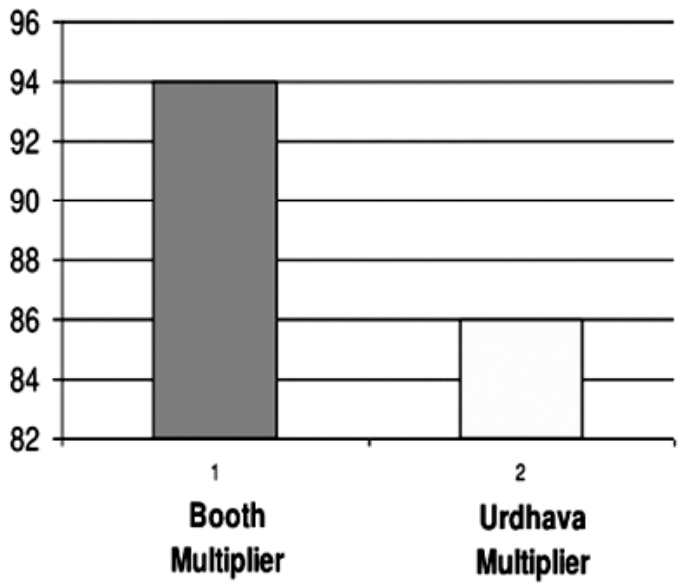


Figure 10: Area Comparisons for (16 × 16)

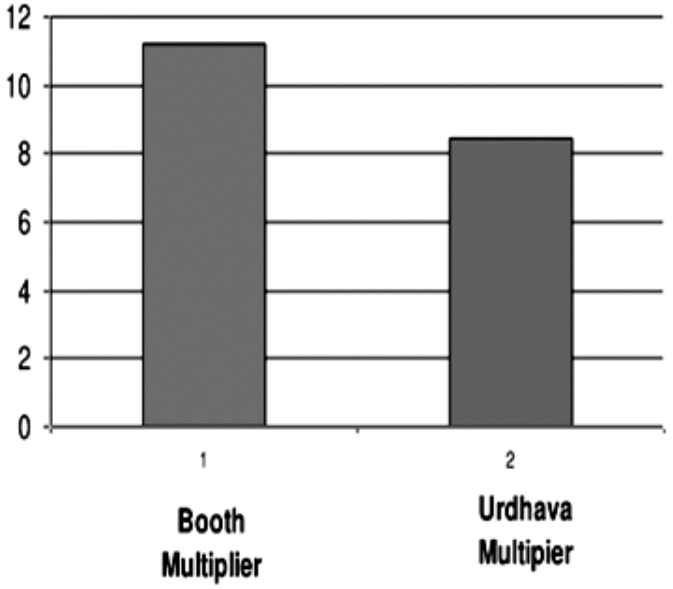


Figure 11: Delay Comparison for (16 × 16)

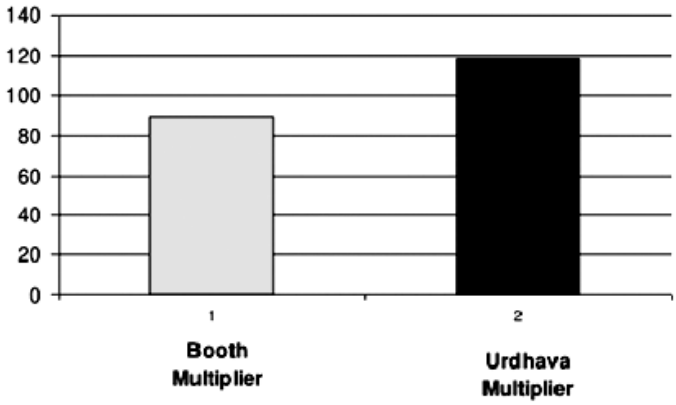


Figure 12: Speed Comparison for (16 × 16)

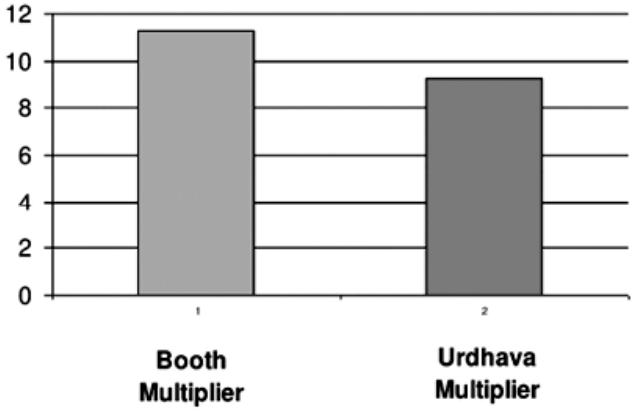


Figure 13: Power Comparison for (8 × 8)

6. CONCLUSION

In this paper, we give an account of a novel complex number multiplier outline in light of the recipes of the old Indian Vedic Mathematics, very appropriate for fast complex number-crunching circuits which are having wide application in VLSI and sign preparing. The usage was done in HDL and XILINX. This novel engineering consolidates the benefits of the Vedic science for increase which experiences the stages and halfway item lessening. The Delay of the proposed Vedic multiplier is 6.216ns and the force utilization is 0.027mW. It is clear from the synopsis that exclusive 203 rationale components are required for the proposed

Architecture. The upsides of this proposed engineering is proficient in rate and area (1ess assets utilized, for example, less number of multipliers and adders) and is Flexible in de outline.

REFERENCES

[1] Prakash Narchi, Siddalingesh S Kerur, Jayashree C Nidagundi, Harish M Kittur and Girish V A. Implementation of Vedic Multiplier for Digital Signal Processing. IJCA Proceedings on International Conference on VLSI, Communications and Instrumentation (ICVCI) (16):1–5, 2011. Published by Foundation of Computer Science.

[2] Sumit Vaidya and Deepak Dandekar. "Delay-power perfor-mance comparison of multipliers in VLSI circuit design". International Journal of Computer Networks & Communications (IJCNC), Vol. 2, No. 4, July 2010.

[3] H. Thapliyal and H.R Arbania. "Time- Area-Power Efficient Multiplier and Square Architecture Based On Ancient Indian Vedic Mathematics", Proceedings of the 2004 International Conference on VLSI (VLSI'04), Las Vegas, Nevada, June 2004, pp. 434-439.

[4] P. D. Chidgupkar and M. T. Karad, "The Implementation of Vedic Algorithms in Digital Signal Processing", Global J. of Engg. Edu, Vol.8, No.2, 2004, UICEE Published in Australia.

[5] Thapliyal H. and Srinivas M.B, "High Speed Efficient NxN Parallel Hierarchical Overlay Multiplier Architecture Based on Ancient Indian Vedic Mathematics", Transactions on Engineering, Computing and Technology, 2004, Vol.2.

[6] Harpreet Singh Dhillon and Abhijit Mitra, "A Reduced– Bit Multipliction Algorithm for Digital Arithmetics", International Journal of Computational and Mathematical Sciences 2.2 @ www.waset.orgSpring2008.

[7] Honey Durga Tiwari, Ganzorig Gankhuyag, Chan Mo Kim and Yong Beom Cho, "Multiplier design based on ancient Indian Vedic Mathematician", International SoC Design Conference, pp. 65-68, 2008.

[8] Parth Mehta and Dhanashri Gawali, "Conventional versus Vedic mathematics method for Hardware implementation of a multiplier", International conference on Advances in Computing, Control, and Telecommunication Technologies, p. 640

[9] Ramalatha, M.Dayalan, K D Dharani, P Priya, and S Deoborah, "High Speed Energy Efficient ALU Design using Vedic Multiplication Techniques", International Conference on Advances in Computational Tools for Engineering Applications (ACTEA) IEEE, pp. 600-603, July 15-17, 2009.

[10] Sumita Vaidya and Deepak Dandekar, "Delay- Power Performance comparison of Multipliers in VLSI Circuit Design", International Journal of Computer Networks & Communications (IJCNC), Vol. 2, No. 4, pp. 47-56, July 2010.

[11] S.S.Kerur, Prakash Narchi, Jayashree CN, Harish M Kittur and Girish V A "Implementation of Vedic Multiplier For Digital Signal Processing" International conference on VLSI communication & instrumentation (ICVCI), 2011.