An Algorithm for Directional Relay during Voltage Inversion

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Abstract: The proposed work highlights possible limitations of direction assessment of fault in series compensated line using current signal. The objective of this work is to estimate the fault direction in series compensated line. Solution is given based on difference of phase among fault and steady (i.e. pre-fault) current. Positive sequence component of current is estimated using Fast Fourier Transform. The approach deals with only current component, so it is time saving and computationally efficient. The proposed approach is verified through the simulated results obtained by PSCAD/EMTDC.

Keywords: Fault direction; FFT; Directional relay; Series compensation; Voltage inversion.

1. INTRODUCTION

Series compensations are applied to lines to reduce transmission line losses, improve power flow, better power system stabilization, and improved voltage control. Directional relay plays a prominent role for series transmission lines and may work in all faulty conditions. Fundamental frequency based directional relay is customarily utilized which assesses direction of power flow from the accessible voltage-current magnitude and phase. The difference between the angles of voltage and current is used for assessment of fault direction of a line. One can easily determine the fault direction by sequence components of voltage and currents (mainly positive and negative sequences).The fault current phasor normally lie in two separate regions depending on fault and pre-fault system conditions. At all faulty situation, the transmission line becomes capacitive and causes voltage inversion depending on system condition like fault type, fault resistance as well as fault location.

Voltage inversion is a practical problem in series compensated lines (SCLs). When fault occurs ahead of the capacitor then relay voltage may lag the current by approximately 90°. Conventional directional relay is unable to identify the fault direction during this situation.

H. Gao *et al.* [1] present a new fault direction estimation technique for extra high voltage transmission lines. John Horak *et al.* [2] give directional over current relaying concepts to decide direction of fault using the voltage and current phase relationship. H. Gao *et al.* [3] provide positive-sequence fault components based novel fault direction algorithm for EHV transmission lines. Bin Su *et al.* [4] present the positive sequence super-imposed components based fault detection technique for symmetrical fault during power Swing. A.K. Pradhan *et al.* [5] present a fault direction estimation scheme for estimating the direction of fault.

A. K. Pradhan *et al.* [6] proposed a technique for low-voltage circumstances when close-in fault in directional relaying by utilizing the direction of power flow. P. Jena *et al.* [7] proposed a better scheme for

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protection of bus-bar derived from difference between positive sequence current of input and output line of a CT. Fuzzy logic approach based a fault detection scheme is proposed by P. Jena *et al.* [8] to handle power swing. A new solution is proposed by P. Jena *et al.* for fault direction assessment for series compensated line [9]. P. K. Nayak *et al.* present a novel negative sequence current based fault identification method during power swing [10].

A. Ukil et al. highlighted a novel current-only fault detection possibility. Discrete Fourier transform (DFT), Kalman filter is used for determine the direction [11]. A Directional relaying algorithm based on multi-criteria fuzzy logic is suggested for double-circuit line protection by P. Jena *et al.* [12]. Monalisa Biswal et al. present a fault direction detection technique based on voting technique [13]-[14]. LS algorithm modeled with current and voltage issued for phasor estimation by M. Biswal [15].

A new fault direction estimation scheme for a line with TCSC is proposed by P. Jena *et al.* [16]. P. Jena *et al.* [17] presented a fault direction estimation algorithm based on negative sequence current phase change for single pole tripping. Positive sequence superimposed components can also be used to build directional relay algorithm as shown by Bin Guo *et al.* [18]. Saptarshi Roy *et al.* [19] proposed a new method for detection, classification and locating the fault and also estimated the zone using negative sequence current. An innovative method is introduced for fault detection of transmission and distribution networks by A. Jalilian *et al.* [20]. The proposed scheme employs only the post fault current. Therefore, it is more efficient than other directional relaying schemes used for detection of fault using voltage or pre-fault current.

The problems with the capacitor bank allocation in transmission line may be described as follows: Over and under reach, system transients, voltage and current inversion etc. In compensated system relay senses the fault in opposite sides of a protected transmission line during voltage inversion. Current inversion is also occurred in SCLs. In most of the cases (internal faults) the fault for an equivalent system, one side is capacitive and inductive in another side.

Available literature clearly signifies that numerous fault direction estimation schemes have been proposed for compensated and uncompensated power system networks. But relatively little work has been done using Fast Fourier Transform (FFT) for detection of fault direction in case of series compensated system.

This paper focuses on voltage inversion problem related to directional relaying and come up with an alternative solution where FFT is utilized for finding the sequence component of system. In Section 2 problems regarding directional relaying are discussed in detail. Here, $\Delta\varnothing$ (difference of phase among fault and steady (i.e. pre-fault) positive sequence current (PSC) to find the direction of fault and only current signal is used for detecting the fault without considering the voltage signal. The method is verified using PSCAD/EMTDC simulated data for a series compensated system placing capacitor in different locations [9]. In Section 4 results are discussed with the above issue. Section 5 concludes the paper.

2. PROBLEM STATEMENT

The inductive reactance and the capacitive reactance are the main causes of voltage inversion at a relay bus. The relay misunderstands fault to be in reverse direction of a protected transmission line due to voltage inversion.
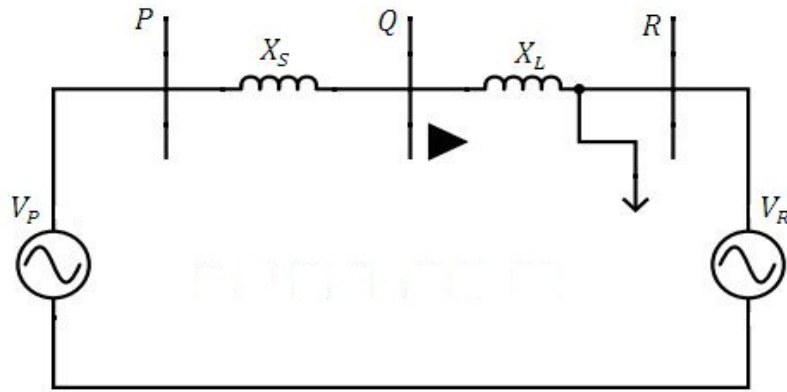
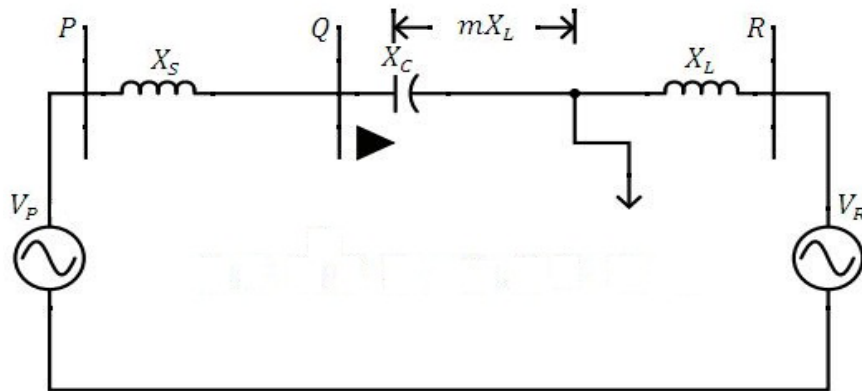**Figure 1: Uncompensated system considering reactance components**

Figure 2: Compensated system considering reactance components

The necessary conditions for inversion of relay voltage at relay bus are given below [21]:

$$X_C \geq mX_L \text{ and } mX_L + X_S \geq X_C \tag{1}$$

where X_C X_c is the line capacitance, X_L and X_S are the inductive reactance of source R and source P respectively, and m is the fault location.
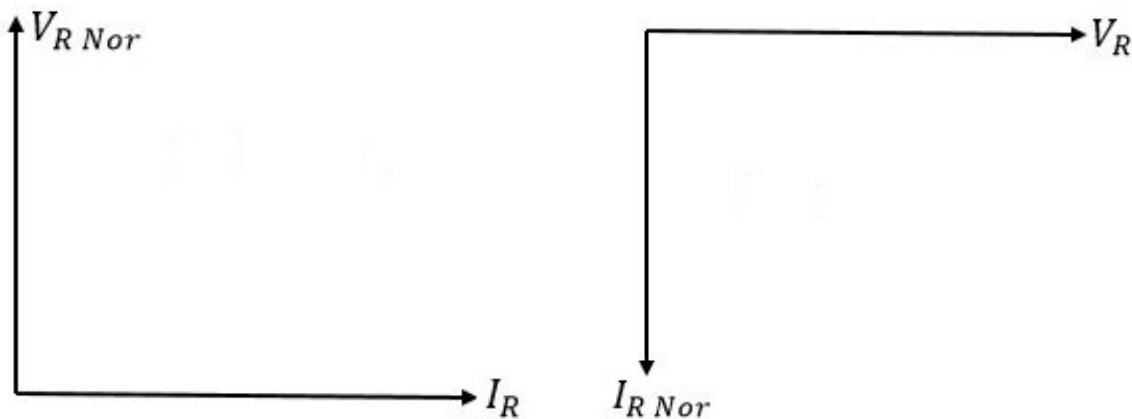

Figure 3: Fault voltage phasor in series compensated line

Fig. 3 depicts the problem of voltage inversion. Where V_{Rnor} the voltage at forward power flow situation and V_{Rinv} is the inverted voltage at forward power flow situation.

3.   SOLUTION APPROACH

The fault path impedance is changed in presence of capacitor in series compensated line. Due to this phenomenon, conventional directional relaying approach finds limitation inspite of several techniques. A 3-Φ power system with relay at bus Q is shown in Fig. 4.
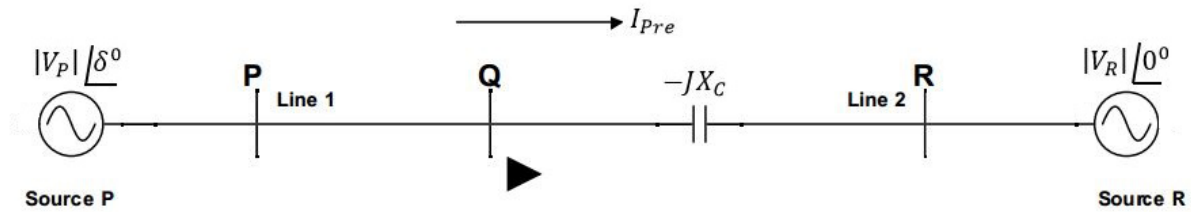

Figure 4: 3-Φ power system

The pre-fault line current can be stated as,

$$I_{Pre} = \frac{V_P - V_R}{Z_1}$$

(2)

where the source voltages are represented by V_P & V_R and total line impedance between two sides is Z_1.

3.1 Power flow from bus P to R

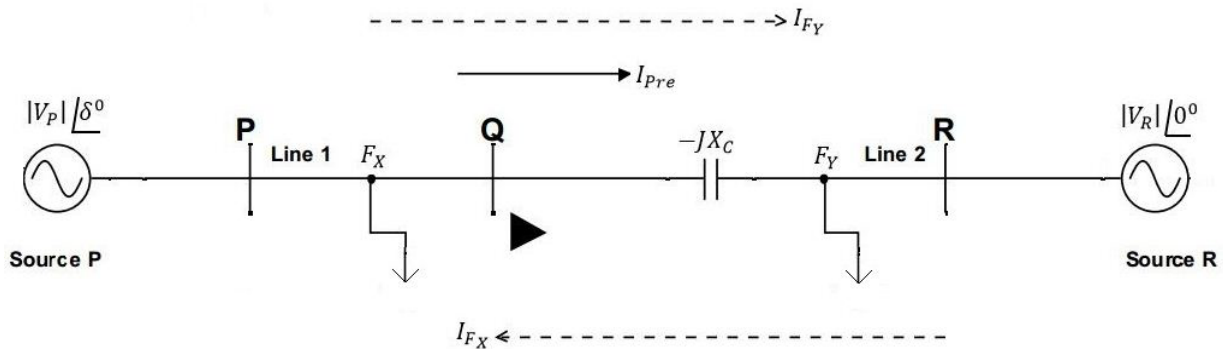Fig. 5 shows the forward power flow in between bus P to bus R.

Figure 5: Forward power flow

Fig. 6 shows the forward power flow with fault at F_X and its phasor diagram is shown in Fig. 7.
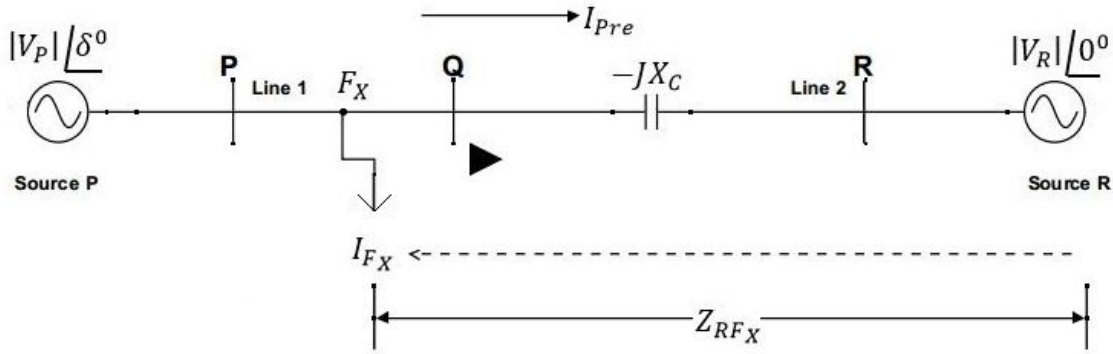
Figure 6: Forward power flow with fault at F_X Forward power flow

The fault current I_{F_x} flowing between source-R and the point F_X (i.e. at lowest potential) in case of upstream fault F_X is given by:

$$I_{F_x} = \frac{V_R}{Z_{RF_x}}$$

(3)

and fault current I_{1FR} through bus Q will be

$$I_{1FR} = I_{Pre} - I_{F_x}$$

(4)

In case of phasor estimation, first pre-fault or steady current (i.e. I_{Pre}) is measured. From Fig. 6, it is observed that power will flow from source-P to source-R and fault occurred at point F_X. Fault current (I_{F_x}) flow from source-R to point F_X. Direction of pre-fault current (I_{Pre}) and direction of fault current are opposite to each other. Sequence current (I_{1FR}) through relay connected bus Q is shown in equation (4).
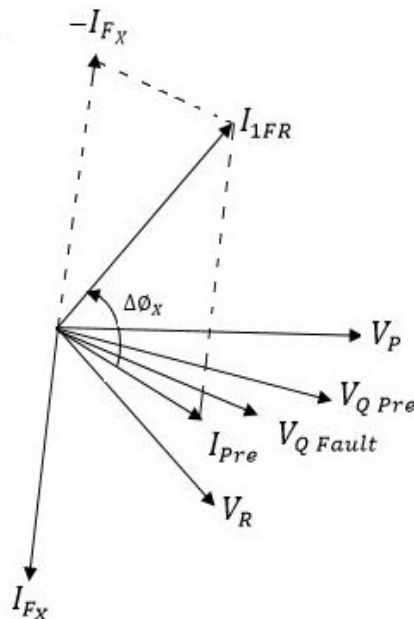

Figure 7: Phasor diagram for forward power flow for fault at F_X

where V_P is the voltage at bus P taken as reference bus, V_{QPre} is the pre-fault voltage seen by relay at bus Q, V_{QFault} is the fault voltage seen by relay at bus Q, I_{Pre} is the pre-fault current, V_R is the voltage at bus-R, I_{F_x} is the fault current flowing from source-R to lowest potential point F_X, I_{1FR} is the difference between I_{Pre} and I_{F_x}, and $\Delta\phi_X$ is the difference of phase among fault and steady (i.e. pre-fault) positive sequence current.

It is clear from Fig. 7 that fault occurs at upstream side of the relay in Fig. 6, and validates the results with simulation.

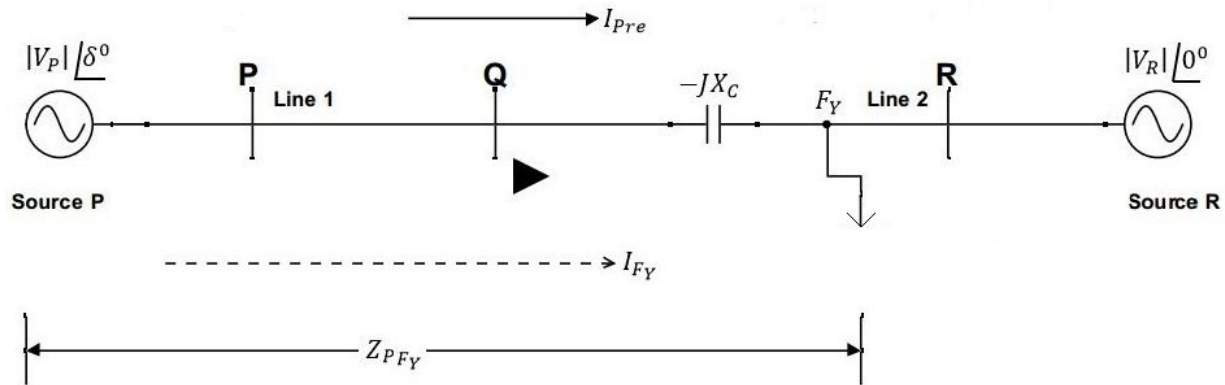Fig. 8 and Fig. 9 indicate the forward power flow with fault at F_Y and its phasor diagram respectively.

Figure 8: Forward power flow with fault at F_Y

The fault current I_{F_Y} flowing between generator-P to the point F_Y (i.e. at lowest potential) in case of downstream fault F_Y is given by:

$$I_{F_Y} = \frac{V_P}{Z_{PF_Y}}$$

(5)

and fault current I_{1FP} through bus Q will be

$$I_{1FP} = I_{Pre} + I_{F_Y}$$

(6)

It is observed from Fig. 7 and Fig. 9 that the phase difference among fault and steady PSC phasors are positive $\Delta\phi_X$ and negative $\Delta\phi_Y$ for upstream fault (at F_X) and downstream fault (at F_Y) respectively.
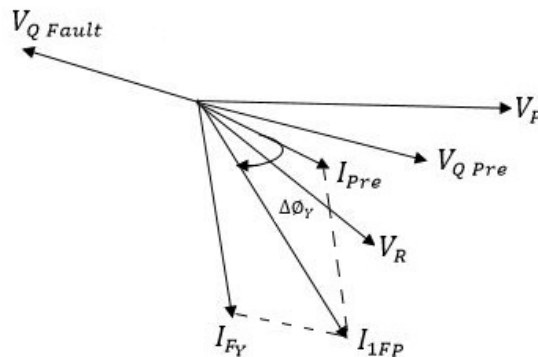

Figure 9: Phasor diagram for forward power flow at fault F_Y

3.2 Power flow from bus R to P

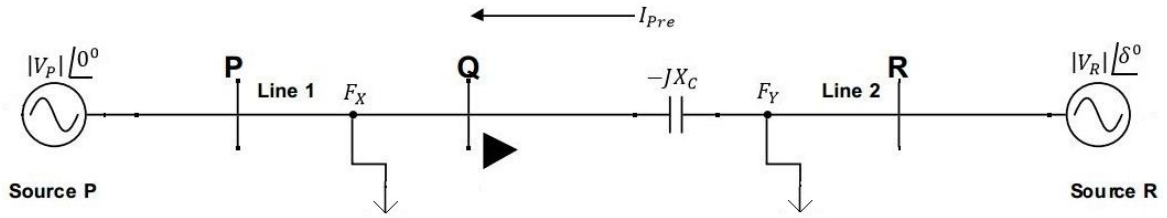Fig. 10 shows reverse power flow where power will transfer from bus R to P.

Figure 10: Reverse power flow

The steady current (i.e. pre-fault current) in the line can be articulated as,

$$I_{Pre} = \frac{V_R - V_P}{Z_2}$$

(7)

where the source voltages are represented by V_R & V_P and total line impedance between two sides is Z_2.

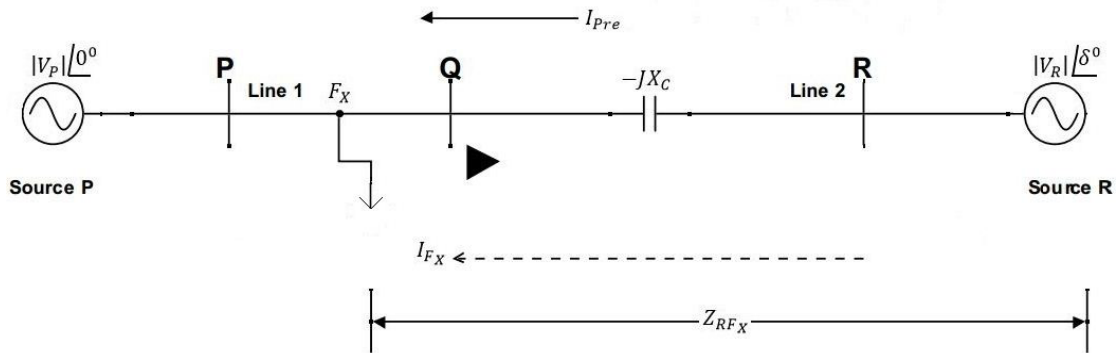**Figure 11: Reverse power flow with fault at** F_X

The fault current (I_{F_x}) flowing between source-R and the point F_X F_X(i.e. at lowest potential) in case of downstream fault is given by:

$$I_{F_X} = \frac{V_R}{Z_{RF_X}}$$

(8)

and fault current (I_{1FR}) through bus Q will be

$$I_{1FR} = I_{Pre} + I_{F_X}$$

(9)

Figure 12: Reverse power flow phasor diagram of fault at F_X

It is observed from the above phasor diagram, that phase difference ($\Delta\phi_X$) among fault and steady PSC phasors for fault at downstream (F_X) is negative.

Fig. 13 and Fig. 14 indicate the reverse power flow with fault at F_Y and its phasor diagram respectively.

Figure 13: Reverse power flow with fault at F_Y

The fault current (I_{F_Y}) flowing between the generator-P to the point F_Y (i.e. at lowest potential) in upstream fault is given by:

$$I_{F_Y} = \frac{V_P}{Z_{RF_Y}}$$

(10)

and fault current (I_{1FP}) through bus Q will be

$$I_{1FP} = I_{Pre} - I_{F_Y}$$

(11)
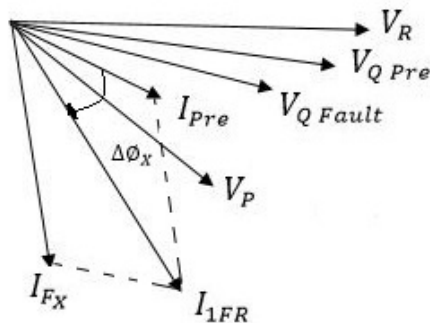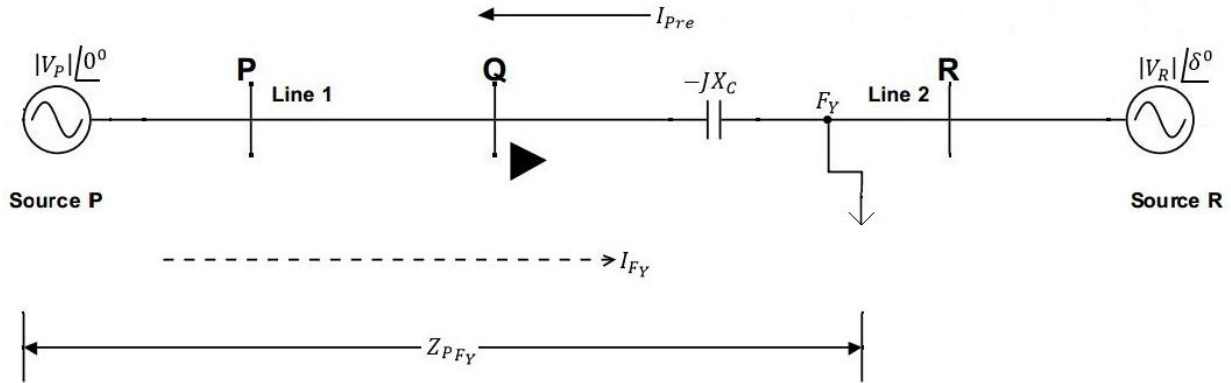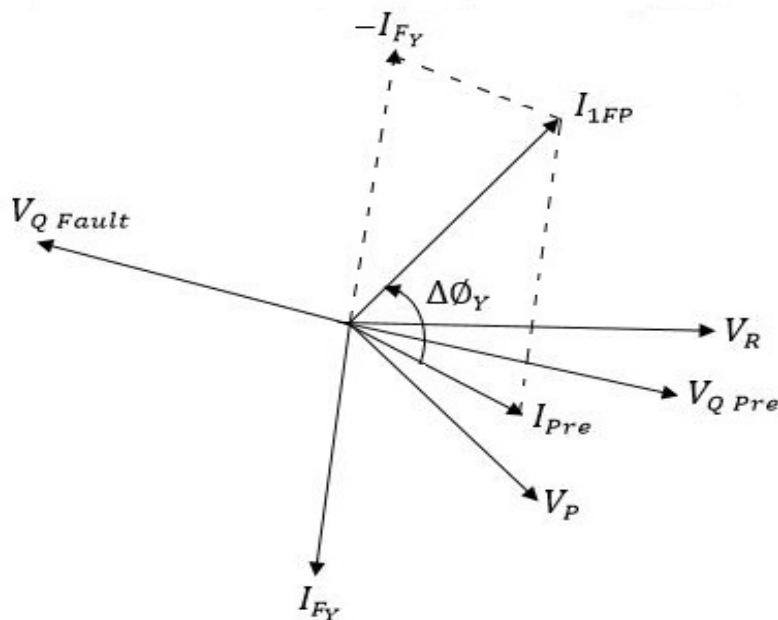

Figure 14: Reverse power flow phasor diagram at fault F_Y

The phase difference ($\Delta\phi_Y$) among fault and steady PSC phasor for upstream (F_Y) is positive as shown in Fig. 14. Summary of the phasor diagrams are shown in Table 1 which lead to the fault direction estimation.

Table 1

Summary of the phasor diagrams

Power Flow from Bus	Power Flow	Fault at	Phase difference among fault and steady PSC phasors
P to R	Forward	Upstream (F_X)	$\Delta\phi_X$ is positive
P to R	Forward	Downstream (F_Y)	$\Delta\phi_Y$ is negative
R to P	Reverse	Downstream (F_X)	$\Delta\phi_X$ is negative
R to P	Reverse	Upstream (F_Y)	$\Delta\phi_Y$ is positive

6. RESULTS AND DISCUSSION

Difference of angles between sequence current and voltage phasors and phase difference among fault and steady current phasor are preferred for the estimation of fault direction in conventional techniques.

Only angle difference of current between fault (I_{fault}) and pre-fault ($I_{pre-fault}$) is utilized to estimate the direction of fault in this paper. The simulated results of the system for distributed parameter model using EMTDC/PSCAD are given in Table 2 to Table 5. FFT is used in this paper for obtaining sequence component.

A 400 kV, 50 Hz 3Ø system is considered in Fig.4. Steady current (i.e. pre-fault current) phasors are estimated with 1-cycle steady current data immediately before fault occurrence and fault phasor are also computed with 1-cycle of fault current data after the commencement of fault. Positive sequence components were calculated with phase-A as reference in PSCAD. The cycle-to-cycle comparison technique is followed for the estimation of fault. Capacitor is used at the relay end as shown in Fig. 4 for 70% compensation of the system. Only current information is used for the performance analysis of the directional relaying at bus Q and results are provided in Table 2 to Table 5 for both side simulation of relay. Appendix I shows the system data.

4.1 Results for Forward power flow

Table 2

Results of ABC fault

Fault Position and State of Capacitor	$I_{pre-fault}$ phasor		I_{fault} phasor		$\Delta\phi$ (rad)
	Magnitude (KA)	Angle (rad)	Magnitude (KA)	Angle (rad)	
F_X, without C	0.097939	-1.249083	0.460084	0.745294	1.994377
F_Y, without C	0.098190	-1.249753	0.411716	-2.023149	-0.773395
F_X, with C	0.163778	-0.978173	0.308138	0.610081	1.588254
F_Y, with C (voltage inversion)	0.1641770	-0.978970	0.433757	-1.724805	-0.745835

Table 2 reveals results for ABC fault (3Ø fault) with capacitor as well as without capacitor. From Table 2, it is clear that, the phase difference is 1.994377 rad which is same with the direction obtained from phasor diagram for upstream fault. Difference of angle between fault and pre-fault current is -0.773395

rad for downstream fault without capacitor, correctly identifies the fault direction and validated the phasors diagram. Fault for upstream case with the capacitor is simulated as (F_X side) 1.588254 rad. For voltage inversion situation (capacitor presents between relay bus and fault point), fault at downstream side, the phase difference among fault and steady current gives proper decision and approximates the angle difference to be –0.745835rad which is same as per direction obtained from the phasor diagram of downstream fault.

Table 3

Results of ABG fault

Fault Position and State of Capacitor	$I_{pre\text{-}fault}$ phasor		I_{fault} phasor		$\Delta\phi$ (rad)
	Magnitude (KA)	Angle (rad)	Magnitude (KA)	Angle (rad)	
F_X, without C	0.097939	– 1.249083	0.340317	0.802467	2.051550
F_Y, without C	0.098190	– 1.249753	0.340781	– 1.836398	– 0.586644
F_X, with C	0.163778	– 0.978173	0.210931	0.413626	1.391799
F_Y, with C (voltage inversion)	0.164177	– 0.978970	0.370483	– 1.583278	– 0.604308

Table 3 shows results for ABG fault (2L-G) for a fault resistance of 5 Ω. Fault at F_X without C and fault at F_Y without C are 2.051550 rad and -0.586644 rad respectively which gives the fault direction properly and the compensated line (here capacitor connected line) at voltage inversion (downstream fault) estimates the angle -0.604308 rad which shows the fault occurred at downstream. Similar results are obtained for AB fault (Double-line fault) is shown in Table 4.

Table 4

Results of AB fault

Fault Position and State of Capacitor	$I_{pre\text{-}fault}$ phasor		I_{fault} phasor		$\Delta\phi$ (rad)
	Magnitude (KA)	Angle (rad)	Magnitude (KA)	Angle (rad)	
F_X, without C	0.097939	– 1.249083	0.369233	0.811806	2.060889
F_Y, without C	0.098190	– 1.249753	0.371221	– 1.866168	– 0.616414
F_Y, with C	0.163778	– 0.978173	0.226663	0.444481	1.422654
F_Y, with C (voltage inversion)	0.164177	– 0.9789704	0.391786	– 1.626003	– 0.647033

Above table shows that during the upstream fault expected angle difference ($\Delta\phi$) is positive and is consistent throughout. From Table 2, Table 3 and Table 4, it is clear that calculated phase difference ($\Delta\phi$) is negative in case of fault in downstream ($F_Y F_Y$) and is steady throughout. These results also validate the direction obtained from the phasor diagrams.

4.2 Results for Forward power flow

The pre-fault (i.e. steady) power transfer direction may vary in reverse power flow condition. Applying theory concept of Section 2, phasor diagrams are first acquired. Fig. 12 and Fig. 14 provide the phasor diagrams of upstream and downstream fault with pre-fault current flows from bus R to bus P. Results for reverse power flow 3Ø fault is shown in Table 5. The estimated current phase difference among fault and steady current is –0.691943 rad for the fault at point F_X taken as downstream without capacitor and 0.713418 rad for fault at point $F_Y F_Y$ (considered as upstream).The estimated phase difference between fault

and steady current is -0.625735 rad for the fault at F_X point (considered as downstream) with capacitor and 0.78694 rad for the fault at F_Y point (considered as upstream) which indicates the direction properly.

Table 5

Results of ABC fault with reverse power flow

Fault Position and State of Capacitor	$I_{pre-fault}$ phasor		I_{fault} phasor		$\Delta\phi$ (rad)
	Magnitude (KA)	Angle (rad)	Magnitude (KA)	Angle (rad)	
F_X, without C	0.095356	1.783734	0.613841	1.091791	–0.691943
F_Y, without C	0.095098	1.784071	0.261984	2.497489	0.713418
F_X, with C	0.158669	2.066474	0.572610	1.440738	–0.625735
F_Y, with C (voltage inversion)	0.158274	2.066860	0.200273	2.853800	0.78694

5.   CONCLUSION

In this paper, fault direction estimation technique (angle difference between I_{fault} and $I_{pre-fault}$) is used to detect the direction of fault when fault occur in upstream as well as downstream during forward power flow and reverse power flow situation. System model designed in PSCAD/EMTDC software. The estimation technique efficiently identifies the fault direction. The technique is tested for normal case system i.e. without capacitor, voltage inversion, power transfer is reverse direction etc. and from the obtained results, it is clear that proposed technique correctly identified the fault direction.

APPENDIX-I

Used system: 400 kV, 50 Hz, 3-Φ system

Line parameters are:

Line1= 255 km.

Line2 = 285 km.

Positive sequence resistance=0.03293 Ω/km

Positive sequence inductance=1.0140*10^{-3} H/km

Positive sequence capacitance =0.01136 μF/km

Zero sequence resistance=0.2587 Ω/km

Zero sequence inductance=2.4925*10^{-3} H/km

Zero sequence capacitance= 0.00768 μF/km

Source parameters are:

Positive sequence resistance=0.06979 Ω

Positive sequence inductance=6.3655*10^{-3} H

Zero sequence resistance=0.2094 Ω

Zero sequence inductance=0.019096 H

Data sampling rate= 4 KHz

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