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A Comparative study of Recessed strap Dopant Segregated Schottky and SYM-K SPACER FinFET

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ABSTRACT

The effect of silicide gating due to fringing fields on recessed strap Dopant Segregated Schottky FinFET is investigated. In the Dopant Segregated Schottky device, the individual source/drain fins should have minimal silicide flaring and be strapped with a metal bar was observed. A new structure is proposed, which combines the merits of optimized Dopant Segregated Schottky and Raised Source Drain FinFETs in a way that provides equivalent or improved performance over all ranges of H_{fin} and reduced capacitance is observed. However, due to the high-K dieclectric spacer, capacitance overhead occurs so an alternative novel called SYM-K spacer structure with reduced capacitance and also with reduced short Channel Effects is modeled.

Keywords: Capacitance, dopant segregation, FinFET, metallic source/drain (MSD), raised source/drain (RSD), Schottky barrier (SB).

1. INTRODUCTION

The fundamental limit for CMOS scaling is less on state current I_{ON} and high off state current I_{OFF}. Ultra thin body MOSFET has large junction parasitic resistance in source/ drain. Due to large parasitic resistance in the source drain and channel regions reduces I_{ON}. Scaling of V_{DD} reduces off-state current I_{OFF} due to sub-threshold swing (SS) but the on-state current I_{ON} reduces due to less overdrive ($V_{GS} – V_T$). By reducing V_T maintains I_{ON} and increases I_{OFF}, which leads to higher standby power dissipation. Metallic source/drain (MSD) MOSFET eliminates resistance in the source/drain and channel regions and maintains I_{ON}. Optimal MSD MOSFET performance is achieved by using heavily doped source/drain extensions (SDEs) adjacent to the Schottky barrier (SB) contacts. Implanting silicide to the Schottky barrier (SB) structure called as dopant-segregated Schottky (DSS) or modified SB MOSFETs [1-5]. The MSD technology reduces short channel effect (SCE) due to the source-side SB and the abrupt silicide to-silicon junction. The MSD technology enhances carrier-injection velocity by SB injection at the source.

FinFETs are wrapping around the source/drain and body areas (diffusion) by the polysilicon gate of the transistor. The electric field passes through in 3 directions (top and both sides) which depletes the channel rather than just from the top as in a planar gate. When the channel can be fully depleted, the need for doping in the silicon decreases or is eliminated. This reduces the manufacture cost as less doping step in the channel. Due to less doping, matching between transistors increases results more stable V_t and better gate-channel modulation but parasitic capacitance increases. The potential impact of parasitic capacitance resulting from fringing field on FinFET device has significant performance and speed but reduces I_{ON}. The strength of fringing field is related to gate-dielectric thickness, the spacer width, fin width and pitch and the gate

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height. However, the introduction of thin metal gate in a multifin device was found increases to device speed without reducing on current drive and less impact on SCE.

The performance of symmetric double-gate MOSFETs with dopant-segregated Schottky (DSS) source/ drain (S/D) regions restricts the design space for meeting low standby power leakage specifications, and so, the RSD structure reduces leakage and enhances on state performance [6]. However, optimized DSS MOSFETs offer no fundamental improvement in ON-state current I_{ON} when compared to optimized raised source/drain (RSD) MOSFETs. For high performance (HP) design, heavier extension doping is required to reduce the higher leakage to optimize DSS and RSD MOSFETs [7]. Thus, by practical considerations the optimal S/D design for HP is dsigned.

In this paper device design optimization in Schottky Barrier FinFET, Raised Source and Drain FinFET, Dopant Segregated Schottky structures is investigated through TCAD and the basic of Reccessed Strap DSS and SYM-K Spacer FinFET modeling approach are described.

2. MODELING APPROACH

2.1. Initial device structure

This paper design with 2D double gate(DG) DSS NMOS structure as shown in Fig1. The DSS NMOSFET in Fig. 1 is initially considered, with gate length L_G = 3 nm, the fin width $t_{body} = L_{sp} = L_{SDE}$ = 7 nm, V_{DD} = 1 V, and the gate oxide thickness t_{ox} = 1 nm which is assumed to be a lower limit in consideration of quantization effects. Only a silicon body is considered in this study.

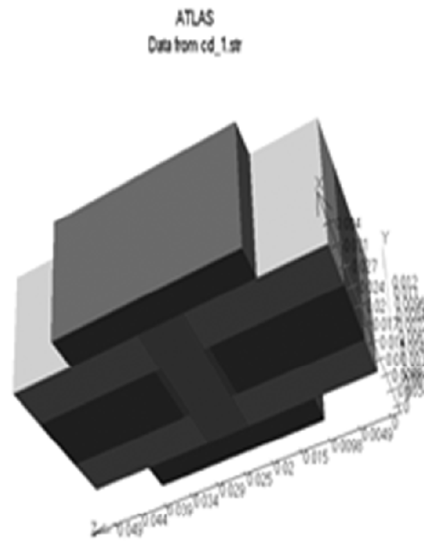

Figure 1: Dopant Segregated Schottky

Parameters	*Nominal Value*
Gate Length	10 nm
Fin Width	7 nm
Source width	5 nm
Source length	27 nm
Gate oxide thickness	1 nm
Underlap	7 nm
Channel depth	12 nm

Device dimension

The Gaussian doping profile in SDE is with peak concentration N_{SDE} at the source/drain SB junctions; L_{SDE} is the distance from the SB junctions to where the SDE concentration drops to 1×10^{18} cm $^{-3}$. L_{sp} is the gate underlap to the source/drain SB junctions where the sidewall spacer is made of silicon nitride[13], t_{flare} is the amount by which the source/drain silicide regions adjacent to the sidewall spacer flare out from the fin structure. The metal gate height t_{gate} = 20 nm, the body doping is 1×10^{15} cm^{-3} p-type, and NSDE = 3×10^{20} cm^{-3}. Meshed DSS structure is shown in fig 2. The SB height (SBH) at the M–S interface is set to 0.1 eV in all the cases simulated here. The work function of the silicide φM is varied independently from that of the SB contacts. The SBH increase due to quantization is 0.376/(m”t_{body}), where m is the effective mass in the quantization direction (0.92 in this case) and t_{body} is expressed in units of nanometers. As a result, SBH increase is 58 mV for t_{body} = 7 nm. This slight SBH increase will not affect I_{ON} significantly. Any effect of quantization is therefore primarily a threshold voltage shift and a reduction in mobility, neither of which would alter the results of a comparative study between DSS and RSD FinFETs.

The RSD FinFETs form an epitaxial RSD region around the fin source/drain region and then partially silicide to this epitaxial region, thus forms a wrapped contact (WC) structure. This is very similar to a DSS FinFET with an epitaxy-induced t_{flare}, but the source/drain region is not fully silicided. Depending upon the silicide the RSD region, affects current crowding within the source/drain regions. In RSD FinFETs fins strapped by lateral epitaxial growth in the source/drain regions offer lower C_{ov} and the lateral epitaxial fin strapping eliminates silicide access to the source/drain sidewalls.

In recessed silicide structure shown in Fig. 4, design with gate length(L_{g1} and L_{g2}) is 10 nm, channel depth L_d is 12nm, fin width (W_{fin1} and W_{fin2}) is 7 nm, source width (SW_1 and SW_2)is 5 nm, source length (SL_1 and

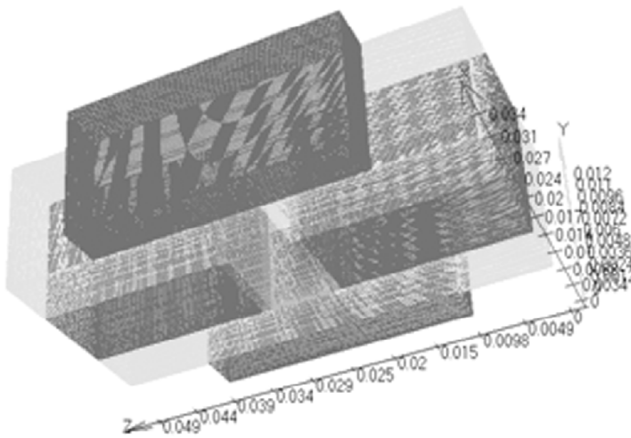

Figure 2: Meshed DSS Structure

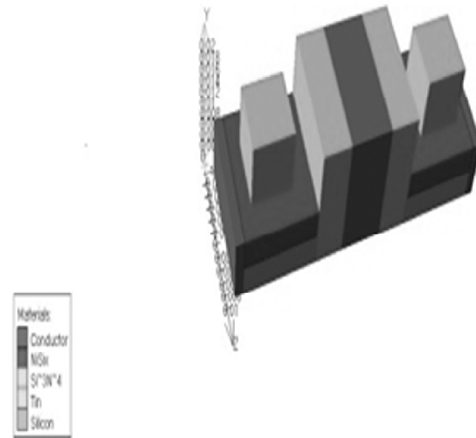

Figure 3: Raised Source Drain structure

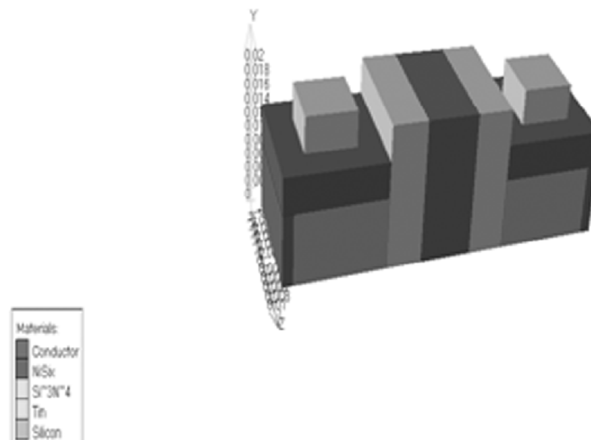

Figure 4: Embedded Silicide RSD

SL_2)is 27nm, gate oxide thickness(t_{ox1} and t_{ox2}) is 1nm , silicide length is 30 nm and underlap(L_{un1} and L_{un2}) is 7 nm. In recessed silicide structure capacitance C_{ov} increases with silicide thickness. Due to the larger combined RSD and silicide area extending the sidewall spacer in the recessed silicide structure suffers higher C_{ov}.

In the “embedded silicide” structure shown in Fig 4 no epitaxial silicon is grown prior to silicidation, lowers C_{ov}. Also the source/drain regions are very heavily doped decreases the voltage drop towards the bottom of the source/drain region. The device geometry and doping profile are same as for the basic 2D DSS structure except that the source/drain regions extending outward from the sidewall spacers. For both the recessed and embedded silicide structures, the inner silicide edge directly abuts the sidewall spacer and, for the embedded silicide structure, it is assumed that no lateral silicidation under the spacer takes place.

In order to avoid the usage of high capacitance recessed strapping is followed and a new structure called Recessed Strap DSS has evolved. Instead of keeping the source and drain immediately after the channel adding the strap like metal very adjacent to channel is recessed strapping. Epitaxial fin strapp, permits the use of vias results in lower C_{GG}. And reduced silicide gating, reduces delay dependence on FP and H_{fin}. M1 fin strapping FinFETs reduces fringing capacitance C_{fr} between the gate and M1 bar for each fin connected in parallel. With lateral epitaxial fin strapping, via pitches larger than FP can be utilized to reduce C_{fr}.

In symmetric K spacer Dual spacers are used for large-L_{sp} RSD FinFETs as shown in fig.6, the inner spacers have higher dielectric constant than the inner spacers. Double spacer reduces C_{GG}, although I_{eff} would also drop. The double spacers RSD FinFET achieve lowest delay on FP. Here Hfo_2 is used for outer spacer to form silicide contact otherwise the narrow SDE regions would be fully silicided.

Figure 5: Recessed Strap DSS

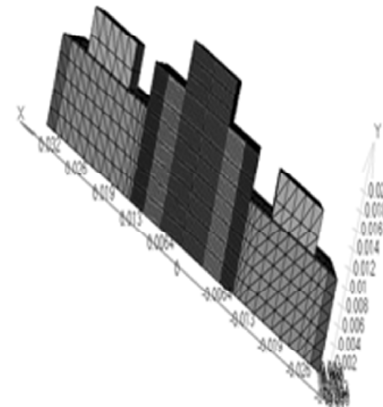

Figure 6: 3D FinFET with Double Spacer

3. RESULTS AND DISCUSSION

Gate Voltage versus drain current:

The graphs Figure 7(a) &(b) shown below are between input gate voltage and drain current with and without the silicides.

The drain current should increases linearly beyond the threshold voltage of the device with respect to the input gate voltage.

From the graph Figure 7(a) & (b) it was observed that drain current of DSS is $8e^{-7}$ ampere and the drain current of RSD is $4e^{-6}$ ampere.

Figure 8 shows the resistivity for raised source drain structure. From the graph it was observed that resistivity is high when the gate voltage less is than threshold voltage.

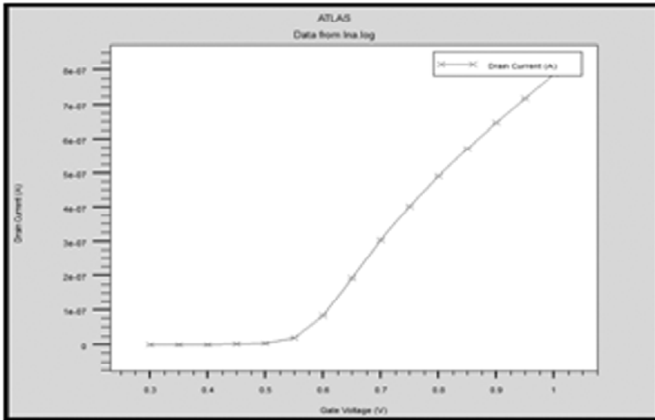

Figure 7: (a) I-V Characteristics of embedded silicide RSD

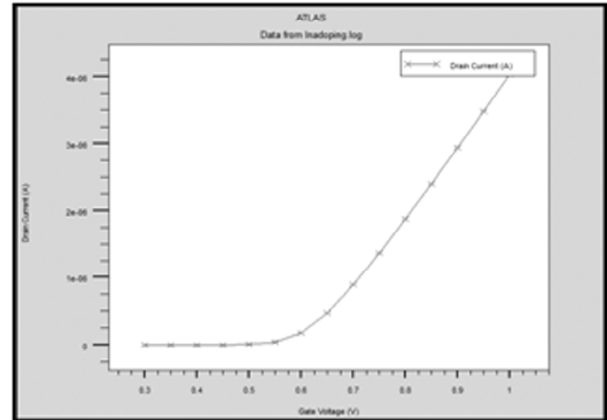

Figure 7: (b) I-V Characteristics of embedded silicide RSD

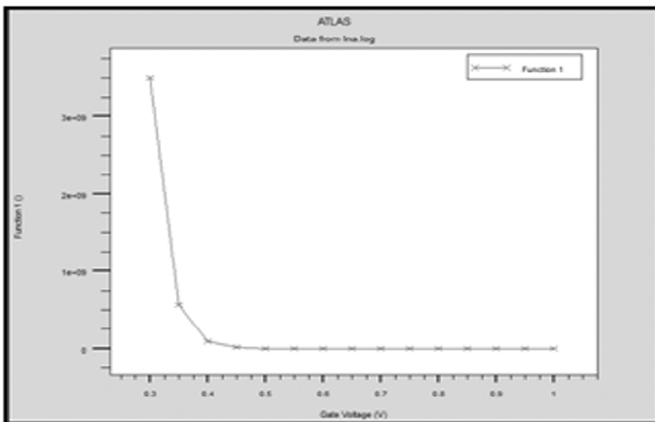

Figure 8: (a) Resistance for RSD structure

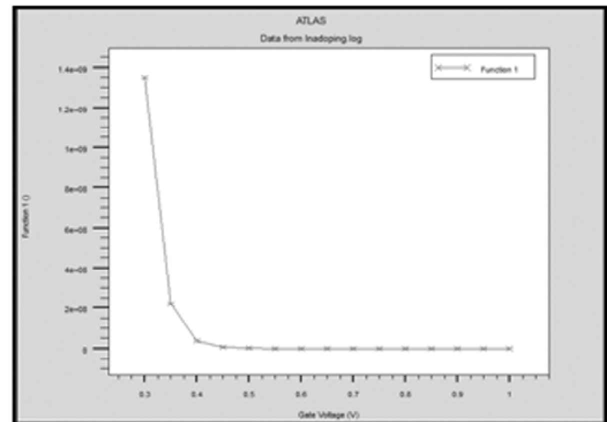

Figure 8: (b) Resistance Curves of Embedded Silicide structure

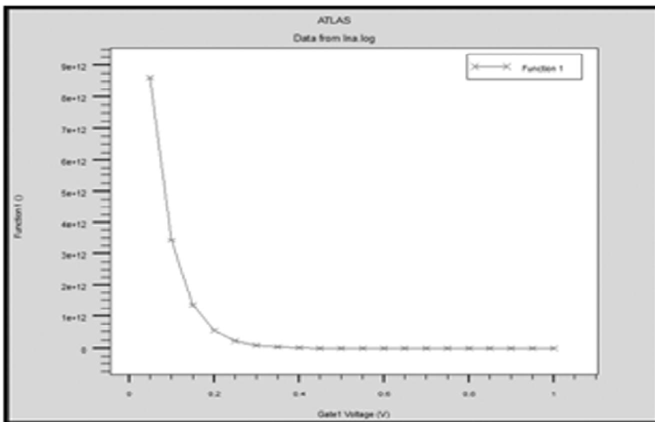

Figure 9: Resistance curve for Dopant Segregated Schottky FinFET

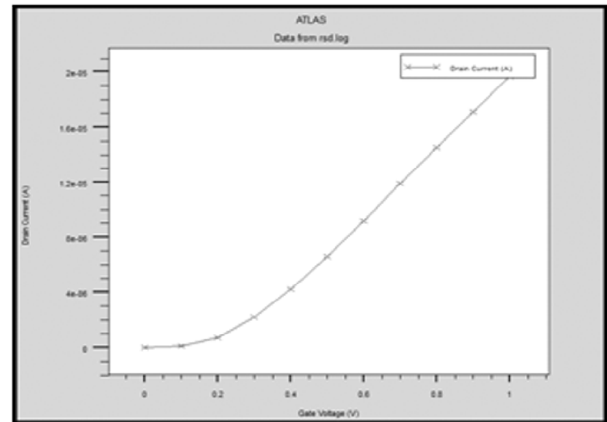

Figure 10: Drain current versus gate voltage

Figure 8(a) 8(b) shows the resistance of RSD is $3e^9$ and embedded silicide is$1.4e^9$ ohms.

From the graph Figure 9 the resistance of DSS is $9e^{12}$ ohms when the gate voltage is less than threshold voltage.

Figure 10 shows When V_{gs} is 0v drain current I_d is zero and it increases linearly above the threshold voltage.

From the figure 12 the resistance of dual spacer FinFET is $1e^{14}$ ohms.

From the above graph Figure 12 shows the capacitance for dual spacer FinFET is less compared to Schottky barrier and RSD DSS structure.

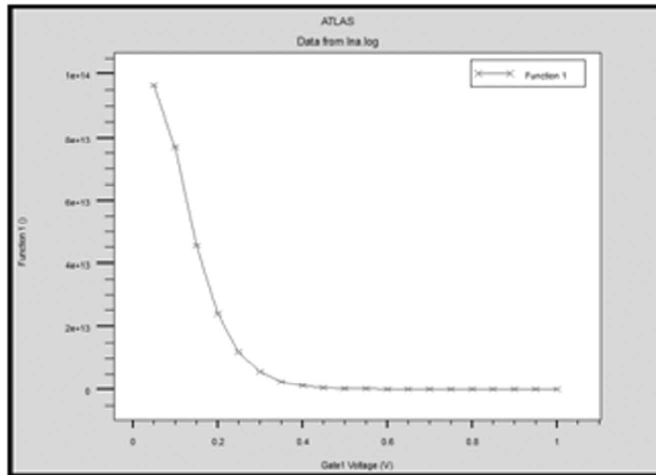

Figure 11: Resistance Curves of double spacer FinFET

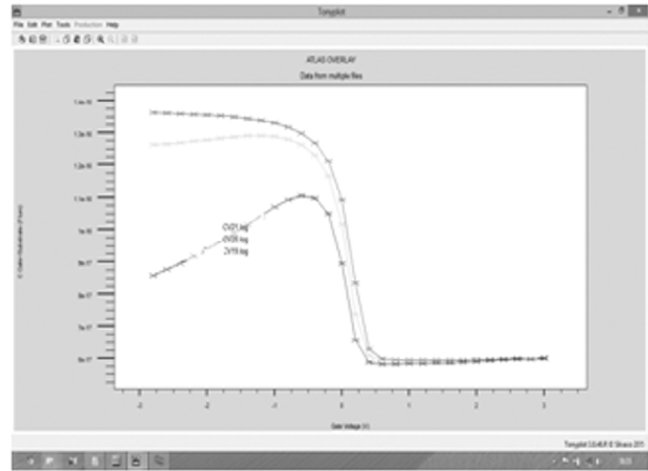

Figure 12: Capacitance vs gate voltage comparison with SB, RS DSS, proposed Sym-k FinFET

4. CONCLUSION

In this paper, various device models like Schottky Barrier FinFET, Dopant Segregated Schottky FinFET, Recessed Strap DSS, Sym-K Dielectric spacer FinFET are modeled and their I-V characteristics are studied and it is concluded that the RS DSS is the improvised structured over the DSS in terms of current and resistance but at the cost of capacitance. In order to have optimum capacitance and without loss of current and with no increament of ON resistance and also with reduced short channel effects, it is concluded that the optimum model is SYM-K spacer FinFET.

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