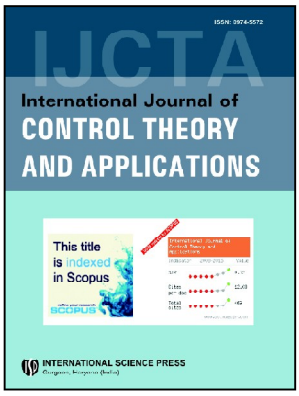

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A Review Article on Fin-FET Based Self-Checking Full Adders

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Abstract: This paper deals with Self checking full adder circuits in Fin-FET technology. Self checking is an interesting design in industrial applications as it reduces the hardware cost, design complexity with high fault coverage. In Self checking circuits by observing the outputs fault occurrence can be determined. Here the work is done by using Fin-FET other than the conventional MOS because the Fin-FET is having the advantage of low leakage power with no short channel effects, operating at high speed and at a low voltage as a result of their lower threshold voltage. The full adder reduces the complexity. Here the full adders are designed by using dual duplication code because the dual duplication code is having the advantage that it is self checking totally for single faults but it requires maximum hardware. Here one adder is constructed with novel differential XOR gate with individual four transistors which is fewer price. And another adder is wholly differential employment with individual 20 transistors so that this design saved 28.57% transistor count related with the employment using standard CMOS technology and it is highly consistent and fast adder. The 'performance parameters and the transient results are simulated in cadence software with 20nm Fin-FET technology.

Keywords: differential XOR, Totally self-checking circuits, self-checking adder, Fin-FET technology, differential full adder.

1. INTRODUCTION

As VLSI circuits increase in complication the attentiveness towards detection of on-line error is also growing continuously. Awareness in the transient faults is allowed by the Concurrent Error Detection(CED). Detection of transient faults is spotting in on-line testing. CED also furnish an opportunity for self-diagnosis and self-correction within a circuit design. Designing of self-checking memory systems, shifters and register files is effortless where as designing of arithmetic units (adders,ALUs,dividers and multipliers) is much more intricate. One of the most fundamental operations for digital computers is addition. It is clear that in the area of self-checking designing of arithmetic units is an important provocation..

Self-checking is nothing but noticing the occurrence of the fault at the output. The subclass of self-checking is totally self-checking(TSC) circuits. By the normal operation TSC circuits are used to spot the fault occurrence. Here a self-checking full adder is proposed with two rail encoding scheme by using novel differential XOR gate with Fin-FET, realized with only four transistors.

In Fin-FET the body of the device is formed by enclosing the conducting channel by a thin silicon 'fin' this is the speciality of Fin-FET which is shown in the Fig. 1. The effective channel length of the device is determined by the thickness of the film. The sheathe around the gate dispenses the electrical control over the channel. It also helps in overwhelm the short-channel effects and also diminishing the leakage current. Fin-FET is having fixed drain and contacts and it allows less power and expose less heat. It also takes less power at stand-by time.

As Fin-FET transistors are going to drive billions of transistors in coming years here it is used and it also possess higher intrinsic gain, better thermal stability and also 30% faster when contrast with non Fin-FET devices. These are mainly used in low power logic circuits.

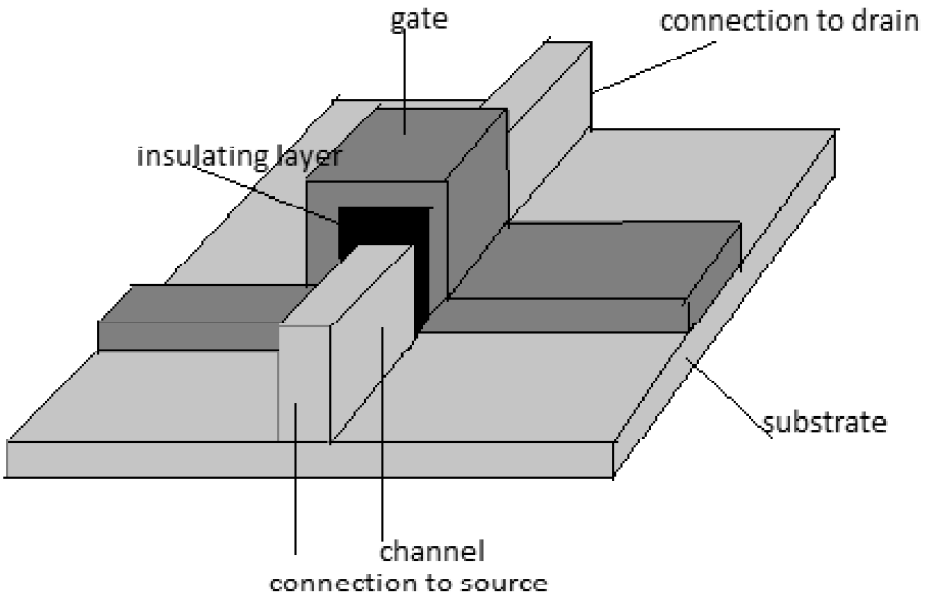


Figure 1: Top view of double gate Fin-FET structure

In this paper a self-checking full adders are designed. One adder is based on two-rail encoding scheme is proposed by using novel differential XOR gate performed in a 20nm Fin-FET logic, and realized with only four transistors. Another design is based on fully differential implementation with only 20 transistors.

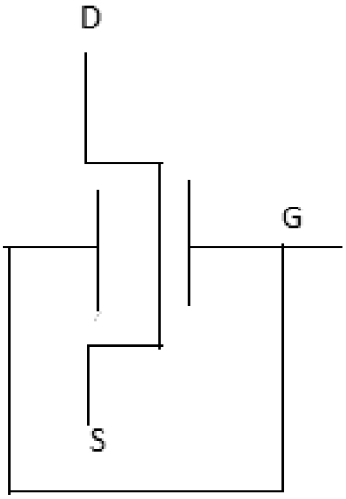


Figure 2: Symbol of Fin-FET

(A) Self – checking (SC) circuits

To design the complex VLSI circuits self-checking circuits are becoming a suitable approach, to handle with on-line and off-line testing. Here by observing the outputs of the circuit the occurrence of fault can be determined. Totally self-checking (TSC) are the important subclass of the self-checking circuits.

(B) Totally self-checking (TSC) circuits

TSC checkers are used to display the outputs when a non-code word is detected to indicate the error. By using the normal operation these circuits are used to detect the errors simultaneously. These circuits produce the encoded outputs by operating the encoded inputs. The TSC concept was first proposed in[15] and generalized in[19].

Totally self-checking (TSC) circuit basic structure is as shown in the Fig.3. Here the basic structure consists of functional block, checker and input as coded inputs and the output as coded outputs with error indication (E.I) at the checker block.

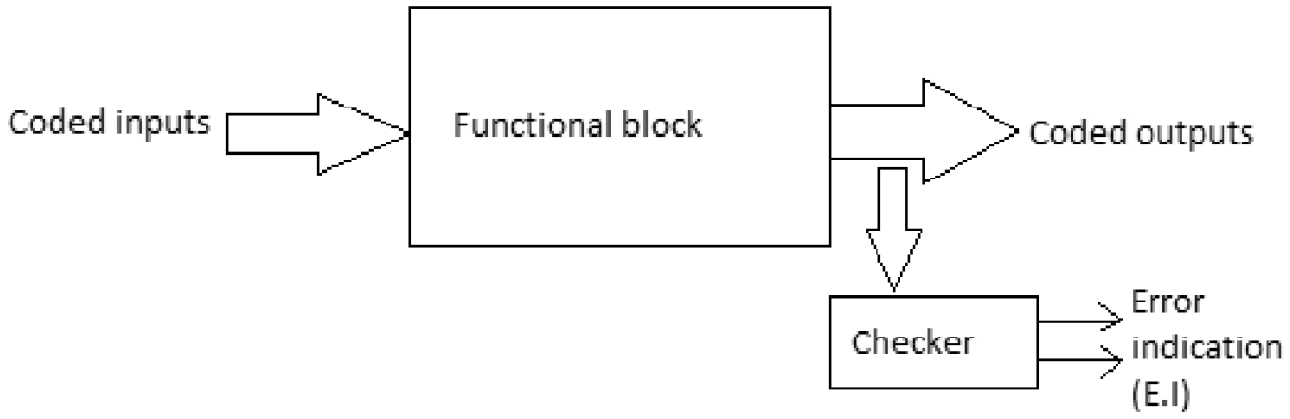


Figure 3: Basic structure of totally self-checking circuit

A totally self-checking block satisfies the following two properties:

(a) The circuit either produces an invalid code word on the output,or does not produce the error on the output for any valid input code word and any single fault. This property is known as fault secure property.

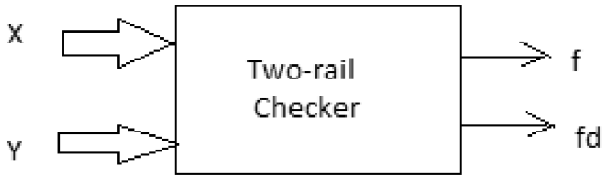
(b) For any valid input code word any single fault is noticeable. This property is known as self-testing property.

Whether the output of the circuit is valid or not is determined by the checker and also it governs the fault happening within itself.

Double-rail checker is based on the dual duplication code. This code compares two input words X and Y which are opposite and conveys a couple of outputs coded in dual rail.

The principle of dual-rail checker is as shown in the below Fig. 4.

In self-checking adder the functional block generates dual outputs by receiving dual inputs using double-rail code. Here the adder which is shown in the Fig.7 consists of two differential XOR and a differential carry gate. It requires large hardware as it is constructed with AND,OR and NOT symmetric gates.



f	fd	Conclusion
0	0	error
0	1	OK
1	0	OK
1	1	error

Figure 4: Principle of dual-rail checker

2. DIFFERENTIAL FULL ADDER

In this paper, the self-checking adder schemes are based on an optimized XOR/XNOR gate realized and are examined in Fin-FET technology as full adders are the fundamental components are XOR and XNOR. Here the adder consists of both sum and carry. To produce double-rail carry the carry gate is duplicated. The carry gate for stuck-at fault model is fault secure and this gate is self-testing. By giving some valid input code word any single internal fault is detectable, since it produces no complementary data and it will disturb only one output. So this scheme is known as TSC for stuck-at fault model. This scheme produces the signals (Gi,Gi bar) which as very helpful for implementation of fast adders such as group and full carry look-ahead ones, these signals are dual generation signals.

Coming to the sum function, it is implemented with two differential XOR gates. The first differential XOR takes ai and bi as inputs along with their complementary and produces the output pi and its complementary. The second XOR also accepts two inputs namely ci and its complementary as the dual carry and the outputs of the first XOR. Here it generates the dual sum function which is shown in the Fig6. Here the output voltage depends on the gate voltage of the switches but not on the number of switch transistors through which the signal travels.

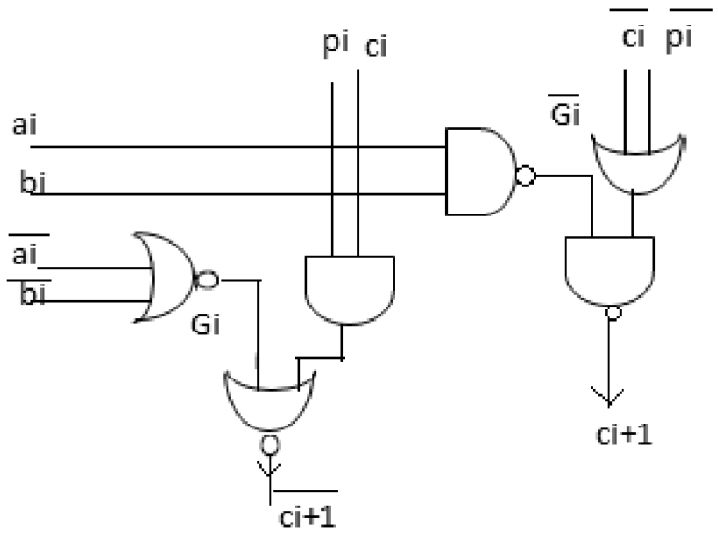


Figure 5: Differential carry gate

Differential full adder is designed by combining the differential carry gate and differential sum gate[1] as shown in the Fig. 5 and Fig. 6 respectively. In the Fig.7 The differential full adder scheme is shown by adding the inverters to restore the degraded signals generated by differential SUM gate. This scheme requires only 28 transistors.

Since the differential XOR1 receives primary inputs it is a self-testing. Differential XOR2 does not receives primary inputs as it receives dual-rail carry signals since they are created by the preceding stage. The differential carry is also self-testing.

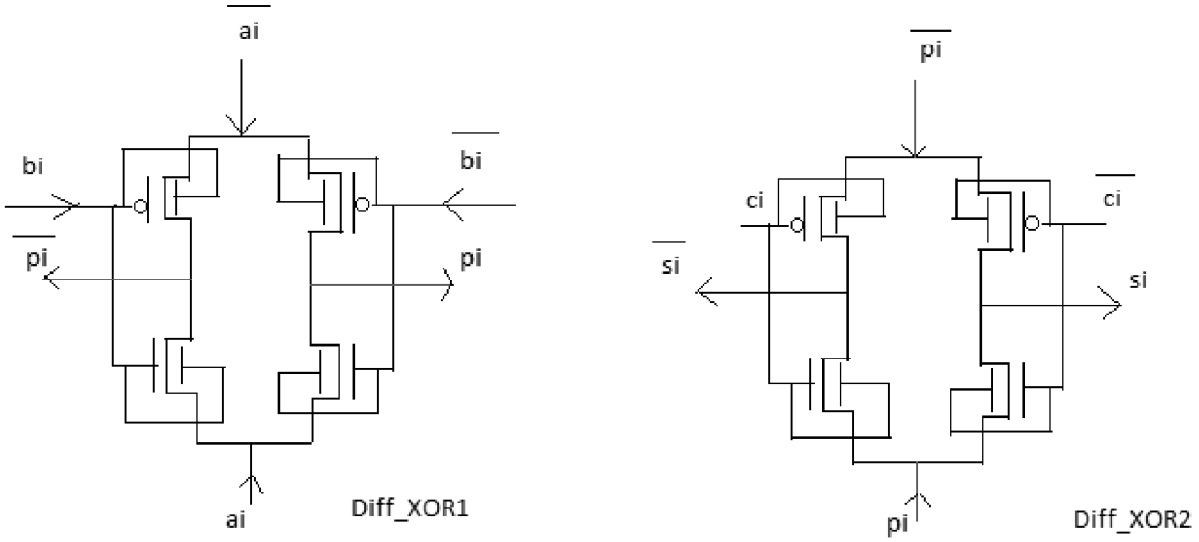


Figure 6: Differential SUM gate

Since the differential XOR1 receives primary inputs it is a self-testing. Differential XOR2 does not receives primary inputs as it receives dual-rail carry signals since they are created by the preceding stage. The differential carry is also self-testing.

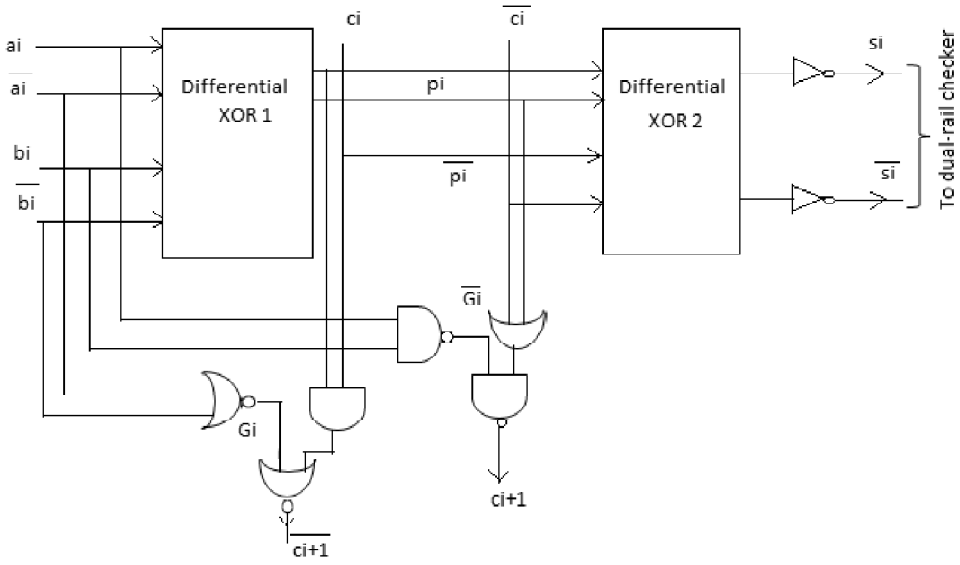


Figure 7: Differential full adder (28 transistors)

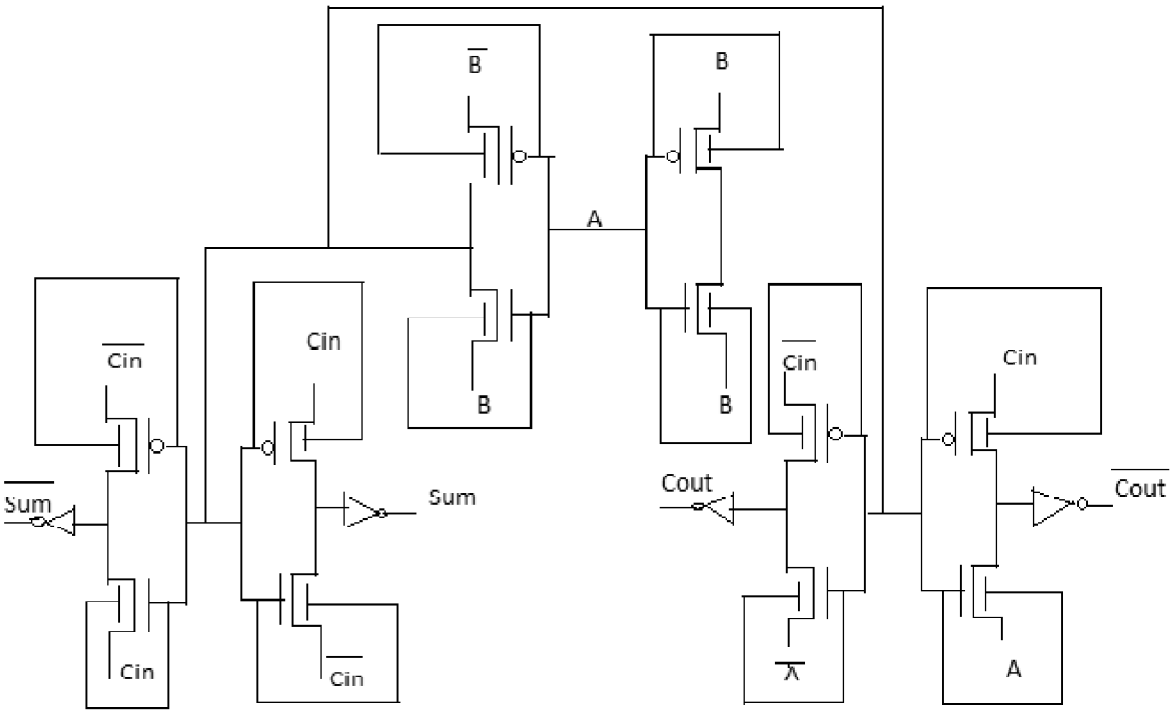


Figure 8: Self-checking Full adder

3. SELF-CHECKING FULL ADDER

A three-input and two-output block is nothing but a full adder, where the three inputs are namely a, b and cin which are summed. The sum operation result is the output which is denoted by sum and the resulting value of the carry output is represented by cout [2]. In literature many full adders have been designed and published which are built upon different logic styles. In this paper the self-checking full adder is based on 20nm Fin-FET. The Self-checking full adder is as shown in the Fig. 8.

4. SIMULATION RESULTS

(A) Differential full adder

The differential full adder is implemented in 20nm Fin-FET technology by taking 0.4V as supply voltage and ai, bi, ci and their complements as inputs to obtain the outputs as sum and carry. The power and delay are calculated for both sum and carry. The simulations were performed in CADENCE virtuoso tool. The simulation results without fault for the Fig. 7 are shown in the Fig. 9. By observing Fig.10 it is clear that the Differential Full adder is self-checking circuit because in Fig.10 the output is faulty.

(B) Self-checking full adder

The self-checking full adder is executed by taking a, b, cin and their complements as inputs to get the out puts as sum, carry along with their complements. This implementation was done in Fin-FET 20nm technology.

The delay and power also calculated for both sum and carry and these results are compared with the result of the differential full adder. The comparison is shown in table1.CADENCE virtuoso tool was used to simulate these results.

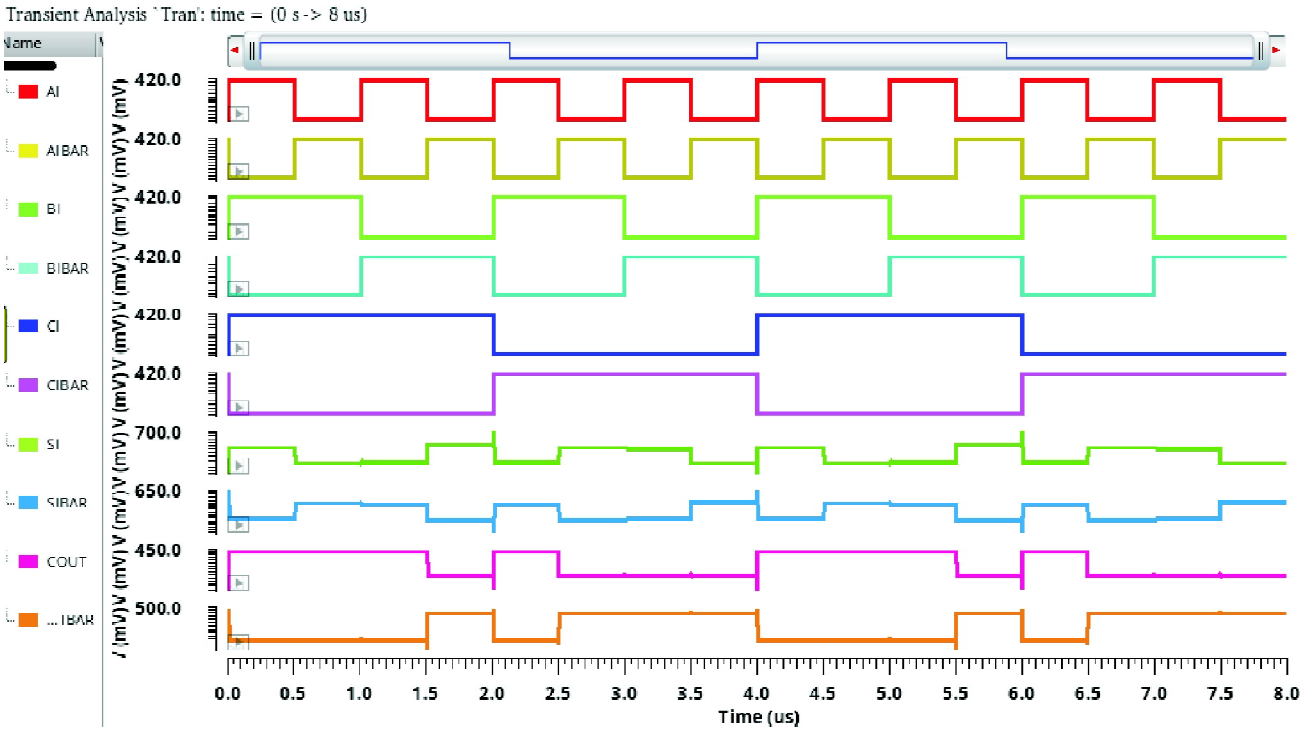


Figure 9: Simulation results for Differential Full adder

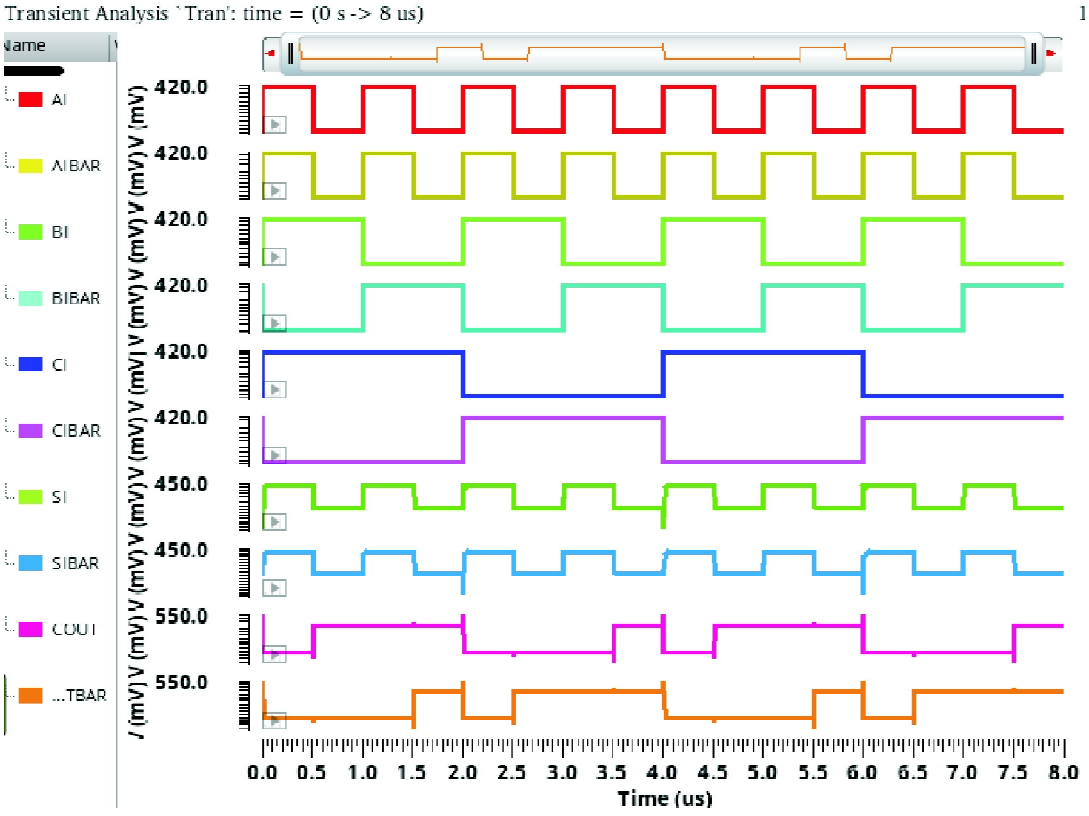


Figure 10: Simulation result for Differential Full adder with fault(a=a)

The power and delay for the Self-checking Full adder is also calculated and the output for that is shown in the Fig.11 which is fault free.

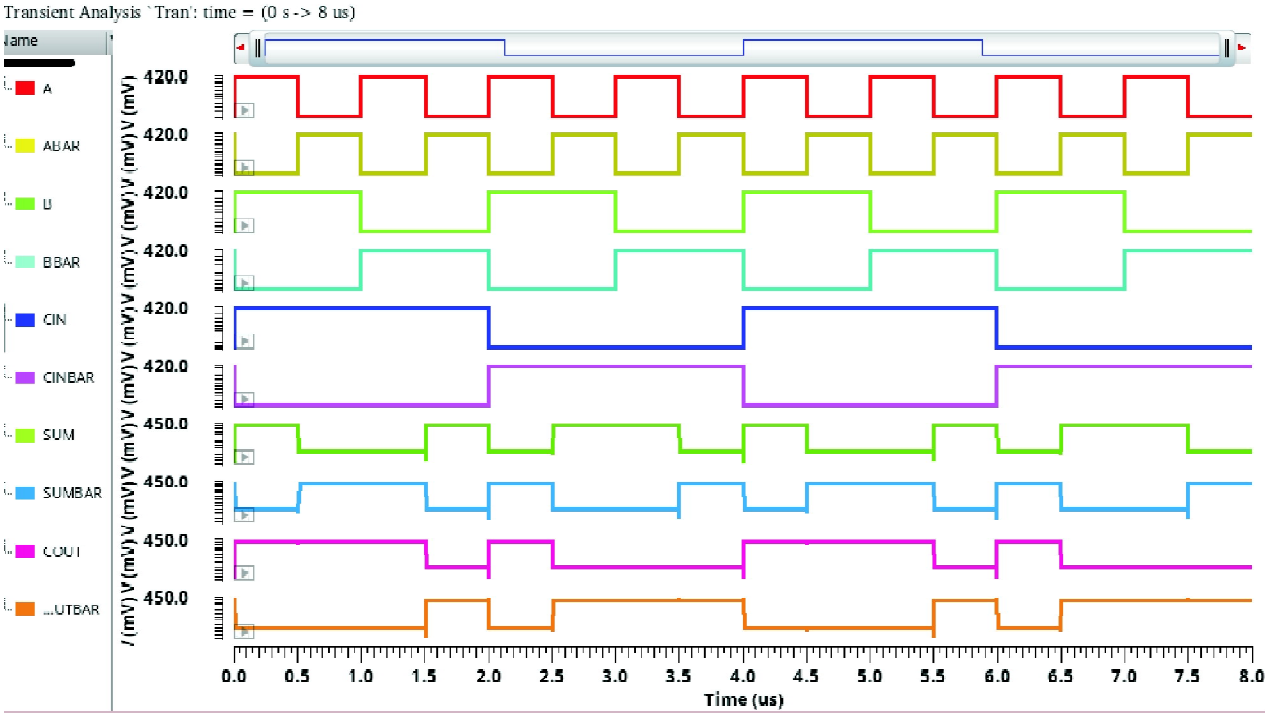


Figure 11: Simulation result for Self-checking Full adder

The self-checking property for the Self-checking Full adder was proved by observing the Fig.12 which shows the faulty output.

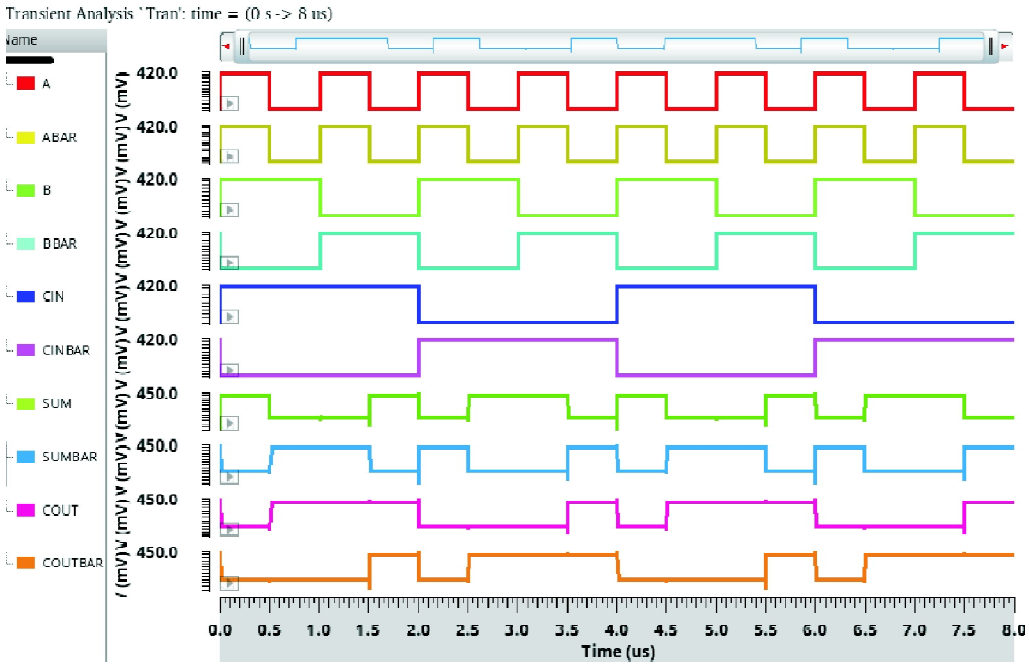


Figure 12: Simulation result for Self-checking Full adder with fault(a=a)

Table 1
Comparison of Power and Delay

Designs Names	*Vdd=0.4V* *Delay(E-6)*	*Power(E-9)*	*PDP(E-6)*
Self-checking Full adder	0.000007395	1.68	1.24236E-05
Differential Full adder	0.750002	3.645	2.73375729

4. CONCLUSION

In this paper there are two full adders namely Differential full adder and Self-checking full adder. In Differential full adder there is an advantage that is it consists of only 28 transistors so that it requires lowest hardware. It also operates at low voltages with a good speed. In Self-checking full adder by using dual-rail checker the fault is detected.

By comparing the power and delay of the both full adders it is clear that Self-checking full adder is having less power and delay. The comparison is shown in Table 1. Here the two adders were implemented using 20nm Fin-FET technology and the simulation is done in the CADENCE.

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