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Design of Independent Gate Symmetric/ Asymmetric Gate Work Function Shorted Gate FinFETs

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ABSTRACT

With the emergence of non-planar CMOS device at the 22nm and beyond manufacturers has started adopting FinFET for high performance process technology. Multigate field-effect transistors (FETs) overcome short channel effect problems because of tighter control of the channel potential by multiple gates wrapped around the body. Amongst multigate FETs, FinFETs have emerged as the best candidate structures from a fabrication perspective. The main objective of this paper, is to study the modeling of different types of FinFETs . In this paper we evaluate the symmetric gate and asymmetric gate work function shorted gate (ASG) FinFETs and independent gate(IG) FinFETs using Sentaurus technology computer aided TCAD.

***Index Terms*:** FinFETs, work function , device simulation

I. INTRODUCTION

The down scaling of CMOS device dimension has been the major driving force of the growth in the microelectronics during the past three decades. Due to the very narrow channel lengths in highly scaled MOSFETs, the drain potential begins to affect the electrostatics of the channel and, consequently, the gate loses the adequate control over the channel. As a result of this, the gate is unable to shut off the channel completely during the off-mode of operation, which always leads to an increased current flow between the drain and the source. The wide use of thinner gate oxides and high-k dielectric materials helps to lessen this problem by increasing the capacitance gate-channel. However, the over thinning of gate oxides is fundamentally leading to the deterioration in gate leakage and gate-induced drain leakage (GIDL) For lithography nodes from 20 m to 0.1 m, MOSFET gate oxide thickness has been deeply scaled together with complex channel doping design is included to suppress short channel effects (SCE). According to the findings of the 1999 International Technology Roadmap for Semiconductors, devices having gate length down to 20 nm can be expected in 2014 [1]. CMOS designs below 0.1 m are higly limited by lateral SCE and vertical gate insulator tunneling [2]. One of the approaches to control the gate tunneling restriction is to alter the device structure in such a way that MOSFET gate length can be scaled again even with thicker oxide. Double-gate MOSFET (DGFET) is always considered as one of the most favourable and realistic candidates for the channel length in the range of 10–30 nm. FinFET is modelled with special importance on process simplicity and compatibility with conventional planar CMOS technology.

There are two main types of FinFETs: shorted-gate and independent-gate . Shorted Gate FinFETs are also named as three-terminal (3T) FinFETs and IG FinFETs like four-terminal (4T) FinFETs. In Shorted Gate FinFETs, the front and back gates are always physically shorted, whereas in IG FinFETs, the gates are physically isolated .Thus, in SG FinFETs, both gates are jointly used to control the electrostatics of the channel. Hence, Shorted Gate FinFETs show higher on-current and also higher off-current (or the

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subthreshold current) compared to those of Independent Gate FinFETs. Independent Gate FinFETs offer the flexibility of applying different signals or voltages to their two gates. This enables the use of the back-gate bias to modulate the of the front gate linearly. However, IG FinFETs incur a high area penalty due to the need for placing two separate gate contacts.Thus, the purpose of this work is to do a detailed study on independent gate ,symmetric gate and asymmetric gate work function FinFETs. We evaluate Symmetric gate work function and Asymmetric gate work function FinFET devices using a high-performance process using 3-D device simulations in Sentaurus technology computer-aided design (TCAD).

The FinFET structure is made of a silicon fin bounded by shorted or independent gates on both side of the fin, on a silicon-on-insulator substrate. In the shorted gate mode of operation, both the gates are biased together to turn on the device, providing maximum gate drive. In the Independent Gate mode of operation, both the gates are electrically independent. The back gate voltage can be used to alter the threshold voltage (*V*th) of the front gate, hence forth controlling the OFF-current (*I*OFF) of the device [3]. *I*OFF in Shorted gate mode devices is obviously much higher than in Independent Gate-mode devices with the back gate kept above (below) the rail for p-type (n-type)], and because of the constant *V*th, it cannot be altered electrically. The *V*th is typically controlled by directly setting the gatework function. If the front and back gates have the same (different) workfunctions, they are referred to as Symmetric gate work function and asymmetric gate work function FinFETs. While Independent Gate -mode devices provide the added advantage of controlling the device *V*th, and so the delay/leakage, they forms a complicated transistor layout strategy. And it is due to this fact that multifin Independent gate-mode FinFETs need higher spacing between the source and drain regions, as well as higher fin pitch in order to land a contact to the back gate in comparison to multifin Shorted gate mode FinFETs with compact layouts.

Circuit designs relied on low-leakage multigate FETs /FinFETs has obtained significant attention over the past one decade, due to the large increase in leakage power consumption in conventional planar FETs at smaller technology nodes. Low-power multigate circuit designs have been investigatd from a device-circuit viewpoint in [4]-[5] , and also the logic styles using the Shorted Gate and Independent Gate modes of FinFET operations always have been investigated. FinFET latches and flip-flops are also been studied in [6]-[8]. Due to its very small dimensions, a FinFET probably suffer from the adverse effects of process and temperature variations. In the gate workfunction fluctuation is shown to be the most important contributor to the variation in *V*th for metal-gate FinFETs. FinFETs with asymmetric gate workfunctions in the form of different n+/p+ polysilicon gates is also been been engineered and investigated in [9]. Since multigate implementaion is likely to be controlled by performance/ area benefits, in this paper, we shortly explain Symmetric gate work function and Asymmetric gate work function FinFETs in a high performance process.

II. SYMMETRIC GATE WORK FUNCTION ASYMMETRIC GATE WORK FUNCTION SHORTED GATE AND INDEPENDENT GATE FINFET DEVICES

In this section, we evaluate Symmetric gate work function and Asymmetric gate work function FinFETs head to head in a high-performance process. In Table I, the parameters for a typical n/p-FinFET device are listed, where *L*GF, *L*GB, *T*OXF, *T*OXB, *T*SI, *H*FIN, *H*GF, *H*GB, *L*SPF, *L*SPB, *L*UN, *N*BODY, *Ö*GF, *Ö*GB and *N*SD are the physical front- and back-gate lengths, front- and back-gate effective oxide thicknesses, fin thickness, fin height, front- and back-gate thicknesses, front- and back-gate spacer thicknesses, gate-drain/ source underlap, body doping, front- and back-gate work functions, source/drain doping respectively. The *V*th of FinFETs is typically tuned by directly adjusting the workfunction of the gate material [10]. The workfunctions for n-FinFET is 4.4 eV devices were chosen corresponding to high-performance logic requirements [11] and yield low-*V*th devices whose symbols are shown in Fig. 1.

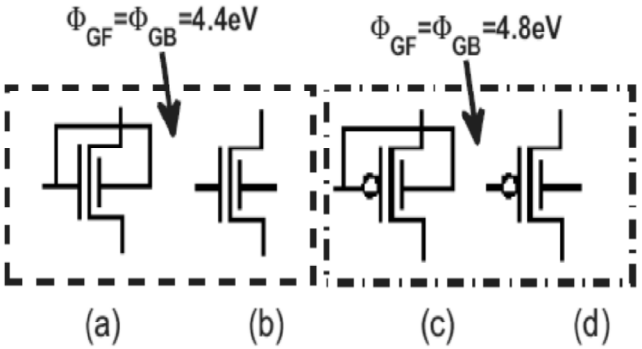

Figure 1: (a) Shorted gate mode n-type (b) Independent gate mode n-type

Table I
FinFET Device Parameters

Parameters	
L_{GF}, L_{GB} (nm)	25
Effective T_{OXF}, T_{OXB} (nm)	1
T_{SI} (nm)	10
H_{FIN} (nm)	50
H_{GF}, H_{GB} (nm)	20
L_{SPF}, L_{SPB} (nm)	20
L_{UN} (nm)	10
N_{BODY} (cm–3)	10^{15}
Φ_{GF}, Φ_{GB} (eV)	Φ_{Gn}: 4.4, Φ_{Gp}: 4.8
N_{SD} (cm^{-3})	10^{20}

We utilized the FinFET device structure shown in Fig. 2, Fig .3, Fig. 4, for 3-D device transport simulations in Sentaurus TCAD

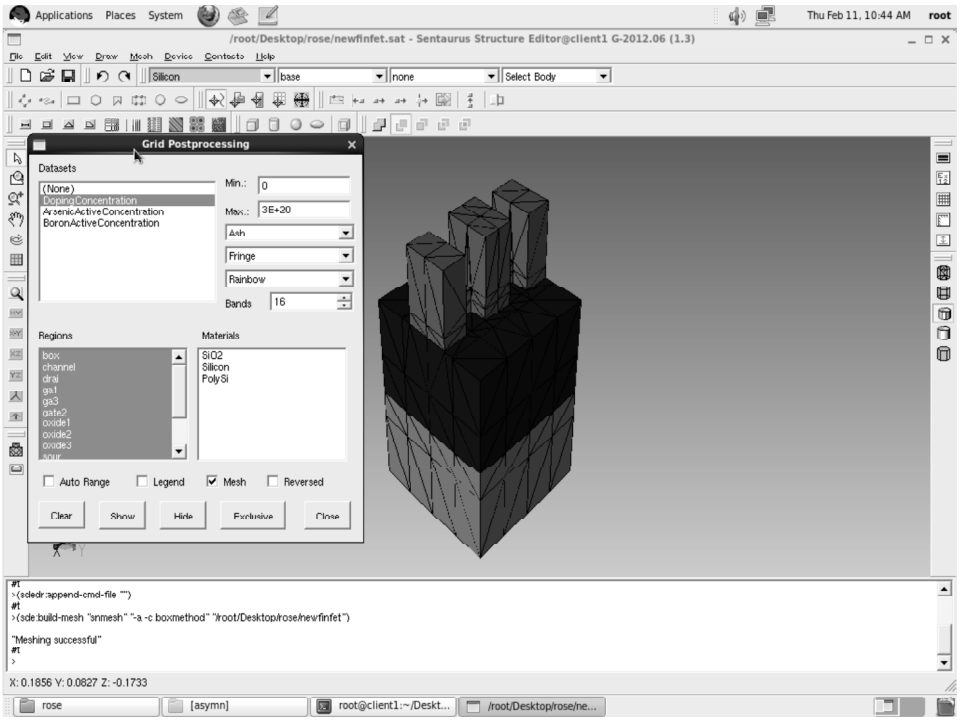

Figure 2: Meshed structure of symmetric gate work function shorted gate FinFET

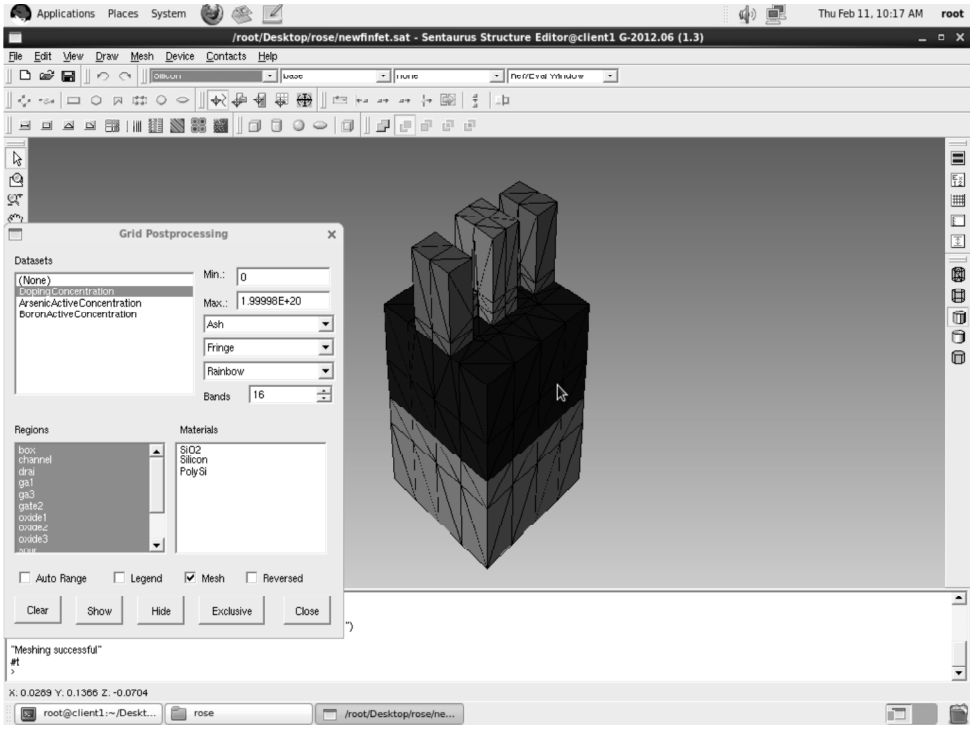

Figure 3: Meshed structure of asymmetric gate work function shorted gate FinFET

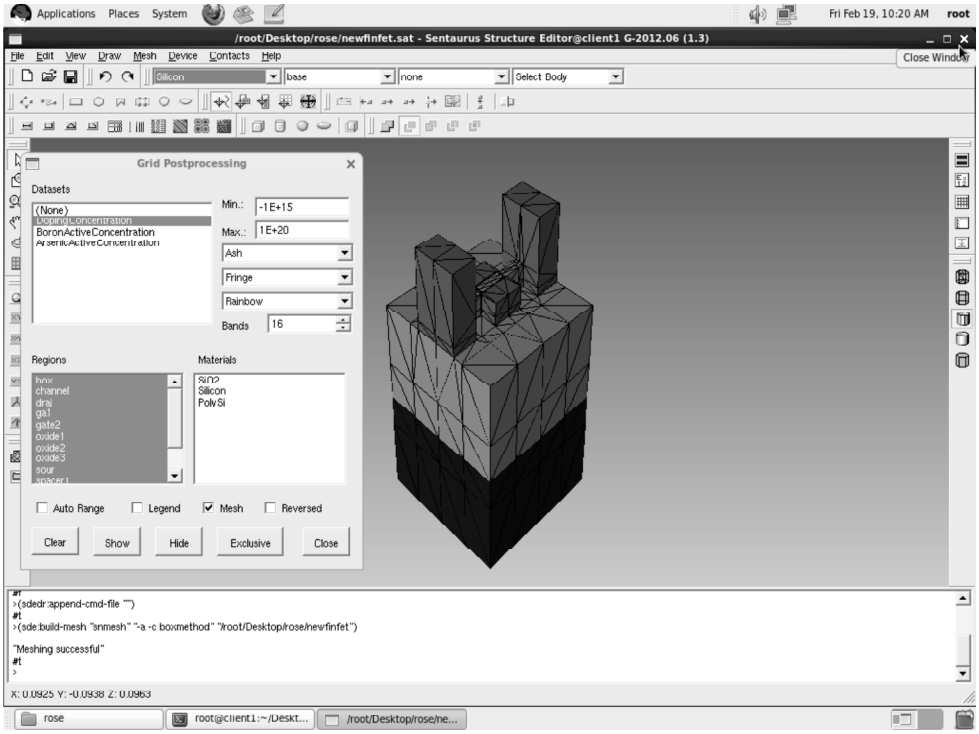

Figure 4: Meshed structure of Independent gate shorted gate FinFET

III. TRANSFER CHARACTERISTICS

We revisit the physics of shorted gate and Independent gate mode devices,to better appreciate the limitations of Symmetric work function devices and the advantages of Asymmetric work function FinFETs. Accounting for temperature effects, we performed hydrodynamic mixed-mode 3-D device simulations on carefully defined meshes (for excellent convergence) and invoked the density gradient model for incorporating

quantum effects in a thin fin. We ignored the effects of gate tunnelling currents due to the undoped fin, and used an effective oxide thickness that can easily be realized using thicker high-k dielectrics to suppress gate leakage. Fig. 5., Fig. 6., Fig. 7. shows the transfer curve of symmetric and asymmetric gate work function shorted gate and independent gate FinFET at VDS = 0.5

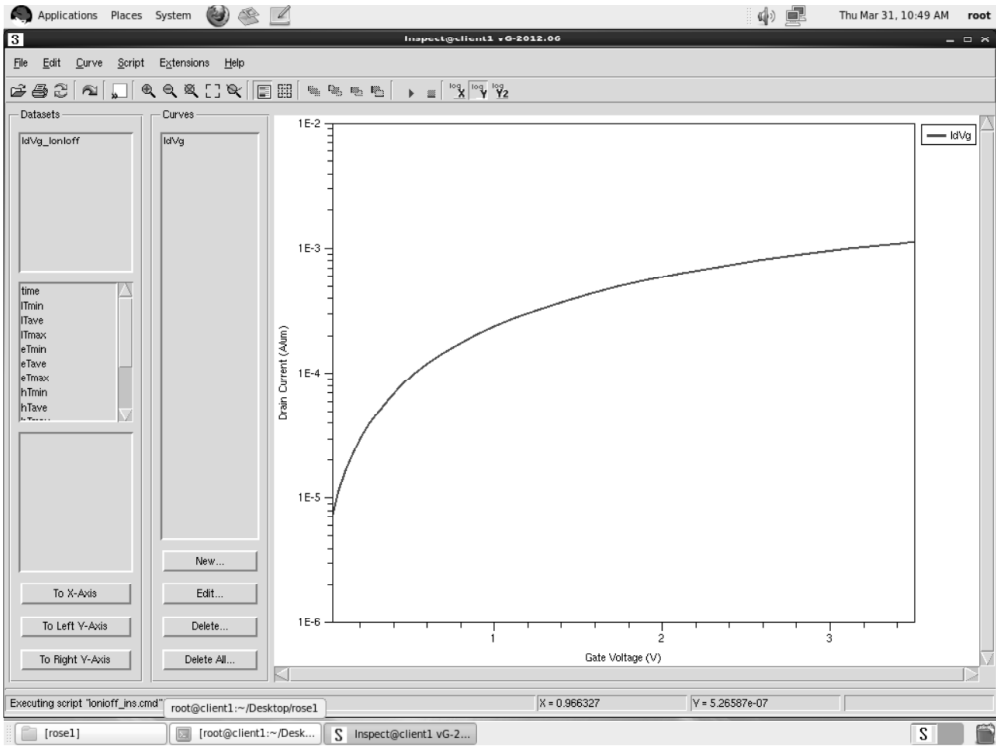

Figure 5: Transfer curve of symmetric work function shorted gate FinFET

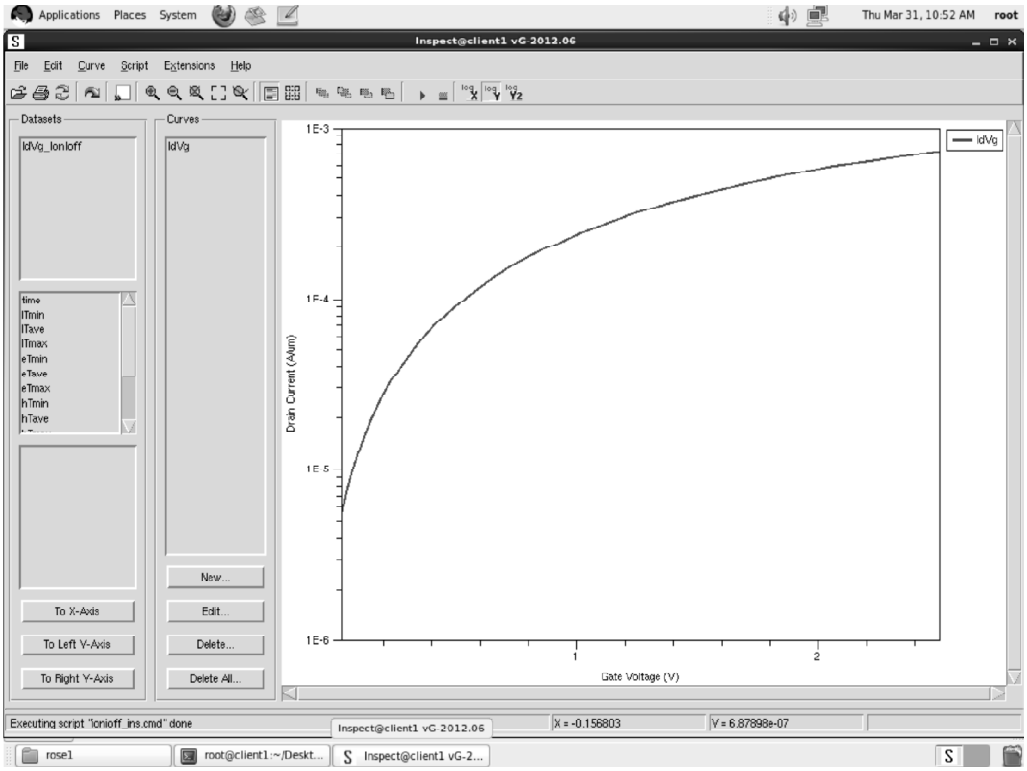

Figure 6: Transfer curve of asymmetric gate work function shorted-gate-FinFET

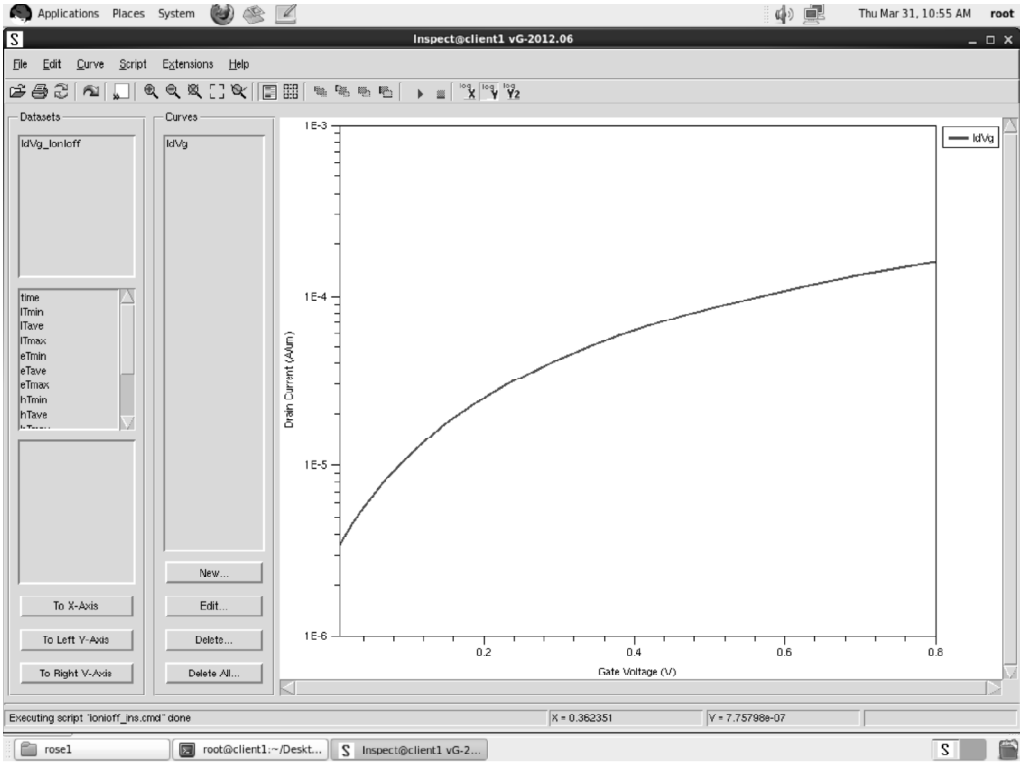

Figure 7: Transfer curve of Independent gate FinFET

IV. INFERENCE

Table 2
Compariosn of Onstate and Off State Current of Different Finfet Structure-S

	On-current(A)	*Off –current(A)*
Symmetric gate work function finFET	1.22×10^{-3}	7.54×10^{-6}
Asymmetric gate-work function FinFET	8.59×10^{-4}	4.65×10^{-6}
Independent gate finFET	1.562×10^{-4}	6.5×10^{-6}

V. CONCLUSION

In this paper, we evaluated Symmetric gate work function shorted gate /Independent Gate mode FinFETs and Asymmetric work function shorted gate mode FinFETs head to head in a high-performance process. Asymmetric work function shorted gate mode FinFETs with high-performance targets provide reasonably high ON-currents in comparison to Symmetric gate work function shorted gate/Independent gate mode FinFETs, and maintain their advantage at high temperature. This suggests that they could be widely used (in combination with Symmetric gate work function Shorted Gate-mode FinFETs when necessary) in off-critical paths.

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