

Development of FPGA Based Wireless Single Phase Induction Drive

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ABSTRACT

The main theme of this paper is wireless monitoring and control of single phase induction motor drive. The speed control is the key issue in the industrial applications. For the automatic operation of the drive the Field Programmable Gate Array (FPGA) is a better choice with the least cost. For control strategy the present research work highlights on the Pulse Width Modulation (PWM) scheme with FPGA. The design of such expected control is possible through Controller, PLC, PLA, FPGA, etc. The digital signals are generated by using the FPGA. The FPGA signals have the control on the pulse width which is used for firing of the inverter. The inverter supplies power to the drive as per the variation of PWM. Single phase induction motor control, using the simple PWM technique, is possible. The wireless operation is also possible with Dual Tone Multi Frequency (DTMF) technique. The system is capable to turn ON and OFF to the motor as well as it also controls the number of pulses per half cycle in PWM.

Keywords: Wireless monitoring, FPGA, PWM, DTMF

I. INTRODUCTION

In past, DC motors were used for control applications but due to certain disadvantages, these were replaced by the induction motors. With the development in technology, the precise control of process was required. Single phase induction motor has been used widely in discipline industry and household whereas simple motor starter can not let vary speed in starting and also running with mechanical load [1-3]. The single phase motors are simple in construction and easy to implement the software as well as control applications. The microprocessor and computer control of single phase induction motor implemented by various researchers [4-5]. Online monitoring and parameter estimation of induction motor has proposed by Uplane and et.al [6], while harmonic reduction schemes are represented by Krishnamoorthy and et.al for power control drives [7]. Many other authors have also implemented the various SPWM schemes [8-10].

The main idea of this research article is to control the PWM gating pulses of an AC motor drive by wireless communication using DTMF decoder technique which is implemented by an FPGA. In case of DTMF technique, every key has a unique tone, which is decided by the combination of keypad's column frequency and row frequency. The DTMF decoder splits the frequencies and then it converts the frequencies into binary values. Hence, the induction motor is controlled by pressing the different keys from the user's mobile unit. PLC based simulated mixer system was designed by Okoli and et.al. [11]. The vector control scheme using PWM was adopted by Zhang and et.al. [12] while the diagnosis of machine ripple effects was carried by F. Fillipetti and et.al [13]. In the recent years A. P. Ghatule, Kumbhar along with Rathod [14-15] have taken keen interest in developing the single phase induction motor drive.

In receiver section the mobile unit is interfaced with DTMF (Dual Tone Multi Frequency) decoder, the decoder detects the signal and then the decoded information is transferred to the Microcontroller unit. The controller unit controls induction motor with the help of control circuit using the PWM firing pulses.

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The system is designed around the FPGA which is commonly used in embedded applications for computing and smart decision-making capabilities to machines, products, and processes. FPGA is capable to interact with number of automated systems. The MicroC software, by Microchip is used for debugging the source code of FPGA and simulated. The simulation helps to build the circuit and avoids the delay and efforts of the human.

II. SYTEM DESIGN

Speed control plays an important role in the industrial processes. There are number of control strategies employed depending on the type of the process used. The different control strategies are also developed by various research fellows. The developments based on FPGA as well as control techniques have made the system more flexible for its operation. The initial trend of growth of control technique was less but the present rate is very high due to the development of modular and compact automated devices using the controller technique and the software simulation implementation in the control strategy. The feedback control with the DTMF control is used for the present system. Due to the feedback system the corrective action is also implemented in the present system. The simulation made the system design easier and its implementation with easier testing conditions. The FPGA is used to generate various types of PWM pulses for driving the gate of the MOSFET. The pulse width is varied to drive the gate of inverter MOSFET

The system design consists of FPGA board, DTMF card, antenna, Mobile unit in auto answer mode, signal driver power supply, etc. as shown in Figure 1.

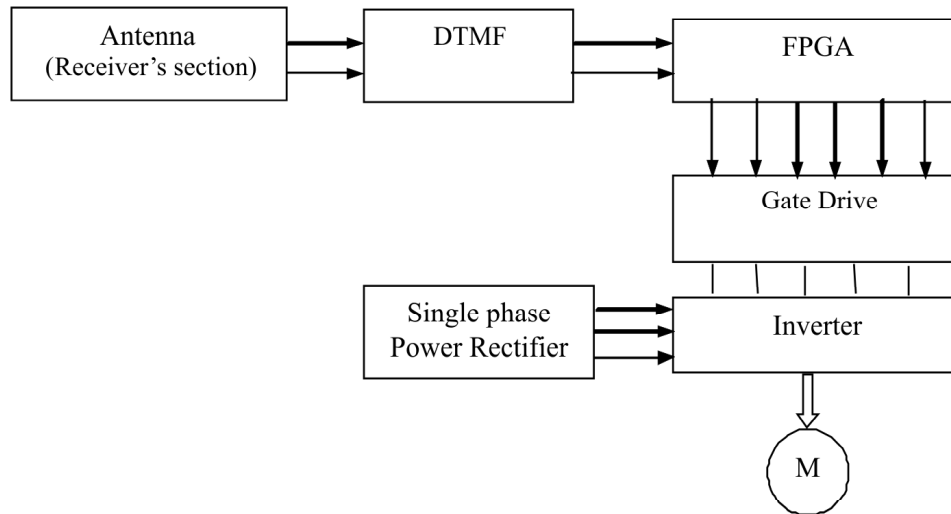


Figure 1: Block diagram of FPGA based DTMF drive

2.1. Inverter module

The inverter model is designed with the use of four power MOSFETs which acts as fast switching device. The H bridge uses MOSEET's to improve the efficiency of the bridge .The four MOSFETs which are controlled by the PWM signal generated using FPGA. The firing sequence is G_1G_4 and G_2G_3 and repeated. The width of the pulse decides the conduction of MOSFET and hence, the power supplied to the drive also varies and the speed also changes. The width of the pulse is controlled by using the software through FPGA.

The capacitor bypass the transient current generated during the switching of PWM through inverter. Depending on the pulse width of the firing pulse, the firing of the inverter takes place and proportional power is supplied to the drive. Figure 3 shows the implementation of MOSFET based inverter control module.

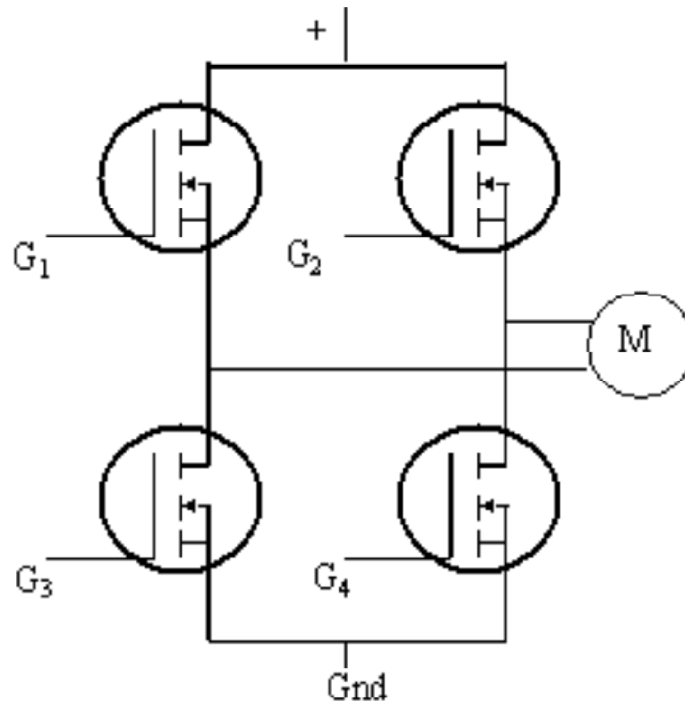


Figure 2: MOSFET Inverter

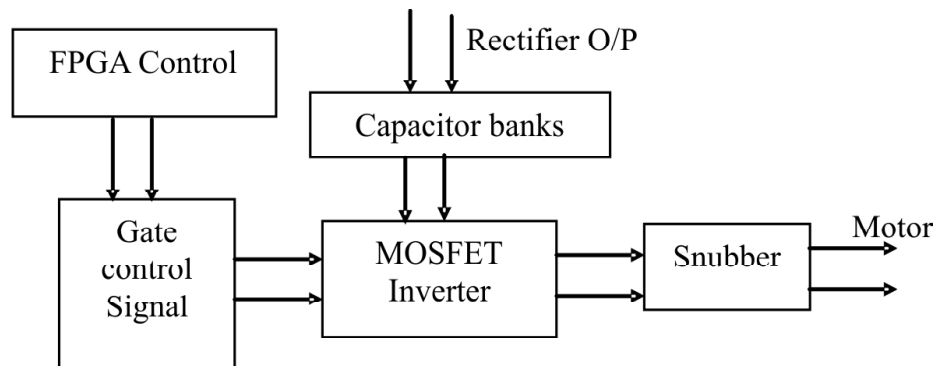


Figure 3: MOSFET Based Inverter Control

The power is supplied to the MOSFET based inverter through the power rectifier KBP 2510. This gives DC voltage of the 230V AC input. The high voltage capacitor banks are connected across the inverter which helps in rectifying and provides the bypass path to the AC. The snubber circuit consisting of inductor transistor, diode is used in series with the load to avoid the surge pulses generated during the firing of the inverter. The buffer amplifier is used to increase the signal strength of firing of the inverter. The isolator MCT2E is used to isolate the power circuit from the control circuit. Figure 4 shows the firing pulses generated by the FPGA and used for firing of the inverter. Each pulse will conduct the pair of MOSFETs little less than 180° .

III. DTMF CONTROL

This system is used in telephone for voice frequency; the signals passing through the telephonic line are in the frequency. It has different tone frequency signals representing sixteen different numbers and symbols. The DTMF [17] is nothing but the dual tone multiple frequency dialing method used in the telephonic system. The combination of lower group and higher group frequencies forms the single tone as output represents digit and symbol. These are placed in rows and column matrix form having 4 rows and 4 columns.

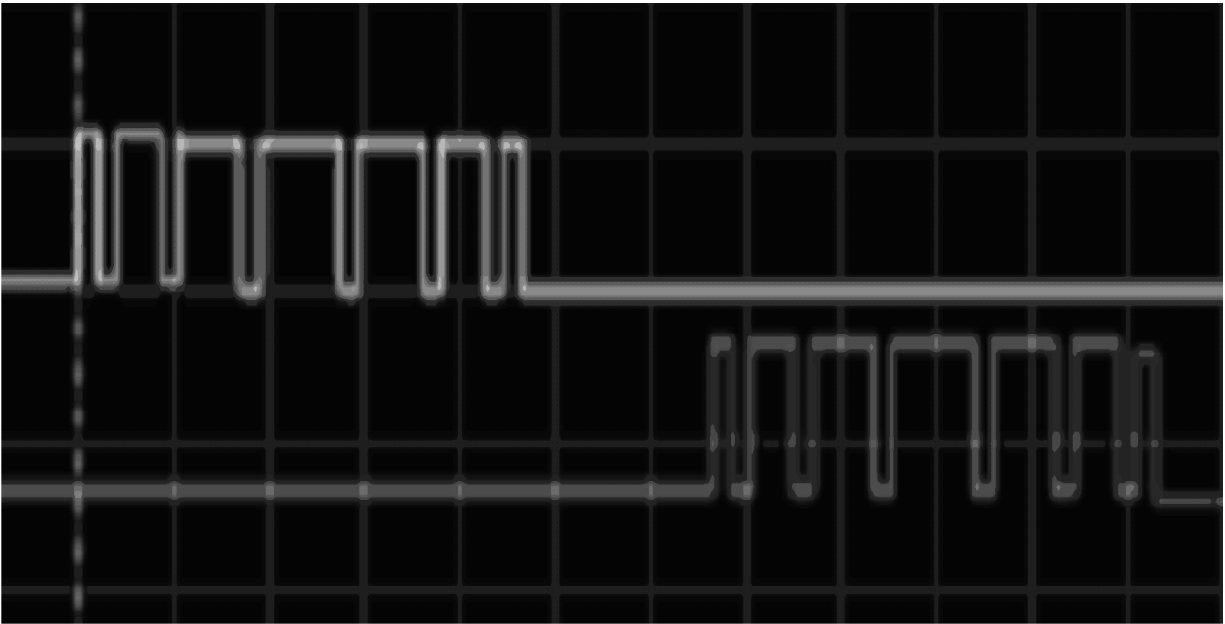


Figure 4: PWM pulses used for firing of MOSFET

Each digit or symbol is represented with combination of row and column together. The DTMF dialing is faster in operation. It can be operated with pulse or tone. Tone dialing is having advantage over the other. In DTMF two pure tones of pure sine wave are mixed and operated for getting the signal with multi-frequency signaling. After mixing the lower group frequencies with the higher group frequencies the digit or symbols are represented as shown in the Table 1.

Table 1
DTMF output to FPGA

<i>LG(Hz)</i>	<i>UG (Hz)</i>	<i>Digit</i>	<i>OE</i>	<i>D₃D₂D₁D₀</i>
697	1209	1	1	0000
697	1336	2	1	0001
697	1477	3	1	0010
770	1209	4	1	0011
770	1336	5	1	0100
770	1477	6	1	0101
852	1209	7	1	0110
852	1336	8	1	0111
852	1477	9	1	1000
941	1209	0	1	1001
941	1336	*	1	1010
941	1477	#	1	1011
697	1633	A	1	1100
770	1633	B	1	1101
852	1633	C	1	1110
941	1633	D	1	1111
		Any	0	zzzz

LG Lower Group of frequencies UG Upper group of frequencies

Table 2
Decoder Action Performed

<i>Number pressed by user</i>	<i>O/P of Decoder</i>	<i>Action performed</i>
0	0 x 00, 00000000	Line voltage checking
1	0 x 01, 00000001	ON
2	0 x 02, 00000010	OFF
3	0 x 04, 00000100	Status of motor
4	0 x 05, 00000101	Speed check

Different functions shown in the tabular format are carried out with the help of the decoder. User by pressing the various numbers the action performed are indicated. The DTMF decoder; M-8870 is used for wireless communication. DTMF receiver is constructed by using the IC technique with complementary MOS technology with decoder integrated function. It is operated with low power and can be able to handle with great precision. The data management is done by using the FPGA. It's digital counting helps to determine the frequency tones. The digital output of FPGA is given in table 1. while working button pressed at one end is heard at the other end with specific tone and processing done by using the FPGA using specific coded software. Use of mobile is one of the techniques gained large importance in the remote control technique that can have ability to control throughout the globe using the mobile frequency range. Table 2 shows the functional decode table of MT8870.

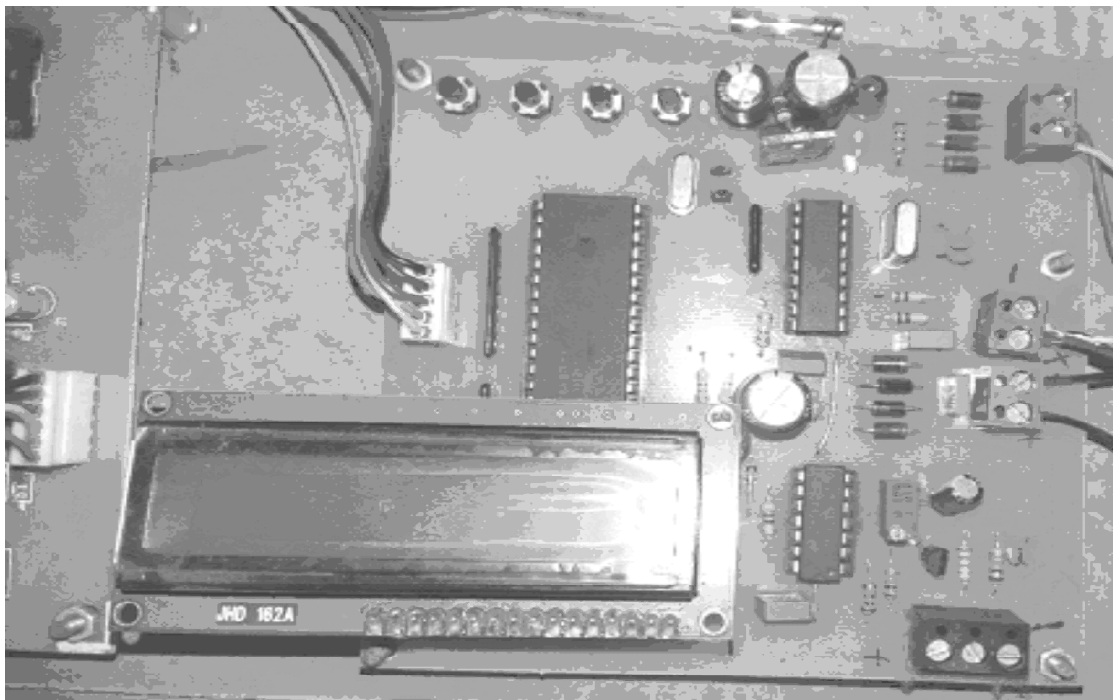


Figure 5: Actual DTMF circuit

The software is written in assembly MicroC language for reading the various parameters. Initially the various drivers are initialized and line voltage is checked if the line voltage is not present it will send the message “ Line voltage is not present” After proper voltage it will ask to enter number between 0 to 4 for reading various parameters. By entering 0 the line voltage is checked. After checking the line voltage it will show the status of the line voltage whether it is present or not. By pressing 1 or 2 ON or OFF the motor action is carried out. By entering the number 3 the current status of the motor is represented and by entering the 4, the speed of the motor is displayed.

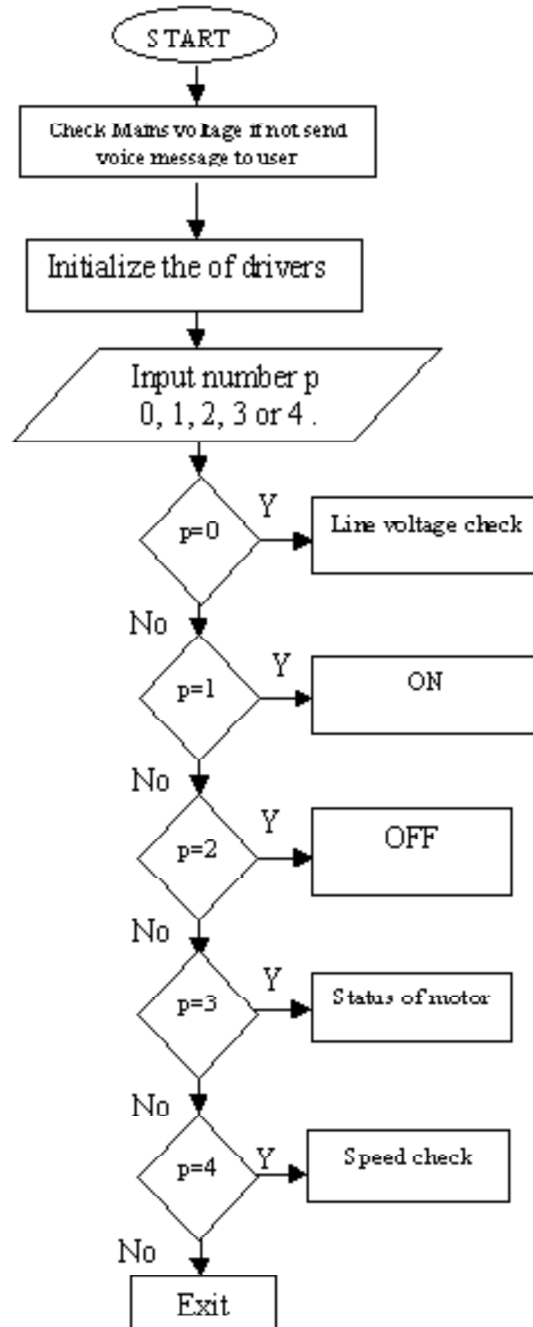


Figure 6: Flow chart of the main routine

IV. RESULTS AND CONCLUSION

The speed efficiency characteristics are shown in Figure 7 for three and five pulses per half cycle. By increasing the number of pulses per half cycle decreases the harmonic contents. However increase in the number of pulses per half cycle increases the switching losses.

It is observed that the variation is linear up to the speed 1050 rpm and then efficiency decreases. It is also observed that as the speed increases the efficiency also increases till 1050 rpm. The best firing scheme is seven pulses per half cycle should be implemented for better results and efficiency of the machine.

The precise speed control of the motor is possible from the remote place using the DTMF technique. The firing of the inverter is done by PWM pulses generated by the FPGA. The variation of the pulse width

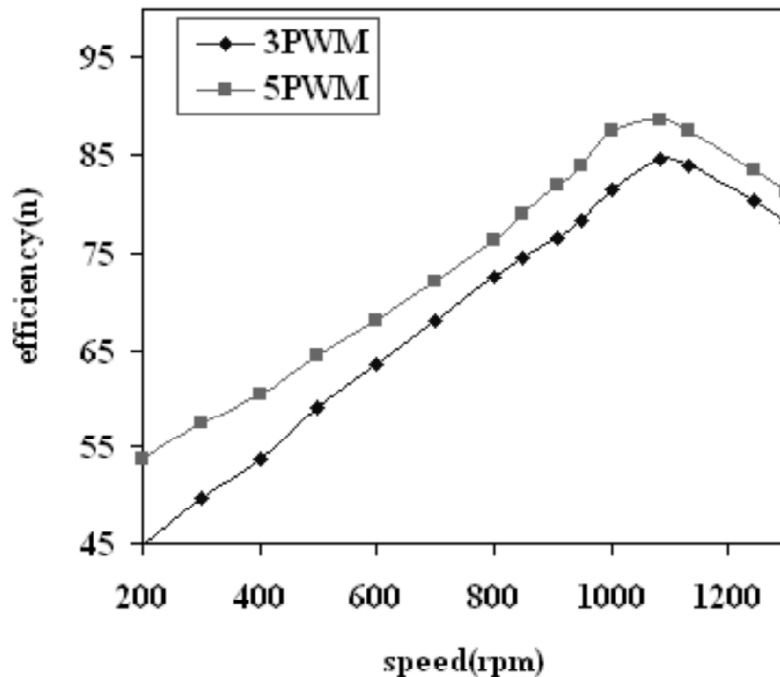


Figure 7: Speed efficiency characteristics

generated by FPGA varies the speed. The width of the firing pulse controls the power and hence the speed of the drive. The results indicated are well within the acceptable range. The deviation in the results is due to the losses in the machine and switching of the inverter. The developed drive is suitable for the industrial application.

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