Fault Detection of Single Phase Induction Drive Motor using the FPGA

Mukesh Payak, Y.K.Vijay and S. R. Kumbhar

[1] Department of Electronics and Communication Engineering, Vivekananda Global University, Jaipur , Rajasthan, India
E-mail: payakmukesh@gmail.com,vijayyk@gmail.com
[2] Department of Electronics, Wilingdon College, Sangli, Maharastra, India, E-mail: srkumbhar@gmail.com

Abstract: Due to revolution in industry in the latter half of the 19th century the simple drives were replaced with horse powered and then mechanical drives. In the modern era, the mechanical drives were further replaced by electrical drives for the motion processes. The developed AC drives dominate the industrial applications in the present scenario. The operation of power drives is generally based on the switching capabilities of power semi-conductor devices. Researches in semiconductor technology improved switching techniques & in turn control processes. The drives are used in variety of applications. Industrial application requires smaller, lighter, high performance & control drives. Large number of the complicated processes are operated with drives and failure of the drive will hamper the desired process and hence the production loss. To avoid this fault detection techniques are developed which can monitor the process simultaneously and able to find the fault in the given time. The Microprocessor, personal computer (PC), Microcontroller based fault detection for the single phase induction motor is carried out. However, the Control parameters available are much less. So to find the requisite fault in the given time is somewhat time wastage and hence the loss of the capital. In the present Investigation the field programmable gate array (FPGA) based fault detection technique is implemented. The required software is written in the MicroC-5 which will help in diagnosing the fault of the system and displays. At the same time, the redundant drive manages the process of the system without any intervention of the system.

Keywords: Fault detection, FPGA drive, Inverter drive, Single phase induction motor drive

I. INTRODUCTION

Drives have gone through number of changes and are used in different industrial applications. The improvement in the switching techniques development has gone towards the Modular concept using the PC, Microprocessor, Microcontroller, programmable logic controller (PLC), etc. For the same, initially induction motor and its parameter estimation were carried by Uplane and *et.al.* [1].The use of PC using the software switching techniques improves the performance. This PC based drive was found to be better over the conventional one. The fault detection method also helped the process to operate drive without fail. The redundancy in the drive has gained importance & such drives are developing rapidly. To have better control over the process the microcontroller and the PLC based drive has designed and developed [2,3] and operated in the industrial applications. The three phase induction motor drive developed by Uplane and *et.al.* [4] with PWM techniques and its performance showed better over

the previously developed drives. The drives started developing in the complex manner and the implementation of the FPGA based fault detection of single phase drive carried by Xilinx software and was implemented by R. Thejaswini and R. Sindhuja [5]. Many people developed the system with PLC and controller based [6-9].

Still, the control and monitoring of various parameters online, the use of FPGA plays an important role and the industrial process requires complex processes to handle so the design of FPGA MOSFET based inverter design is necessary. The present article highlights the design and development of fault detection of FPGA based induction motor.

II. SYSTEM DESIGN

The speed control techniques are the important part in many industries. The different control strategies are employed depending on the type of the process used. The different control strategies are also developed by different research scientists. The development in semiconductor and its design made the system more flexible for the control. The initial trend of growth of control technique was very poor but the present rate is very large due to the development of semiconductor devices and the software simulation implementation in the control strategy. The feedback systems are prominently used which have the ability to detect errors in the parameters sensed and also to take the corrective action. The accuracy in the control is one of the major part which is easily possible through software along with the required hardware. In the present situation, the FPGA will generate the pulse width modulated (PWM) pulses whose width can be varied using the software. The required PWM firing pulses are generated by the FPGA, to control the gain of the inverter. As the pulses generated by FPGA are not quite sufficient to drive the gate of insulated-gate bipolar transistor (IGBT) of inverter therefore, buffer and amplifier are used. The isolation is required to separate power circuit from the control circuit. The width of the firing pulse generated is controlled by the FPGA which is as shown in Figure 1.
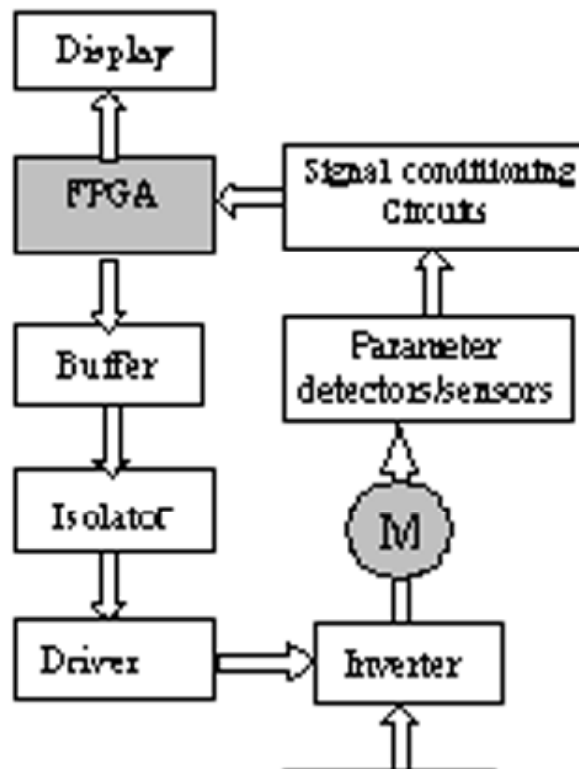

Figure 1: Block diagram of single phase inverter drive system
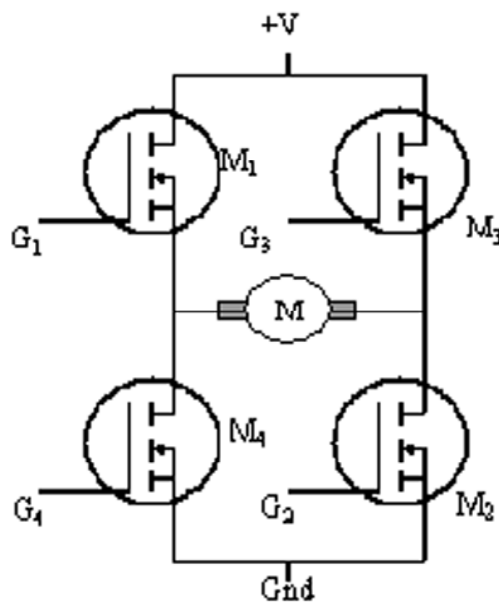
III. FAULT DETECTION

Recently industries uses lot of complex processes and to operate them the complicated control circuits are involved. At the same time many parameters are managed, so due to complexity, abnormal process or input conditions, or surrounding conditions fault is likely to occur in the system. The fault management is tedious and a time consuming job. Therefore, to find the fault quickly and also the exact location, the software is developed in MicroC5. The method of fault detection helps to reduce the time of repair. In the present situation the voltage of the main drive is continuously sensed. If the fault occurs in the main drive, the voltage will change and the software will transfer the working of motor to redundant drive and starts fault finding and displays the fault in the Figure 4 shows the complete configuration of the fault detection system. The fault detection block diagram consists of FPGA, redundant drive, main working drive, various parameter sensors and detectors along with their signal conditioning circuits. Using the various sensing techniques the line voltage, rectified voltage, current of motor, speed, etc. were sensed. The data read from FPGA is compared with the standard data and the logical conditions were set for comparison.

The firing PWM pulses are generated through software using FPGA. The isolator circuit requires the 15 mA current for its working the input PWM pulse generated using FPGA and its driving capability is 5 mA. So it is essential to boost its current capability and is done by using buffer, output of which drives the LED and opto-coupler called the gate driver. The inverter is fed with DC supply from the rectifier and fired by the PWM pulses which provides the proportional voltage to the motor. The supplied voltage is continuously sensed through channel 1 of ADC using the voltage sensing circuit. The sensed data is compared with standard data stored. If the compared data is not within the acceptable range, the firing pulses are generated using other port of FPGA and
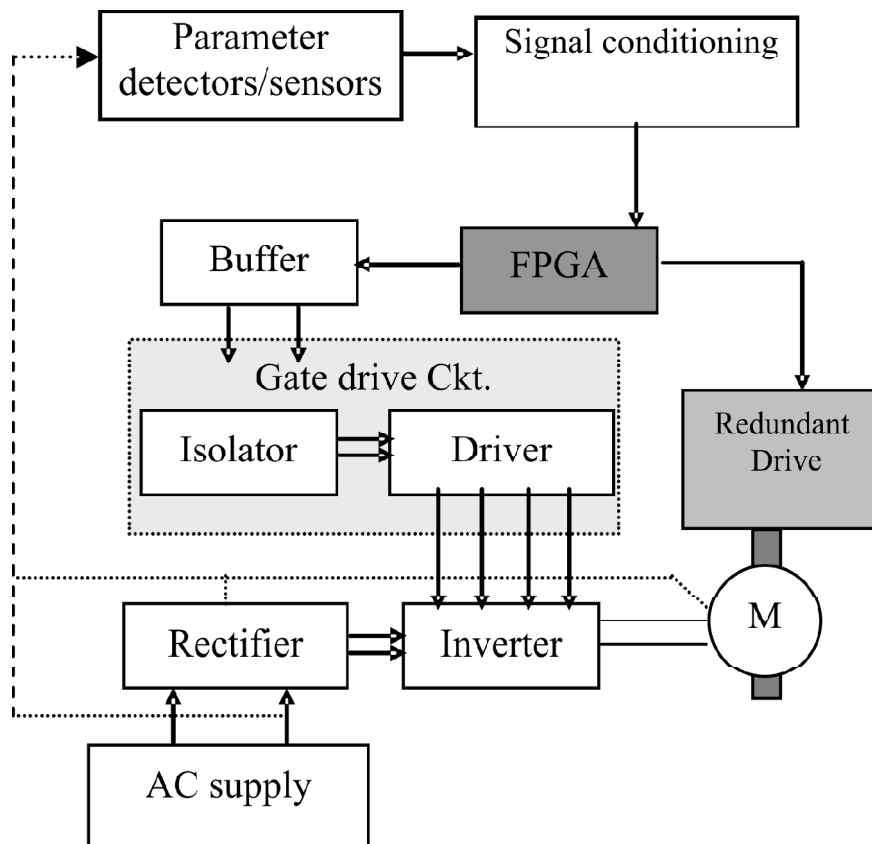

Figure 4: Fault detection block diagram of single phase drive

are used to turn-on the redundant drive and hence switching takes place from main drive to redundant drive. The process continues to operate through redundant drive and the FPGA starts scanning the input channel data for rectifier voltage. Initially FPGA checks the AC line voltage sensor data through channel 2. The requisite channel data is sensed and compared with the standard data. If it is below the permissible range then line voltage fault message is displayed on the monitor and process returns for generation of the PWM pulses. After every half cycle one parameter is checked. Also getting the line voltage or with no fault the FPGA scans the next parameter. After the diagnosis of the rectifier fault the FPGA scans the firing pulse of the first MOSFET through the next channel, if the fault in gate drive then displays and like way after scanning four gate parameters. Therefore, after six half cycle the fault detection process gets completed. If all the conditions are all right then the main drive is ready for the operation. The software switching takes place from the redundant drive to main drive by switching the redundant drive input pulses.

IV. PARAMETER SENSING

The various parameters are sensed using the following circuits-
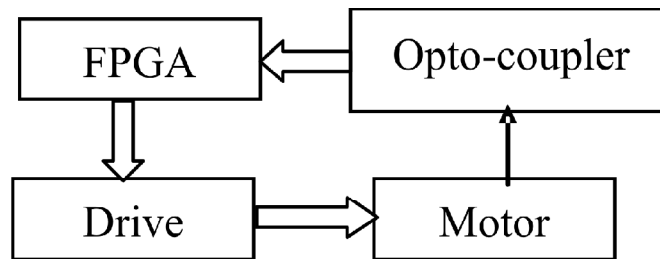
4.1. Speed sensing

Figure 5: Speed sensing arrangement

The opto-coupler is used for speed sensing [11] which consists of LED and Detector. The disc is connected to the motor shaft and to its periphery one hole is drilled. The arrangement is made in such a way that disc rotates in between LED and detector which provides one pulse for every rotation. The number of pulses is counted for a particular time interval through FPGA and corresponding speed is indicated. After comparison of the data with standard data if necessary correction factor is implemented through the software.

4.2. AC Voltage Sensing Circuit

The peak detector is used for the AC voltage sensing which is shown in Figure. 6. The voltage across the inverter through sstep-down transformer is sensed by the peak detector and corresponding change in the peak detector
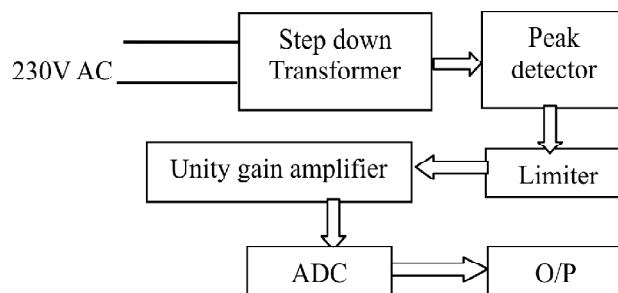

Figure 6: Voltage sensing by peak detector circuit

through ADC gives the proportional voltage in the range of 0-5V. The software represent the correct voltage across the inverter which is implemented through software. The 0-5V is scaled to represent 0-230V.

4.3. DC Voltage Sensing Circuit

The potential divider is used for the DC voltage measurement. The fine quality of two resistors forms the potential divider. The input voltage is given as shown in the Figure 7 and proportional developed voltage is given to the OP-AMP and finally to the ADC channel which gives the proportional voltage. The measured voltage by the FPGA is between 0 to 5V which is proportional to 0 to 250 V. The measured voltages are scaled through the software to achieve the range of 0 to 250 V.
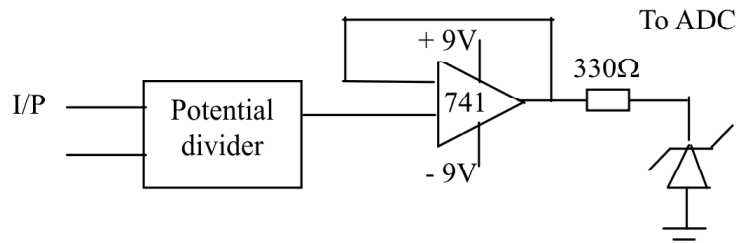

Figure 7: DC voltage sensing circuit

4.4. Current sensing

The current sensing is done by using the good quality of shunt wire. For the current measurement, the following circuit configuration is used which is shown in Figure. 8. The current which is to be sense is passed through 1 W good quality resistance which develops a potential proportional to the current across the two terminals of the resistance. The developed potential is given to the step down transformer which gives proportional current in the range 0-5 A. After scaling and applying the correction factor the correct current is represented.
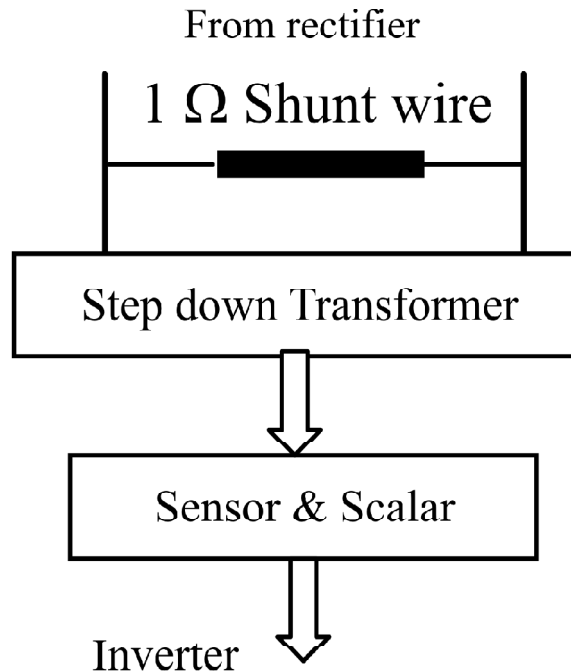

Figure 8: Circuit Sensing Experimental Arrangement

V. FLOW CHART OF THE FAULT DETECTION

The beginning of the fault detection starts with the initialization of the system interfacing circuits. By selecting the appropriate address, port is selected. The various parameters to be checked are given to various channels. The primary flow chart of the fault detection is shown in Figure 9.

Initially, check the line voltage through the voltage sensor. If there is a fault in the line voltage then it displays otherwise check the rectifier voltage after finding the rectified voltage correct it will check one by one the gate firing pulses. If the fault is in the firing pulses respective fault is displayed. After getting all the faults corrected by the system automatically, transfer to the main drive.
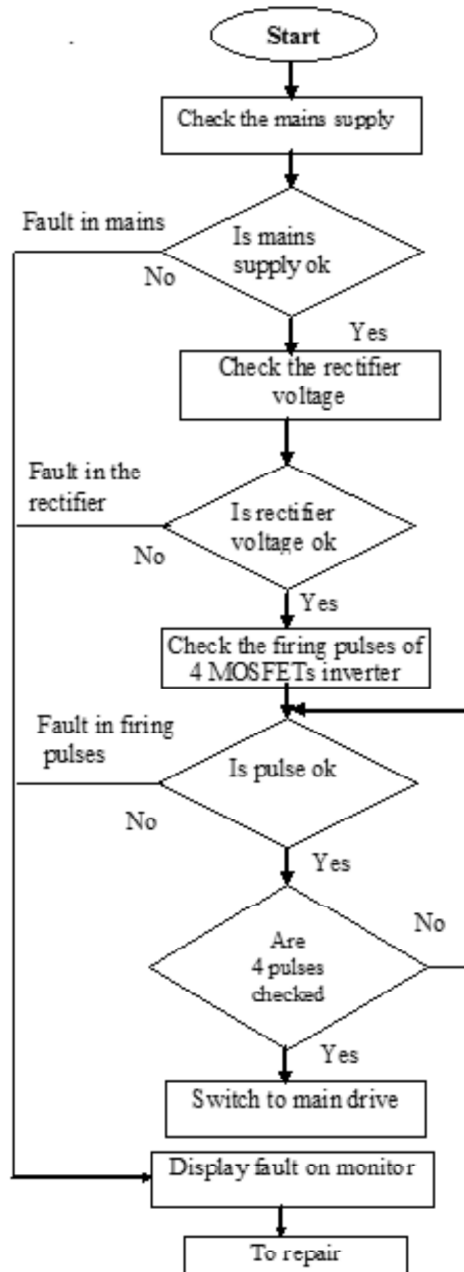

Figure 9: Flow chart for fault detection

VI. RESULTS AND DISCUSSION

To avoid the termination of the process the fault detection technique is developed which can monitor the process simultaneously and will be able to find the fault in the given time. FPGA based fault detection for the single phase induction motor is implemented. The PWM technique is implemented for the variation of the speed and the power supplied to the load. At the same time, the redundant drive manages the process of the system without any intervention of the system. The software based system is designated and simulated. After simulation, the various sensing circuits are assembles and tested. Then, the combined result of the working system is taken. However, the results of the speed, voltage and current measurement is quite comparable with the standard parameter. But there is a slight deviation in the actual results which is due to the machine losses and also due to the instrumental errors. The system has working and redundant drive. So, after detecting the fault in the working drive it will transfer its process on the redundant drive.

This system is quite suitable in finding the faults of the drive and without hampering the normal process it will locate the fault.

REFERENCES

[1]   M. D. Uplane, S. R. Kumbhar, M. S. Gaikwad, M. S. Chavan," Data acquisition system for simulation and online parameter estimation of induction motor using computer", Journal of IETE, New Delhi, Vol.41, 2000, pp. 23-28.

[2]   S. K. Rathod, S. R. Kumbhar, PLC Minor research project Submitted to UGC WRO, 2015.

[3]   Maria G. Ioannides," Design and Implementation of PLC based Monitoring Control system for Induction motor", IEEE Transactions on Energy Conversion, Vol. 19, No. 3, Sept 2014.

[4]   S. R. Kumbhar, A. P. Ghatule, M. D. Uplane, "Design of single phase induction motor drive and its fault detection using personal computer", International journal of research in computer Science and information technology, ISSN: 2319-5010, Vol. 1, Issue 1, 2012, pp 33-37.

[5]   R. Thejaswini and R. Sindhuja, "Voltage/ frequency control of induction motor using FPGA", International Journal of Emerging Engineering Research and Technology, Vol. 2, Issue 2, May 2014, pp. 101-106.

[6]   E. Monmasson, Contributions of FPGAs to the control of electrical systems - a review, IEEE Industrial Electronics Society Newsletter, 2003.

[7]   A. A. Kalage, V. M. Jape, S. V. Tade, M. M. Hapse and R. G. Dabhade, "Modelling and simulation of FPGA based direct torque control of induction motor drive", International Journal of Recent Trends in Engineering, Vol.1, no.4, May 2009, pp. 72-74.

[8]   G. Mailloux, S. Simard, R. Beguenane, "FPGA implementation of induction motor vector control using Xilinx system", 6th WSEAS International Conference on circuit, system, Electronics, control and signalprocessing, Cairo, Egypt, Dec. 2007, pp. 252-257.

[9]   Young S., Kang G., "Simulation of New Lateral Trench IGBT Employing Effective Diverter For Improving Latch Up Characteristics", J. Microelectronics, Vol. 32, 2001, pp. 749-753.

[10]   Mukesh Payak, S.R. Kumbhar,"Development of FPGA based wireless single phase induction drive", International Journal of Control Theory & Applications, Vol. 9, 2016, pp. 8533-8540.

[11]   Mukesh Payak, S.R. Kumbhar, "FPGA based PWM Control of Induction Motor Drive and its parameter estimation", International Conference on Applied and Theoretical Computing and Communication Technology, IEEE 2015, pp. 631-635.