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Design of DM² Adder with Low energy and High speed

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ABSTRACT

In this paper, DM² Adders designed for low energy and high speed. This adder is proposed by combining two independent techniques DMADD (Dual mode addition) and DML (Dual mode logic). DML is a special gate topology that allows on-the-fly adjustment of the gates to real time system requirements, and also shows a wide energy-performance trade-off. DMADD is odds based circuit architecture with a huge energy-performance trade-off. But when DMADD used in pipelined processor, it requires extra clock cycles sometimes. So to avoid this, DML is applied in DMADD, thus it became DM² Adder.Here DM² adder is implemented in 180nm process technology and was designed with Cadence's Virtuoso tool.

Keywords: Adders, DML, Low Energy and high speed

1. INTRODUCTION

Primary goal is to obtain energy efficiency and low peak power while providing computational performance in contemporary processor design. Performance improvement and energy reduction have been studied extensively from the very high level of application algorithms, through system, architecture and logic levels, to the gate circuit, device and interconnect levels. Finally, energy reduction on the basis of pipelined digital systems has also been studied.

This also associates with the advance engineering levels and proposed gate. It shows how the combination of these independent methods yields great performance enhancement and energy efficiency.

The first method is dual-mode addition (DMADD). It takes advantage of the carry probability to produce low-power addition. However, it requires some pipeline modifications to support multi-cycle addition. The alternative method is a logic gate topology which is otherwise termed as dual-mode logic (DML) comprising the static and dynamic operation modes within the same gate.

In this paper we come across Squared Dual Mode DM² approach combining DMADD and DML. DM² main objective is to eliminate the DMADD and the use of multi-cycle addition by replacing its ordinary CMOS logic with DML, thus avoiding the architectural overheads. Furthermore, DM² enables considerable energy savings due to the inherent properties of the DML gates.

2. DMADD-DUAL MODE ADDITION

This adder is designed for the expected longest carry rather than the worst-case. The addition completes within a single clock cycle with minimum energy for most cases, while few additional cycles are required and in a very small probability.

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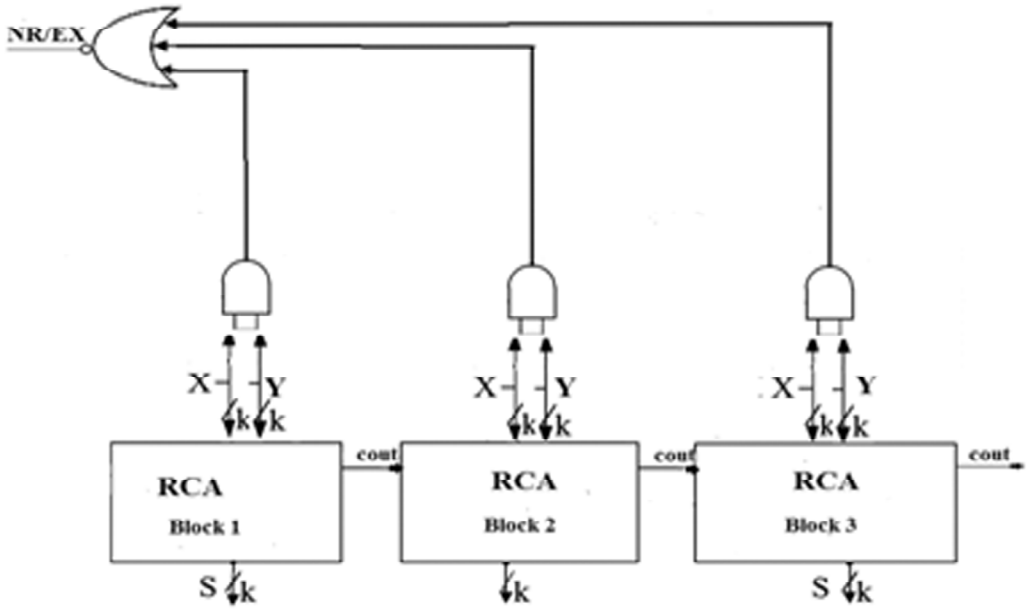

Figure 1: Dual mode addition topology

DMADD comprises two addition modes. The energy efficient one-cycle mode, called normal, is used most of the time to properly compute addition. It takes the benefit of tolerable (expected) longest carry in addition.

The other approach, called extended, occurs very infrequently and requires several clock cycles to properly add. The decision of which approach should turn up requires an appropriate control circuit. When this control is used in a pipelined processor it selects the appropriate method at the instruction decode (ID) stage, prior to the ALU stage.

A dual-mode adder is working either in a single clock cycle (normal-mode), or in multi cycles (extended-mode). The adder properly computes within a single clock cycle when the longest carry does not exceed k

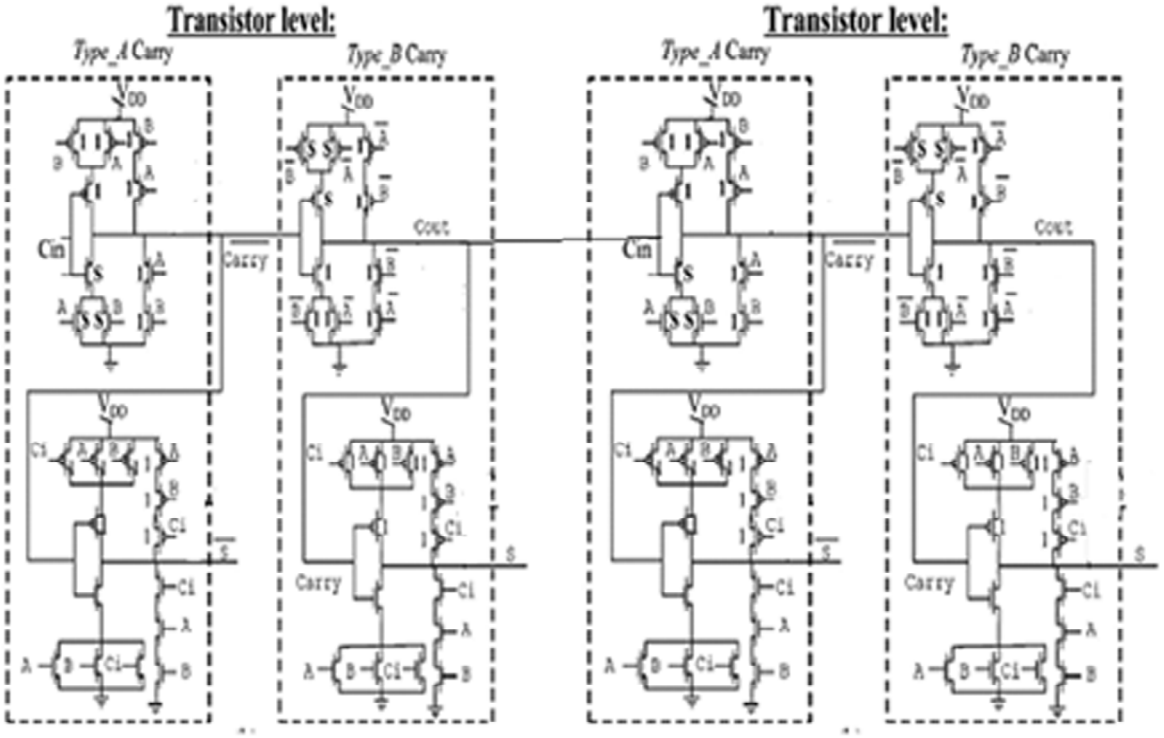

Figure 2: Ripple Carry Adder with alternative polarity full adders

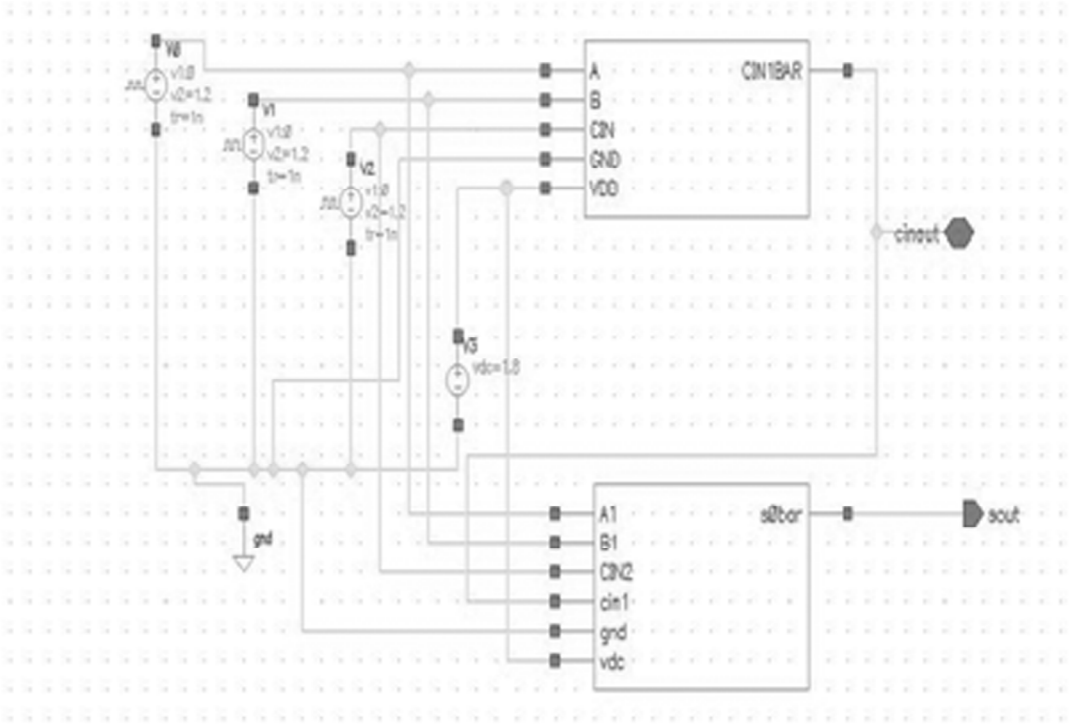

Figure 3: Schematic of full adder in DMADD

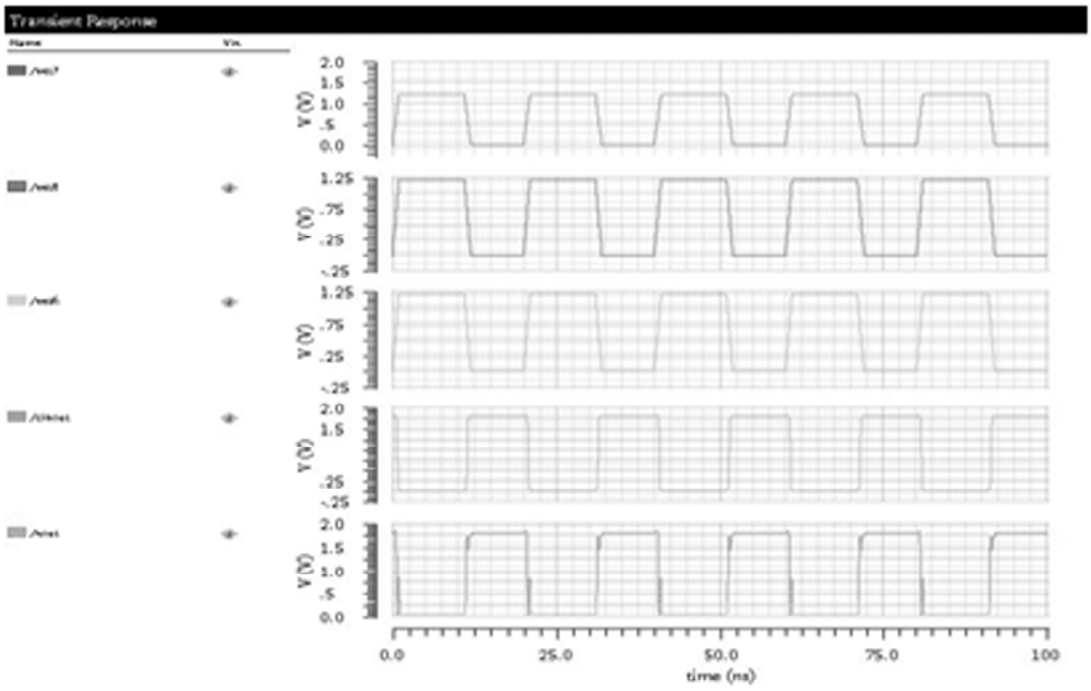

Figure 4: Transient response of full adder

bits. If the longest carry exceeds k bits, the adder will use additional m-1 clock cycle to properly complete its computation.

The setup of DMADD in an in-order pipelined processor requires stalling the pipe for m cycles in case of extended- mode addition. This imposes some design overhead and performance degradation. More severely, DMADD in out of order architectures may be extremely difficult. Here we can find how DML avoids the extended, multi-cycle mode. It ensures that regardless of the carry propagation, the DMADD will always properly compute within a single cycle

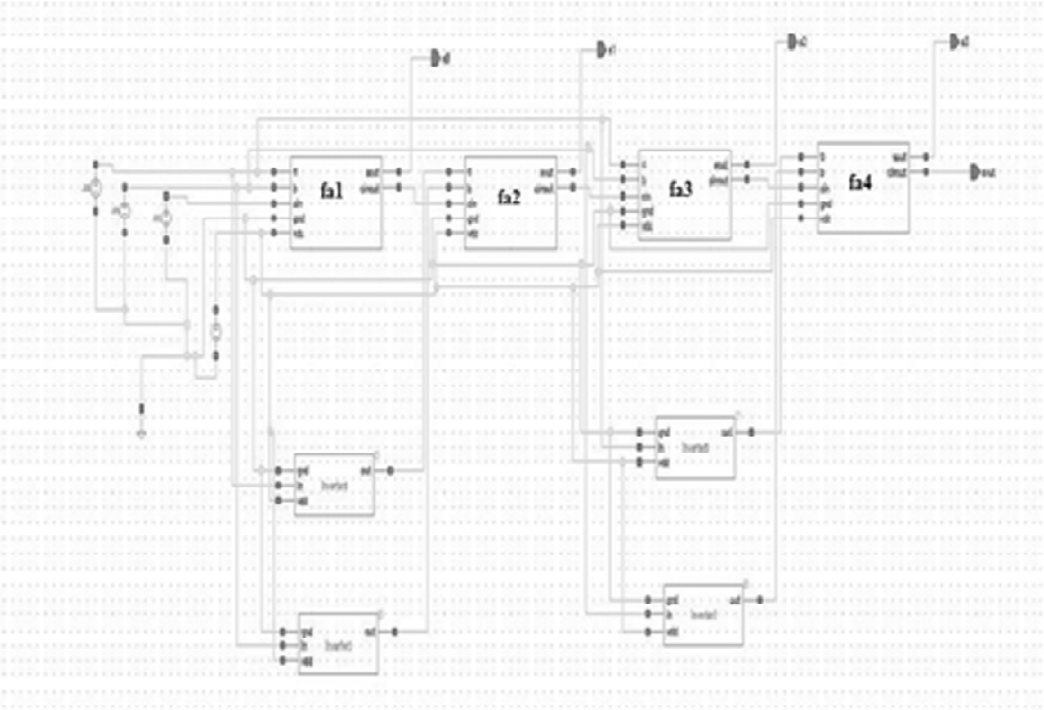

Figure 5: Schematic of Ripple carry adder with alternative polarity full adders

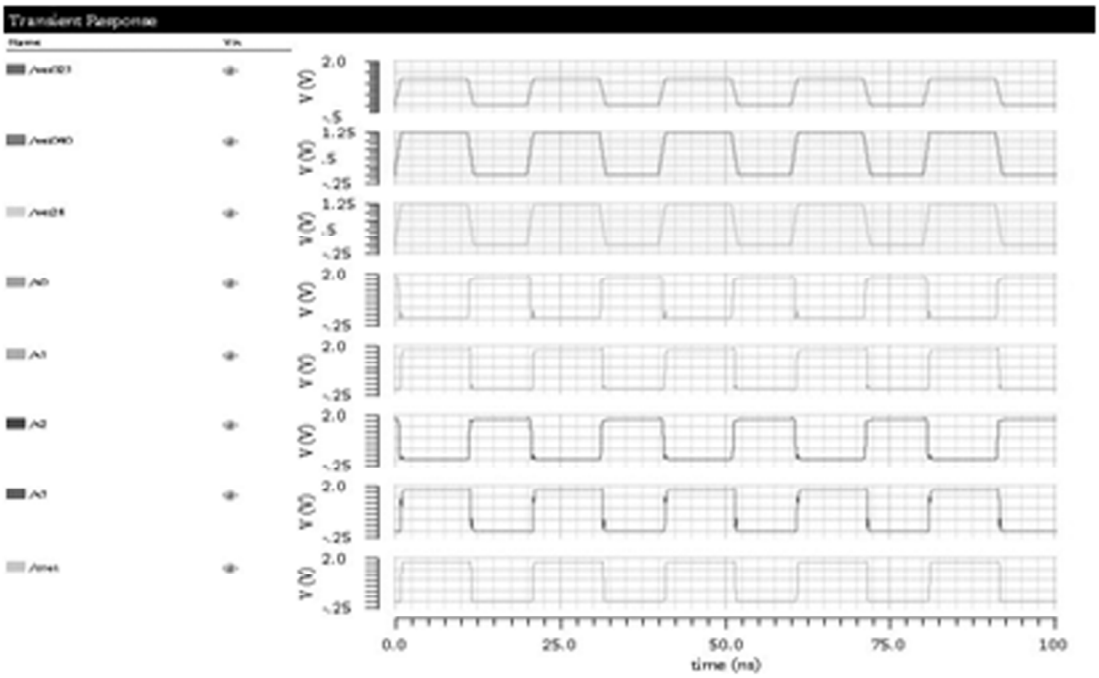

Figure 6: Transient response of ripple carry adder

Using three ripple carry adders, DMADD is designed. Here if cout is 1, it takes extra cycles to complete addition. So we should make cout as 0 by using DML logic in RCA.

3. DM² ADDER

When DMADD is used in pipelined processor, it goes to extended mode rather than normal mode. In extended mode, it takes extra clock cycles for addition. So to avoid this extended mode, DML logic is inserted in DMADD, thus it becomes DM² adder.

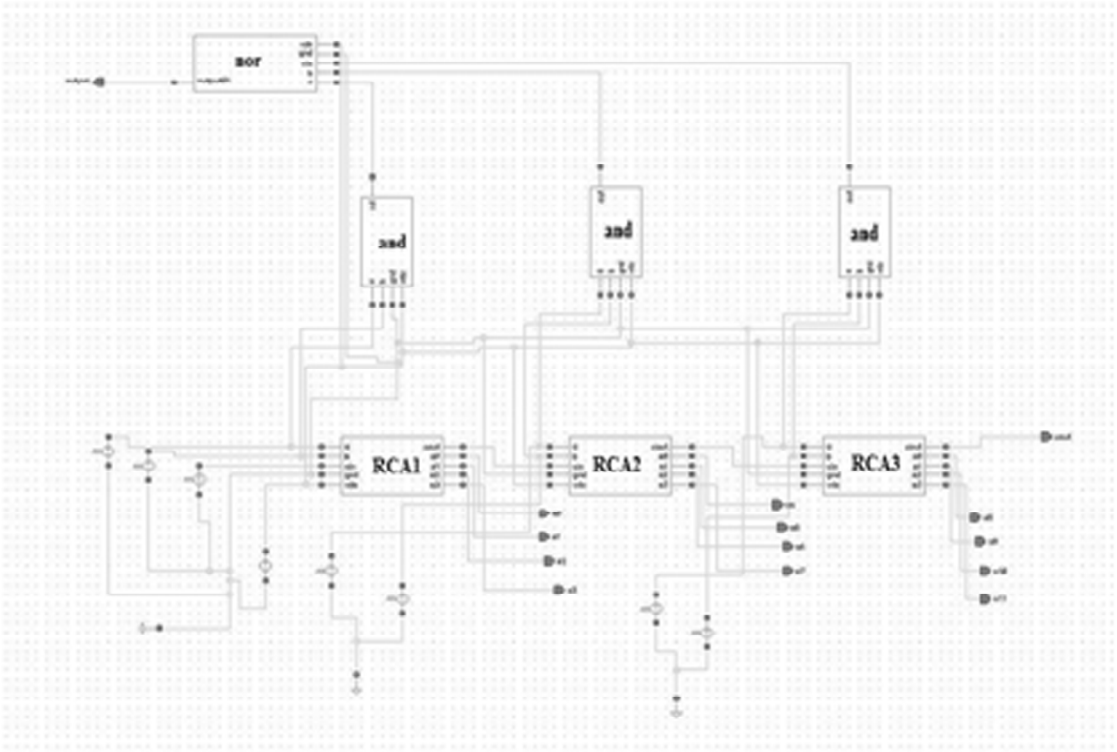

Figure 7: Schematic of DMADD (Dual mode addition)

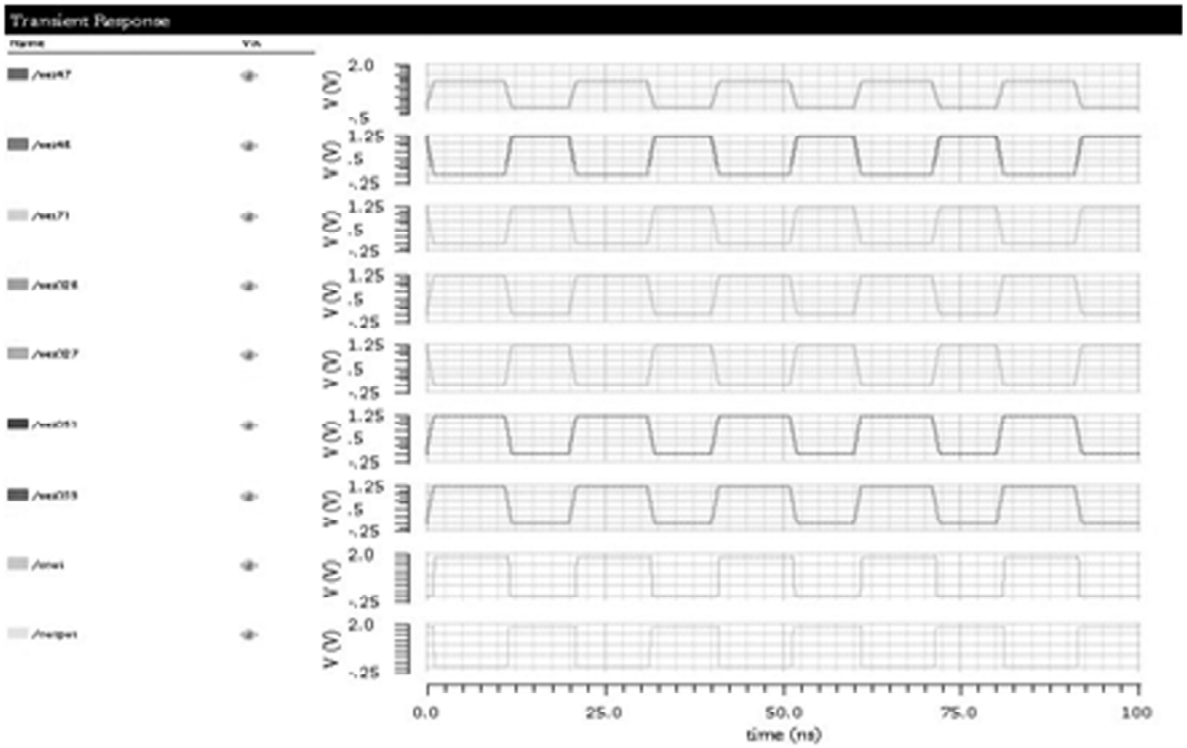

Figure 8: Transient response of DMADD

DML empower on-the-fly switching in clock cycle resolution between the high performance energy efficient static and dynamic operation modes. This instantaneous switching is obtained by a unique circuit topology complemented by apt transistor sizing. Although the topology of a DML gate is similar to a static logic family gate, which consists of an additional transistor. DML gates have a very normal structure; however, they require an unconventional sizing scheme to achieve the target behaviour.

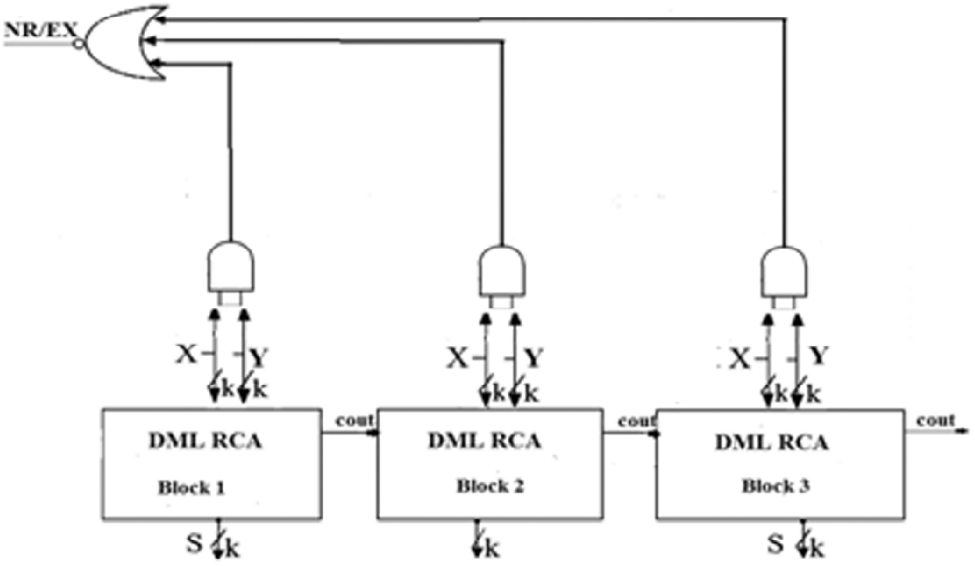

Figure 9: DM² ADDER

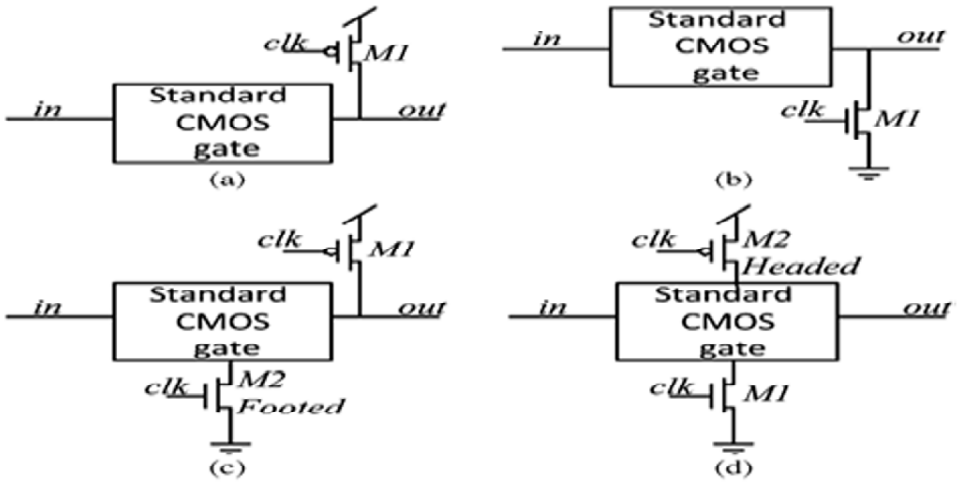

Figure 10: (a) TYPE_A DML topology (b) TYPE--_B DML topology (c) Footed TYPE_A DML gate (d) Headed TYPE_B DML gate.

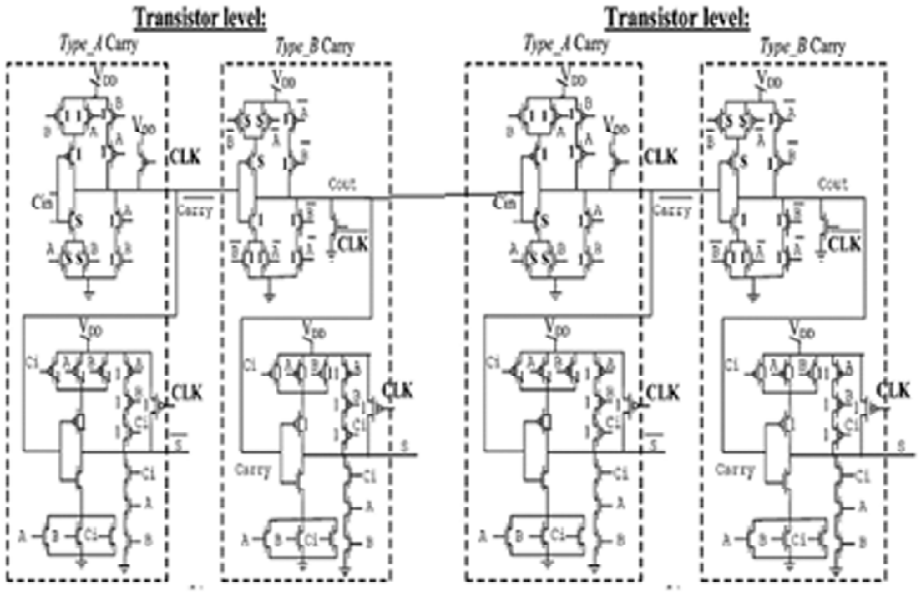

Figure 11: RCA with dml Transistor

In the static DML operation mode, M1 transistor is cut off by applying the high clk signal for "Type A" and for "Type B", applies low clk_bar and this helps all these gates operate similarly to static CMOS logic.

For the dynamic operation mode, the clk switches, providing two different phases named pre-charge and evaluation phases. In the pre-charge phase, in Type A gate, the output is charged to VDD and in type B gate discharged to GND. whereas in the evaluation phase, the output is evaluated according to the values of the gate inputs.

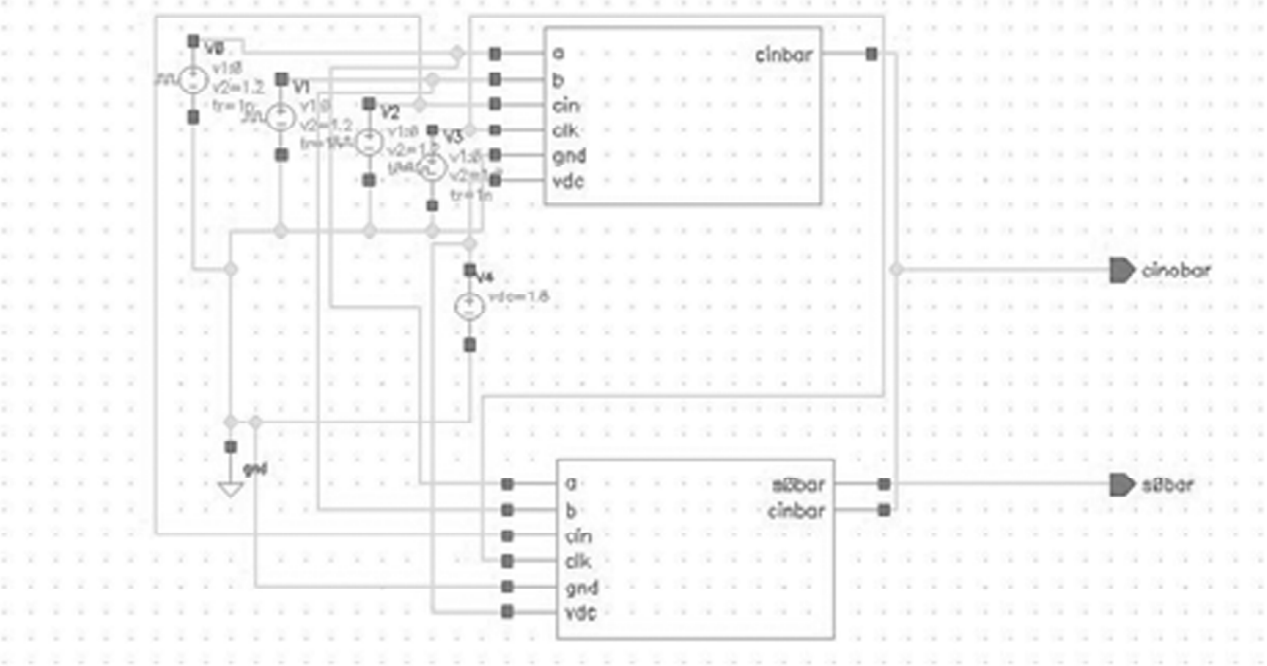

Figure 12: Schematic of full adder in DM² adder

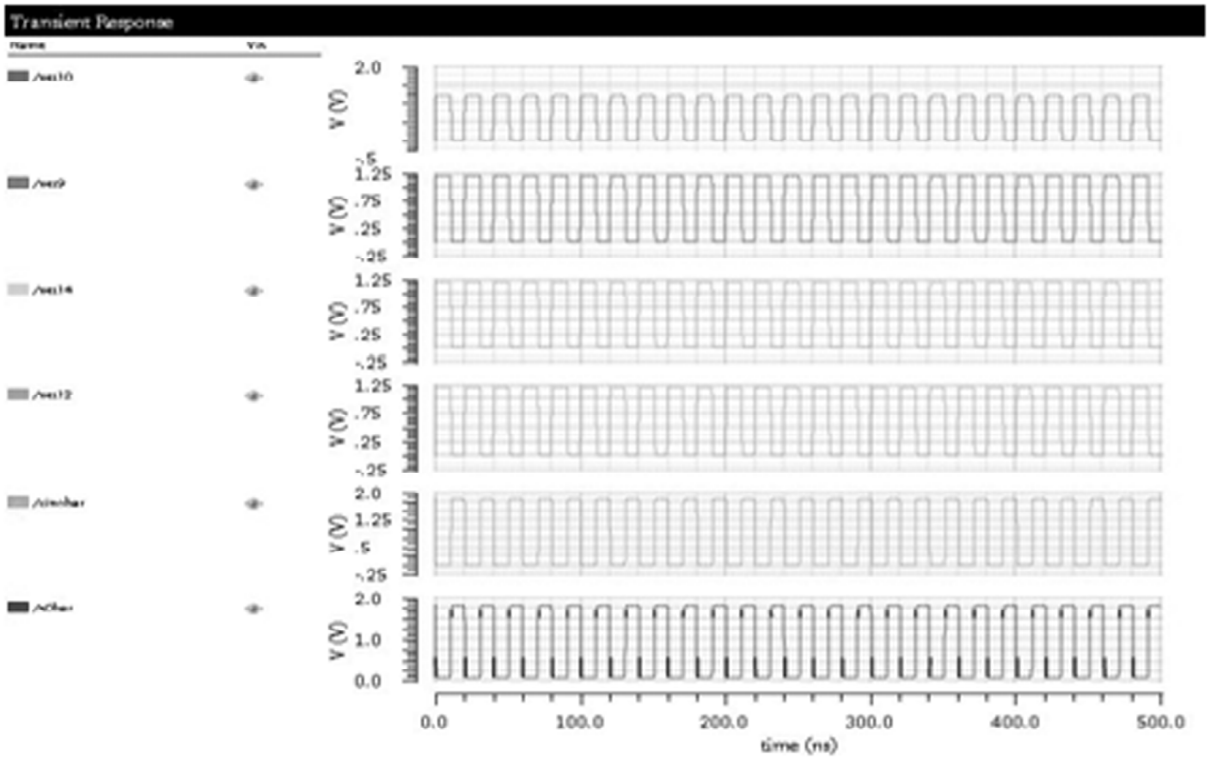

Figure 13: Transient response of full adder

Using four full adders with alternative polarity, RCA is designed.In full adders alternative polarity is used to reduce the delay in ripple carry adder. By using inverting technique in full adders, we can make rca works fast twice as possible

In this DM² adder, we used three ripple carry adders in which dual mode logic is inserted.By using this, the result of cout is 0 which makes adder to complete addition in one cycle and reducing power. If extra cycles are used for addition, it takes extra power to complete the required operation

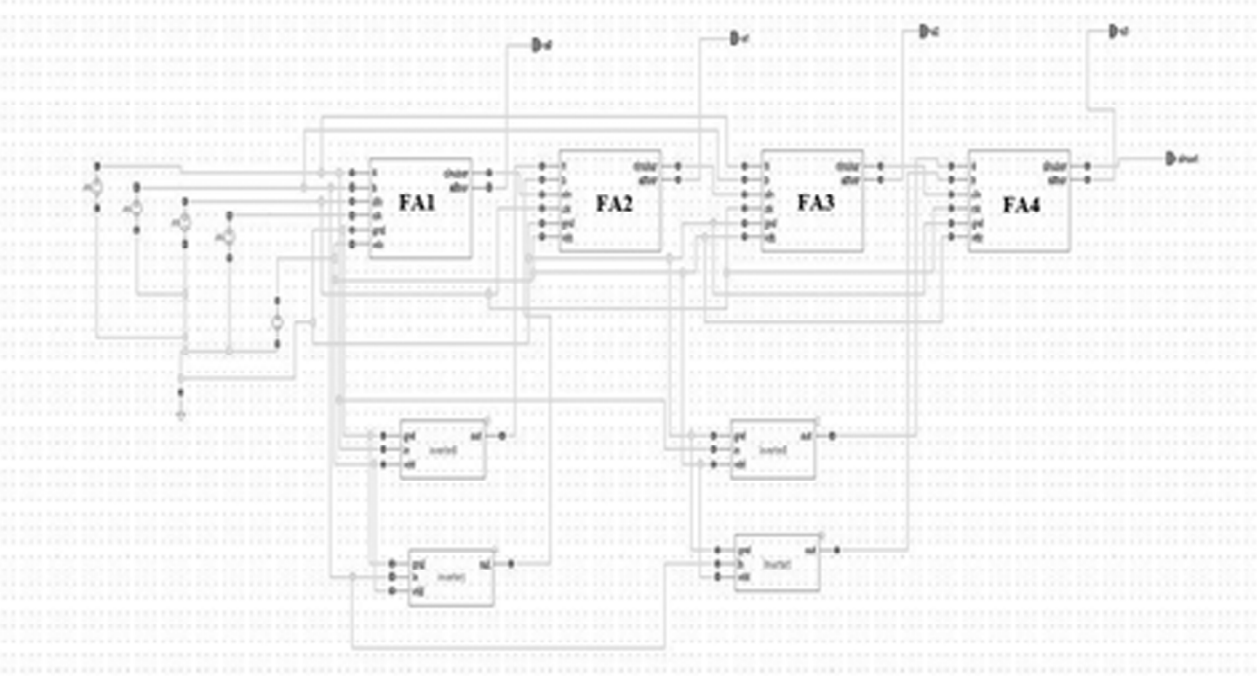

Figure 14: Schematic of Ripple carry adder

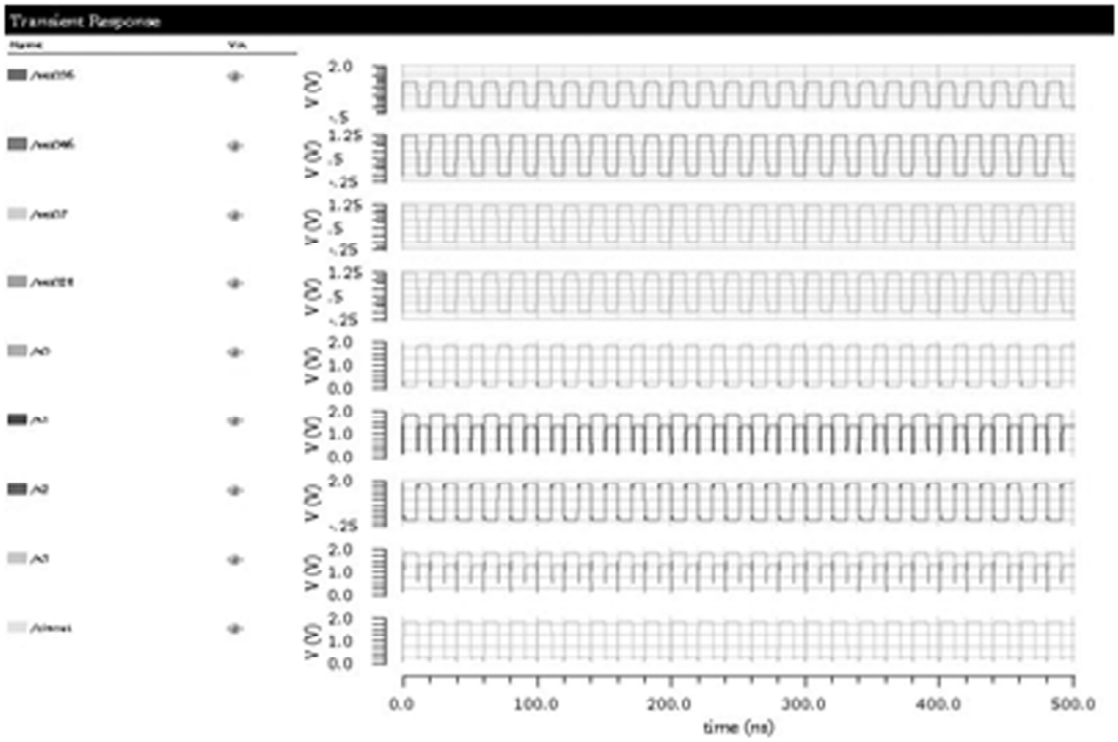

Figure 15: Transient response of ripple carry adder

DMADD can benefit from DML by fast switching between DML static and dynamic modes, depending on whether the DMADD needs to operate in the normal or extended mode. In both cases a single clock cycle suffices, making the dual mode useful for out-of-order architecture without any penalty in clock cycles of pipeline stall. As mentioned, DML utilization also yields considerable energy reduction. This follows from the lower energy of its static mode compared to CMOS, operated with very high probability. This mode only rarely occurs even though its dynamic mode energy is higher than CMOS.

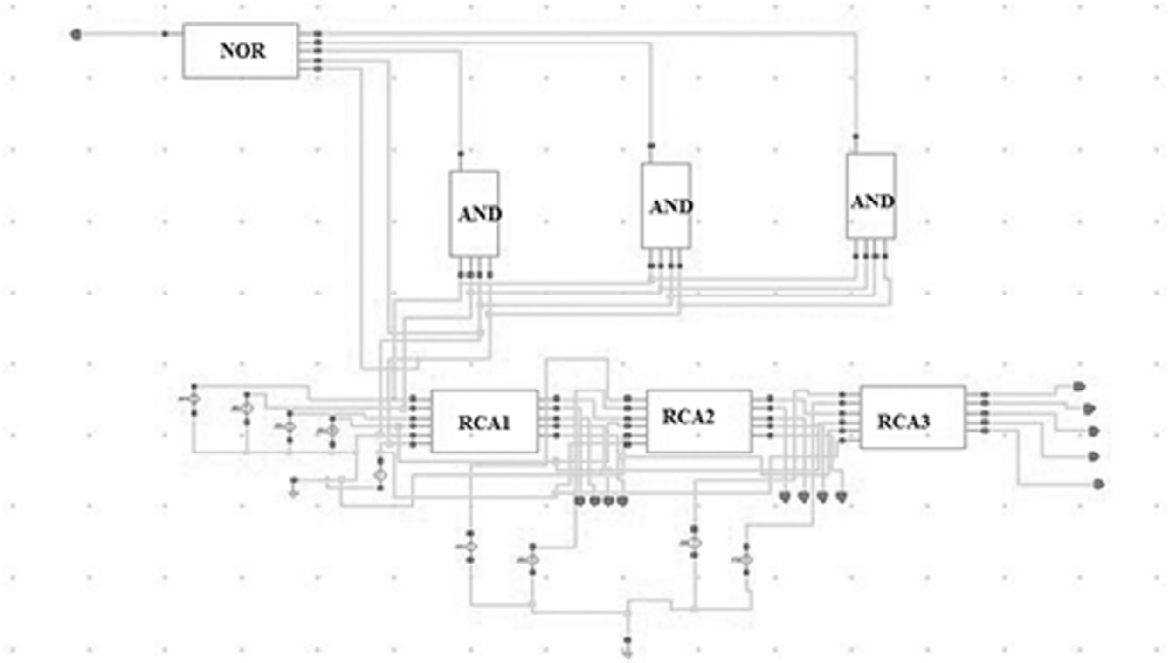

Figure 16: Schematic of DM² adder

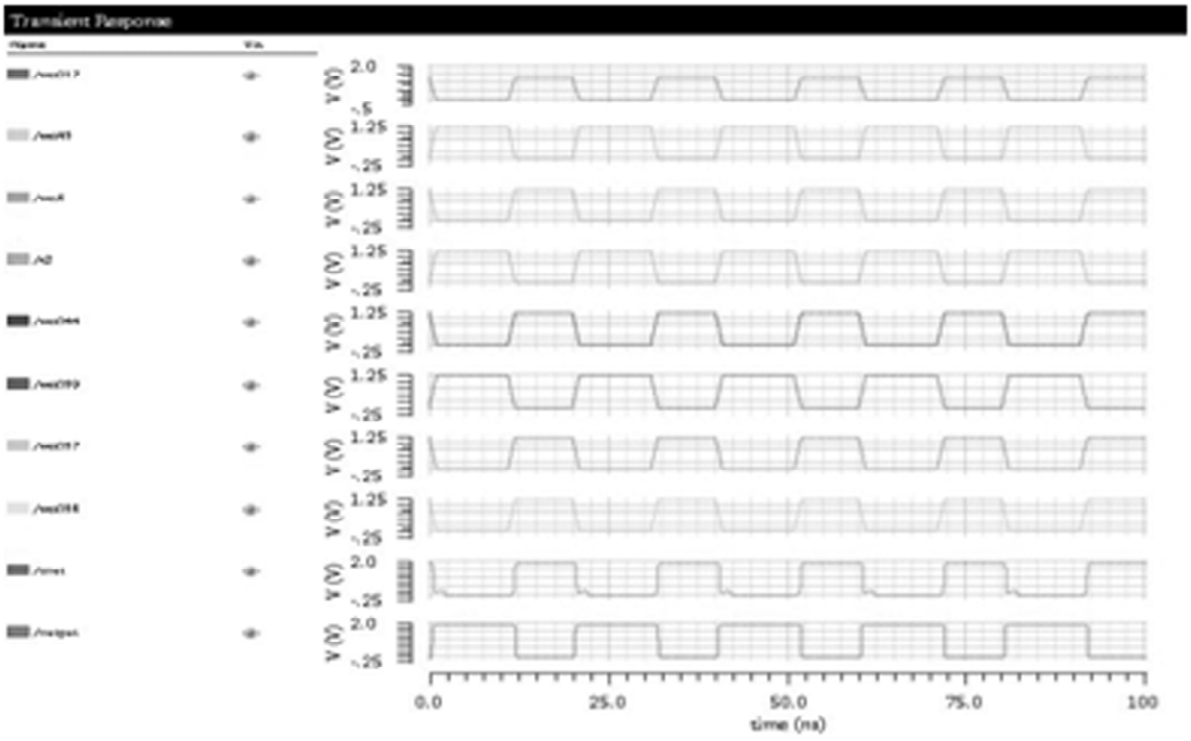

Figure 17: Transient response of DM² adder

Table 1
Power, Energy and Delay comparisons of DMADD and DM² adder

	DMADD			*DM²*		
	FA	*RCA*	*DMADD*	*FA*	*RCA*	*DM² ADDER*
POWER (μw)	116.2	293.7	1068.1	77.57	271.0	850.9
Delay (pSec)	649.2	671.8	1086	593.9	627.2	831.1
Energy(mJ)	0.8640	2.18	6.3	0.576	2.01	1.59

4. CONCLUSION

A novel low-energy and high-performance DM² adder combining DML logic and dual-mode addition was described. It simplifies the usage of dual-mode addition in a pipelined processor. The combination of novel circuit topologies and probability-based computational circuit architecture can fulfil considerably greater energy than traditional designs. Future work includes research of whether DM² can be operated with multipliers, which will first require determining whether multipliers have small carry probabilities.

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