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Voltage Balancing of Five Level Diode Clamped Multilevel Inverter Using Five Level Boost Converter

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ABSTRACT

The multilevel inverters have drawn tremendous interest in power industry sector. Since the conventional two level voltage source inverters have some limitations in operating at high frequency due to switching losses, they are not much used in high power applications. Among the three configurations of multilevel inverter, Diode Clamped Multi Level Inverter (DCMLI) has the simple design and offers high efficiency at fundamental switching frequency. But it suffers the problem of dc link capacitor voltage unbalance which makes it not suitable for many applications. This paper proposes a new method to solve the balancing problem of the DCMLI using a Five Level Boost Converter. By varying the duty cycles of the switches in the boost converter, a constant voltage across all the capacitors can be maintained.

Keywords: multilevel inverter, voltage unbalance, five level boost converter

1. INTRODUCTION

Multilevel inverters (MLI) have become more popular over the years in high power electrical applications without use of a transformer and with promise of less disturbance and reduced harmonic distortion. The general structure of the multilevel inverter is to synthesize a sinusoidal voltage from several levels of voltages, typically obtained from capacitor voltage sources. The applications include static VAR compensators, high voltage grid interconnections, variable speed motor drives etc. The input dc voltage of the multilevel inverters can now be replaced by photovoltaic cells. There are mainly three types of multilevel inverters; Diode Clamped MLI (DCMLI), Flying Capacitor MLI and Cascaded MLI. The DCMLI has many advantages compared to other configurations such as high efficiency for the fundamental switching frequency, the capacitors can be pre-charged together at the desired voltage level and the capacitance requirement of the inverter is minimized due to all phases sharing a common dc link [1]. Even though DCMLI has these many advantages, it is not so commonly used because of its one major disadvantage; voltage unbalance of the dc link capacitors.

For the DCMLI with more, if the modulation index is increased more than a limited value, the center capacitors gradually discharge and finally the inverter output converges at three levels [2], [3]. To eliminate the problem of dc-link capacitor voltage unbalance in the five level diode clamped inverter, the following methods were used: Space vector modulation, coupled inductors, feedback control [4]. But these methods have limitations that include low range of operation, harmonic distortion, leakage current problem etc [5].

This paper proposes a new method to solve the voltage unbalance problem of dc link capacitors by using a five level boost converter. The boost converter charges and discharges the capacitors by turning on and off the four switches. A separate control circuit is used to varying the duty ratios of the switches [6].

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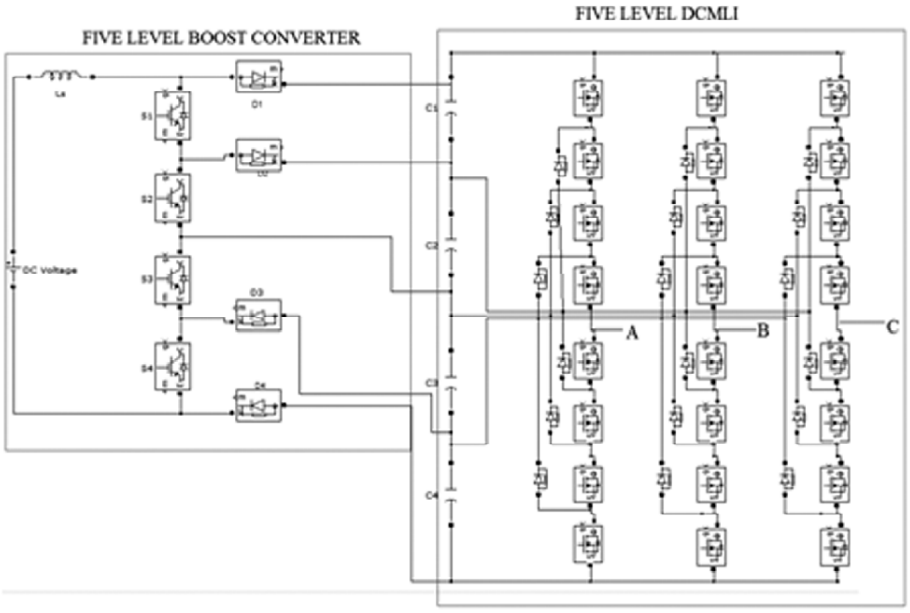

Figure 1: Circuit diagram of the proposed system

The multilevel inverter uses sinusoidal pulse width modulation technique to generate gate pulses for the inverter. The circuit diagram of the proposed method is shown in Fig.1.

2. FIVE LEVEL BOOST CONVERTER

A multilevel boost converter is a very attractive topology in high power applications. The main advantage of the multilevel boost converter is it can achieve high gain without increasing the duty cycle. Fig. 1 illustrates the five level boost converter which combines the boost converter and the switched capacitor function to provide an output of several capacitors in series with the same voltage and self-balanced voltage. The major advantages of this topology are: (i) its input current is continuous (ii) it has a very large conversion ratio with low duty cycle and without a transformer, its gain is approximately five times compared to the conventional boost converter [7] . Its output voltage can be increased to any value by increasing the number of levels. It can be built in a modular way and more levels can be added without changing the main circuit.

A five level boost converter can be operated in two ways; Continuous Conduction Mode (CCM) and Vertical Inter Leaved (VIL) mode. The 5-level DC-DC boost converter can be modulated by turning on and

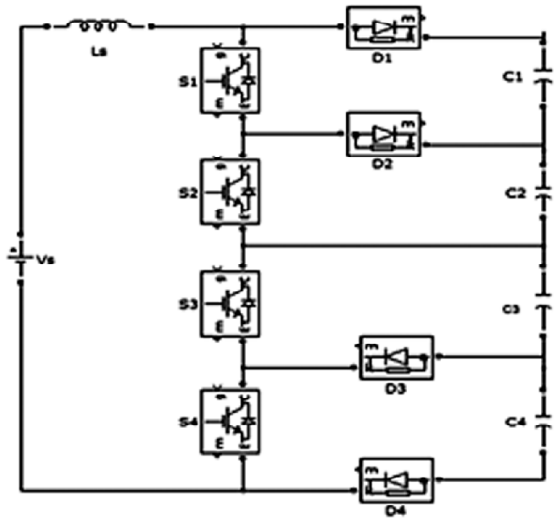

Figure 2: Five level boost converter

off all four main switches during one period of the input current [10]. There are five modes of operation in five level boost converter as illustrated in Fig. 1(a), 1(b), 1(c), 1(d) and 1(e). The current flow in each mode is represented in thick lines.

In mode 1, all the four switches S_1, S_2, S_3 and S_4 are on and the current flows through the inductor, switches and then returns to the input.

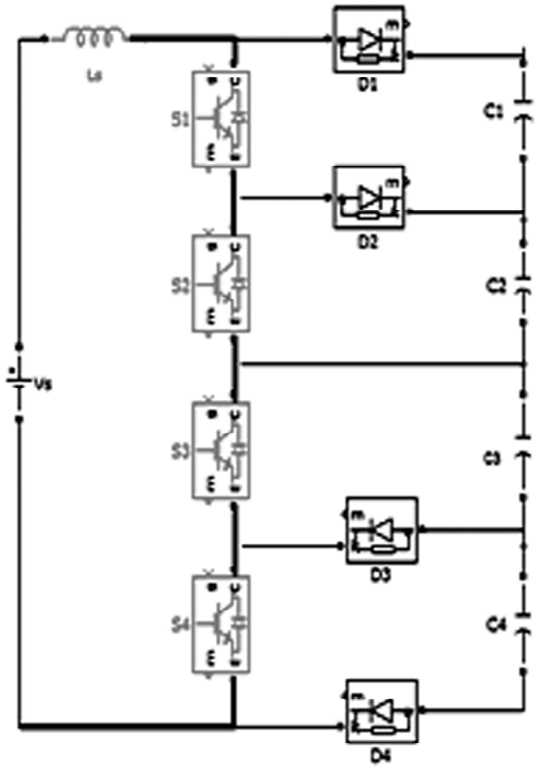

Figure 2 (a): Mode 1

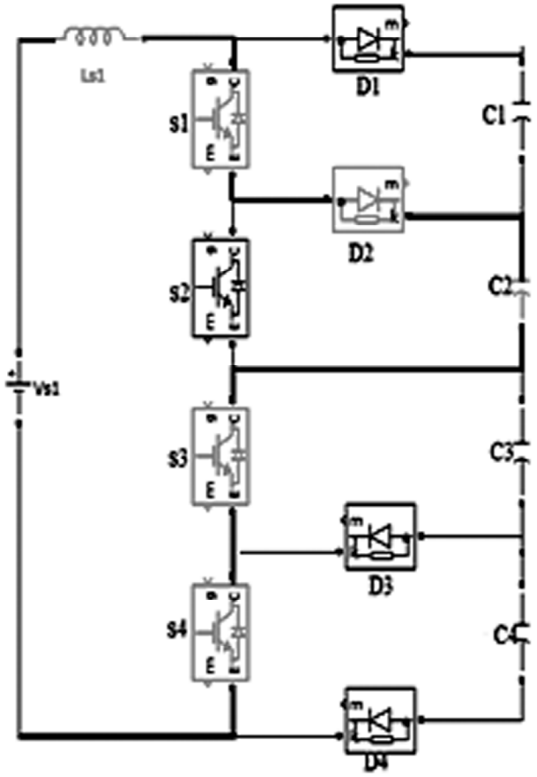

Figure 2 (b): Mode 2

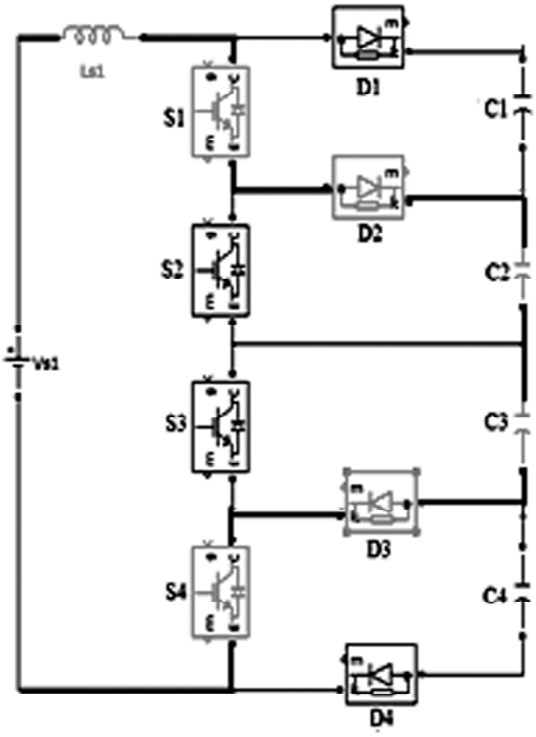

Figure 2 (c): Mode 3

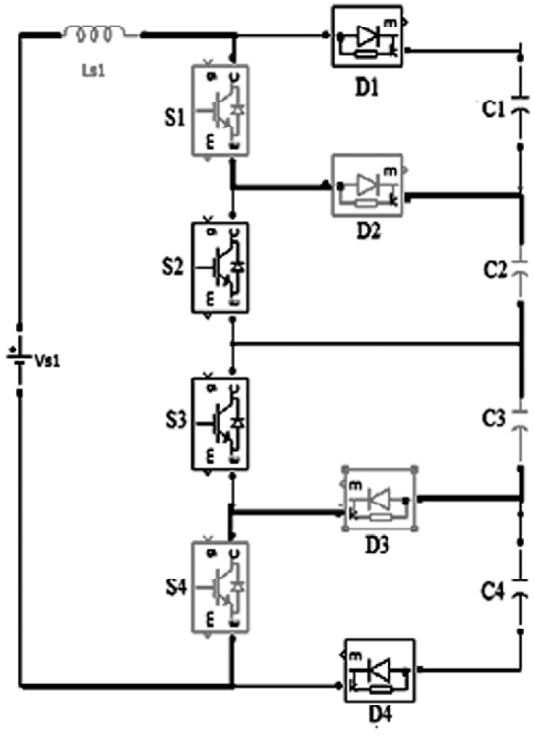

Figure 2 (d): Mode 4

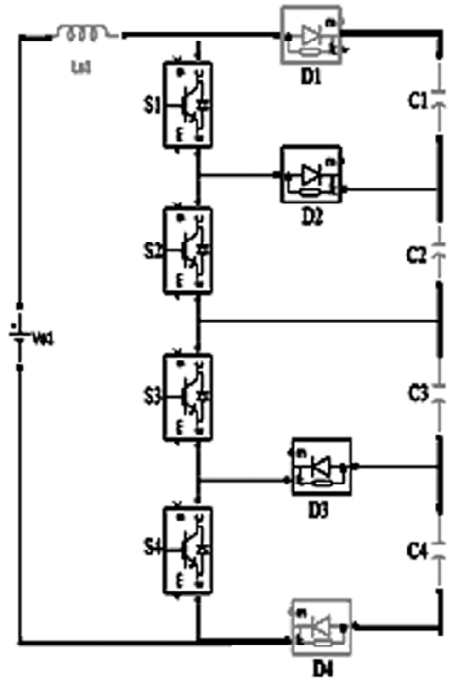

Figure 2 (e): Mode 5

In mode 2, switches S_1, S_3 and S_4 are turned on and the capacitor C_2 is charged. The current flows through the path inductor L_S, switch S_1, D_2, C_2, S_3, S_4 and then to the input. In mode 3, the switches S_1 and S_4 are turned on and the capacitors C_2 and C_3 are charged. Mode 4 begins when the switch S_4 alone turns on thereby charging the capacitors C_1, C_2 and C_3. In mode 5 no switches are turned on and all the capacitors are charged simultaneously.

The control diagram used for the five level boost converter is shown in Fig. 3. The gate signals for the five level boost converter are generated by a separate control circuit that consists of a comparator and PID controller. The capacitor voltages are measured and compared with the reference voltage and the error

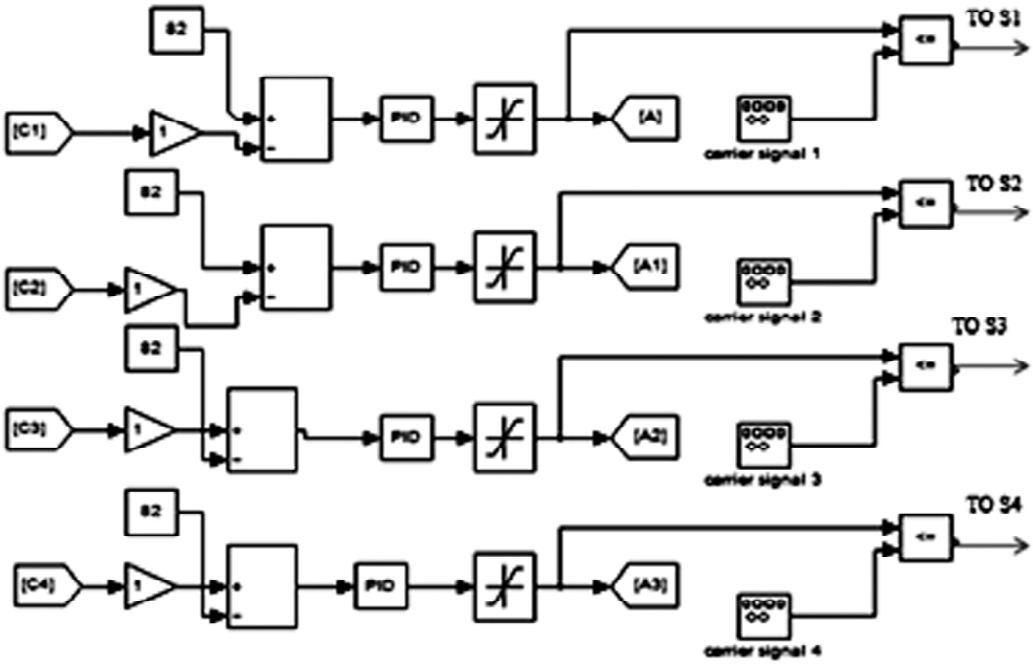

Figure 3: Control circuit for five level boost converter

signal is given to the PID controller [8]. The output is given to a comparator that compares it with a carrier signal of fixed frequency.

The voltage equation of a five level boost converter is given by (1) as follows:

$$V_0 = \frac{N}{(1-D)} * V_s \tag{1}$$

$$= \frac{5}{(1-0.5)} * 20 \tag{2}$$

$$= 120 \tag{3}$$

3. FIVE LEVEL DIODE CLAMPED MLI

The general structure of the multilevel inverter is to synthesize a sinusoidal voltage from several levels of voltages typically obtained from capacitor voltage sources. The "multilevel" starts from three levels. A five level diode clamped multilevel inverter has the following [9]:

$$\text{No. of switches: } 2(m-1) = 2(5-1) = 8 \tag{4}$$

$$\text{No. of capacitors: } (m-1) = (5-1) = 4 \tag{5}$$

$$\text{No. of diodes: } (m-1)\,(m-2) = (5-1)\,(5-2) = 12 \tag{6}$$

The structure of five level DCMLI is given in Fig. 4. The general structure of the multilevel converter which has multiples of the usual six switches found in a three-phase inverter is to synthesize a sinusoidal voltage from several levels of voltages, typically obtained from capacitor voltage sources.

The main motivation for such converters is that current is shared among these multiple switches, allowing a higher converter power rating than the VA rating of the individual switch which would otherwise allow with low harmonics. As the number of levels increases, the synthesized output waveform, a staircase like wave, approaches a desired waveform with decreasing harmonic distortion [10]. The gate pulses for the MLI is generated using sinusoidal pulse width modulation (SPWM) technique. The control circuit for the

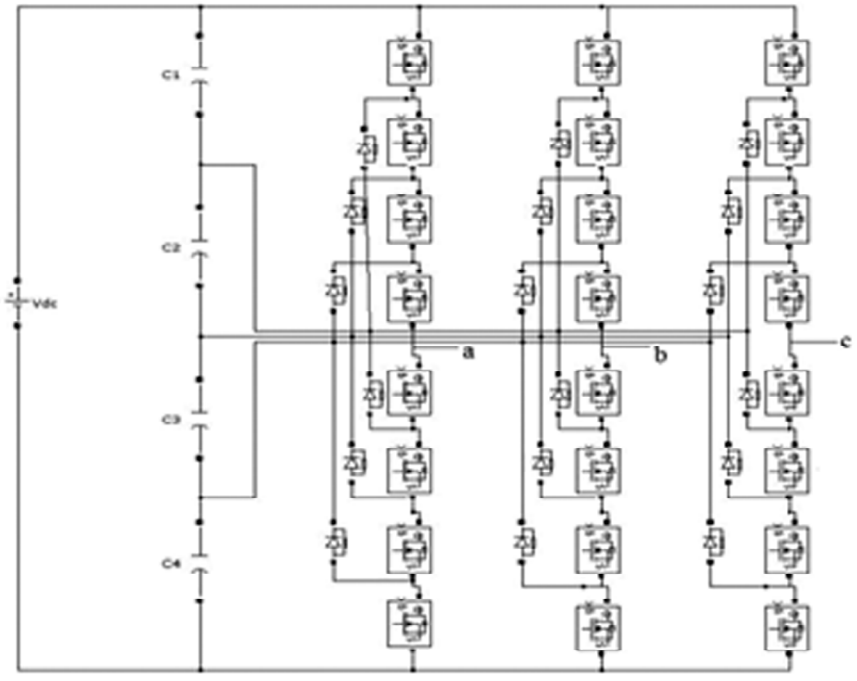

Figure 4: Five level diode clamped MLI

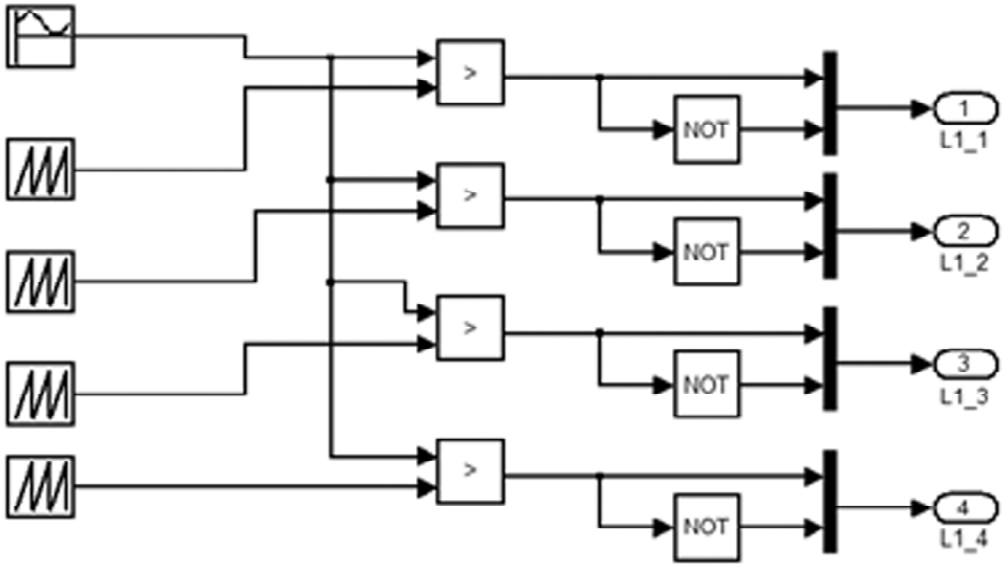

Figure 5: Simulink model of sinusoidal pulse width modulation

SPWM is shown in Fig. 5. In SPWM technique, the width of each pulse is varied in proportion to the amplitude of a sine wave evaluated at the centre of the same pulse. The gating signals are generated by comparing a sinusoidal reference signal with a triangular carrier wave of frequency f_c. The frequency of the carrier wave is selected as 2 kHz.

4. SIMULATION ANALYSIS

The proposed configuration has been simulated using MATLAB/Simulink software for different load conditions. The overall simulation diagram is shown in Fig. 6. The dc link capacitor voltages, line voltages and phase voltages with R load and RL load are captured and analyzed. The analysis is done separately and detailed in the following sections. Section A includes the analysis with R load and in Section B analysis with RL load is done. It is observed from these analyses that for R load and RL load, the output line voltages and phase voltages remain constant at 200 V. That is the circuit can be used in various load power

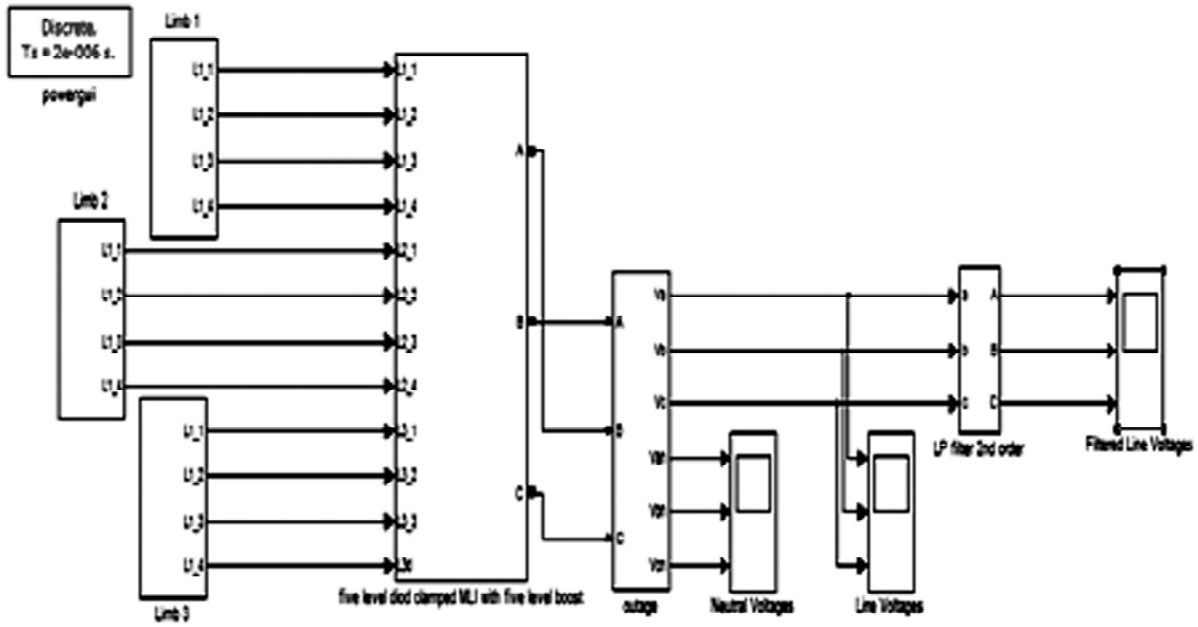

Figure 6: Simulation model of the proposed system

factor conditions for a constant output voltage. Fig.10 shows the balanced dc link capacitor voltages. FFT analysis is done and the results are depicted in Fig. 13 and Fig. 14 respectively.

The values of inductor and capacitors of the five level boost converter are 12 mH and 2200 μF respectively. The switching frequency of the boost converter is selected as 5 kHz.

4.1. Simulation Analysis with R- Load

The simulation results with R - load (150 &!) are shown in the following figures. The results of boost converter output voltage, dc-link capacitor voltages and multilevel inverter output voltage and current are shown in fig. 8, fig. 9, fig. 10, fig. 11 and fig. 12 respectively. The boost converter input voltage is 20 V and input current measured is about 5 A. The boost converter output voltage is obtained as 200 V and output current is 22 A.

It is clear from Fig. 9 that all the four capacitor voltages are balanced to a voltage of around 50 V. The line to line rms output voltage of the inverter is measured as 200 V.

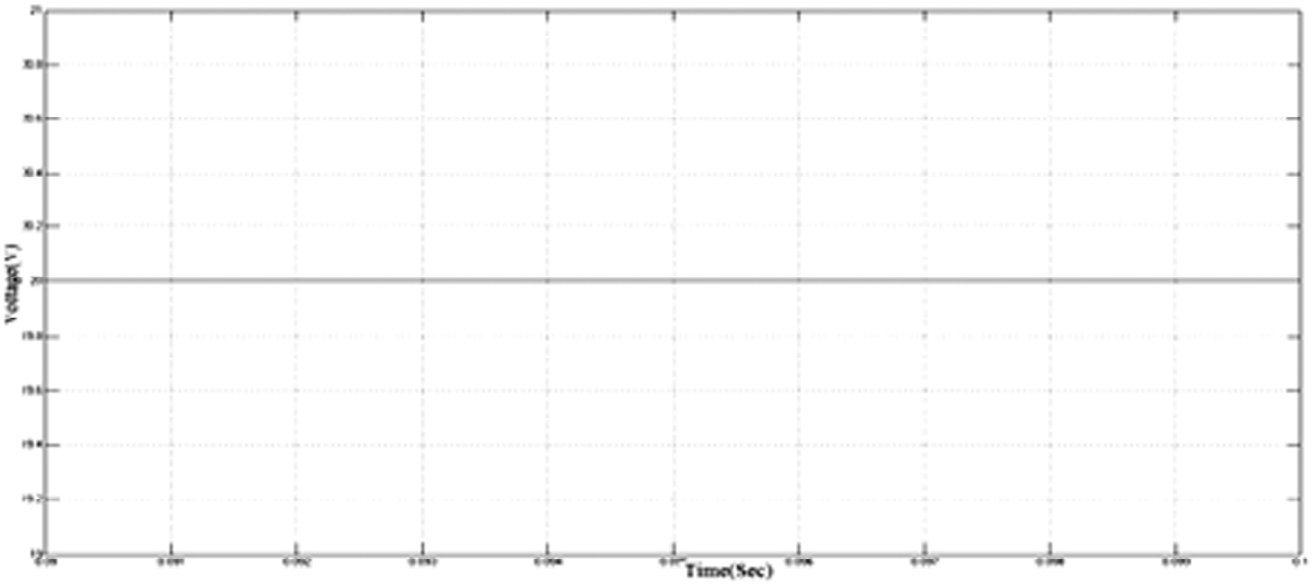

Figure 7: Boost converter input voltage

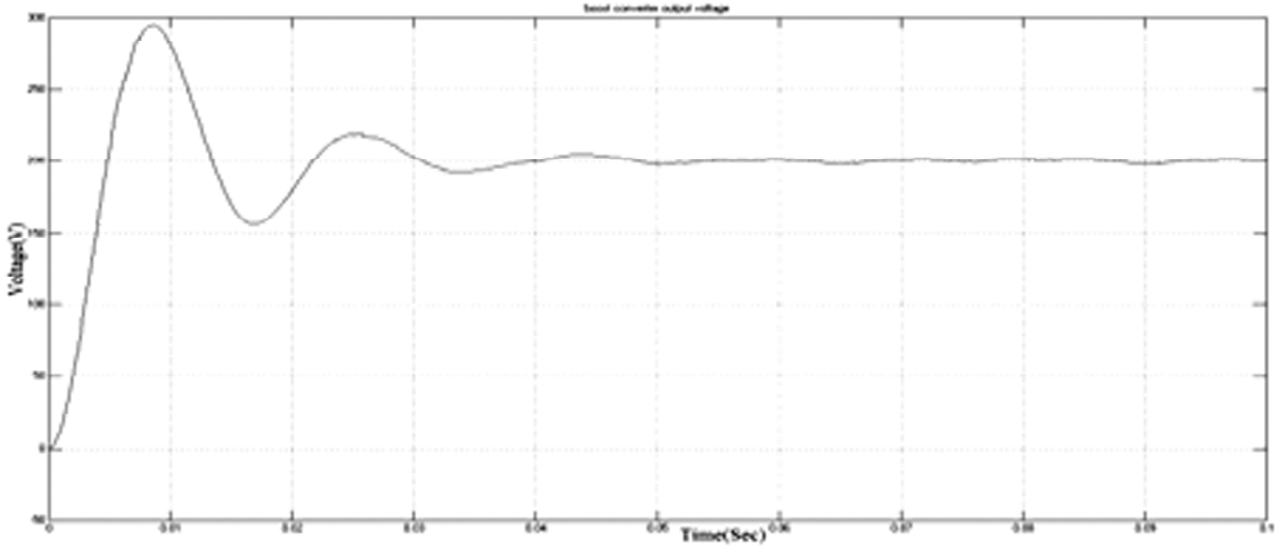

Figure 8: Boost converter output voltage

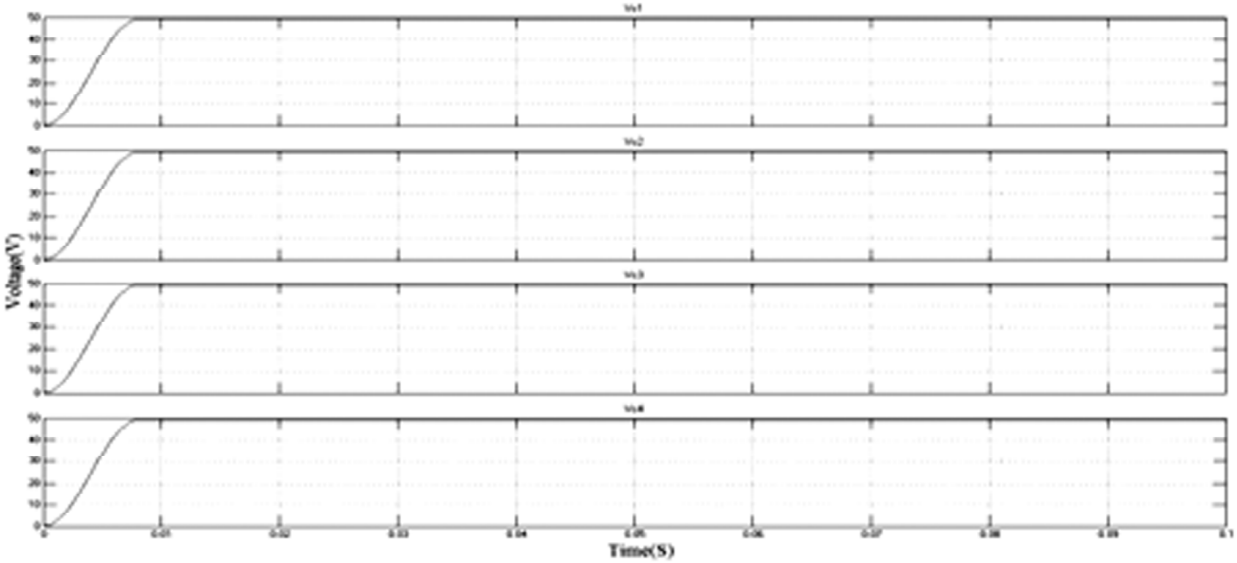

Figure 9: DC-link capacitor voltages

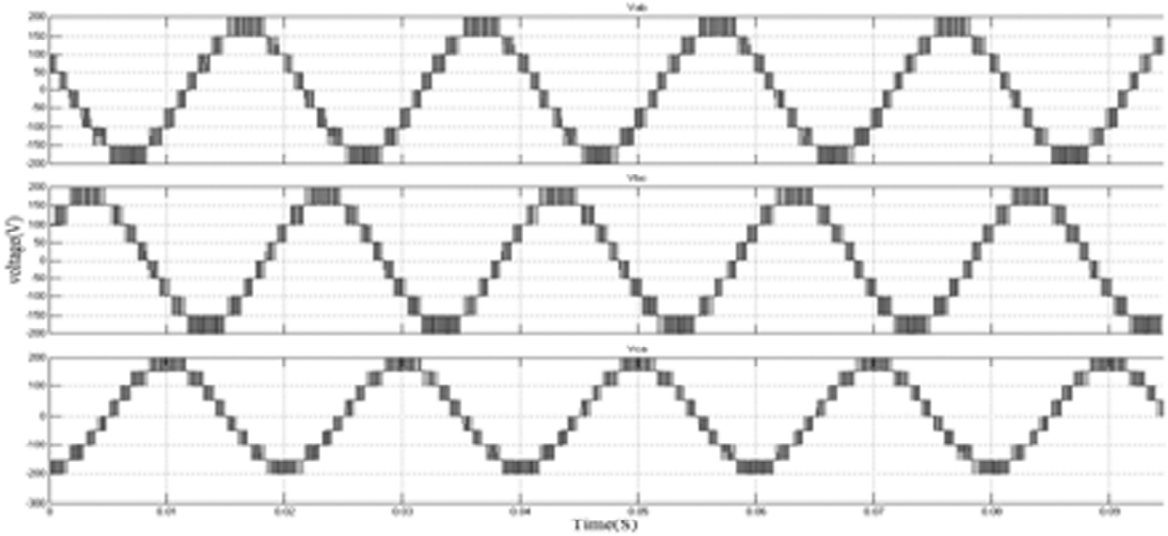

Figure 10: Multilevel inverter output line voltages

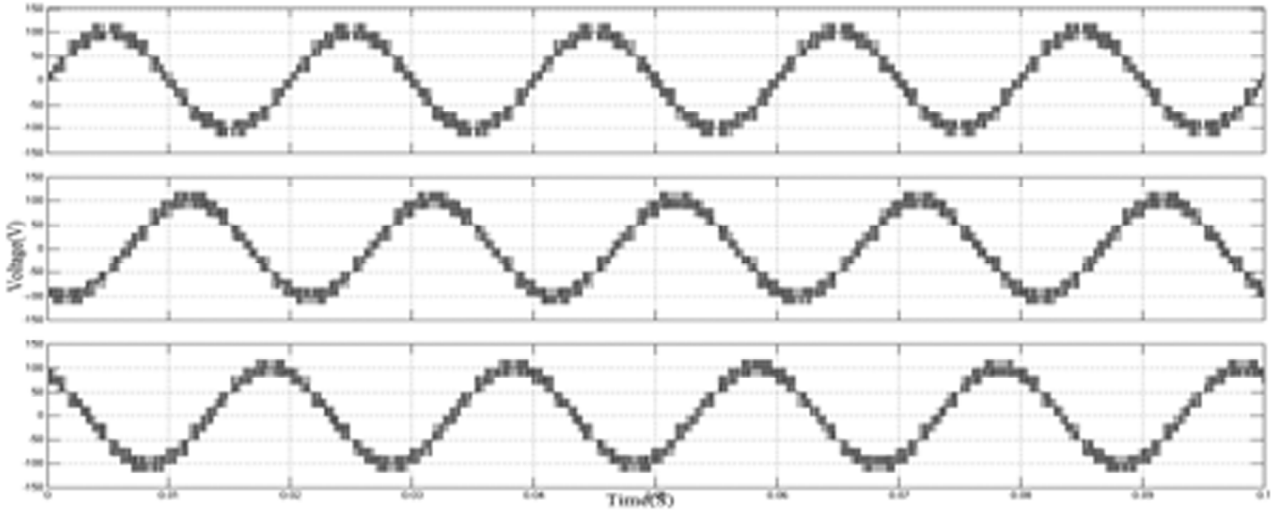

Figure 11: Multilevel inverter output phase voltages

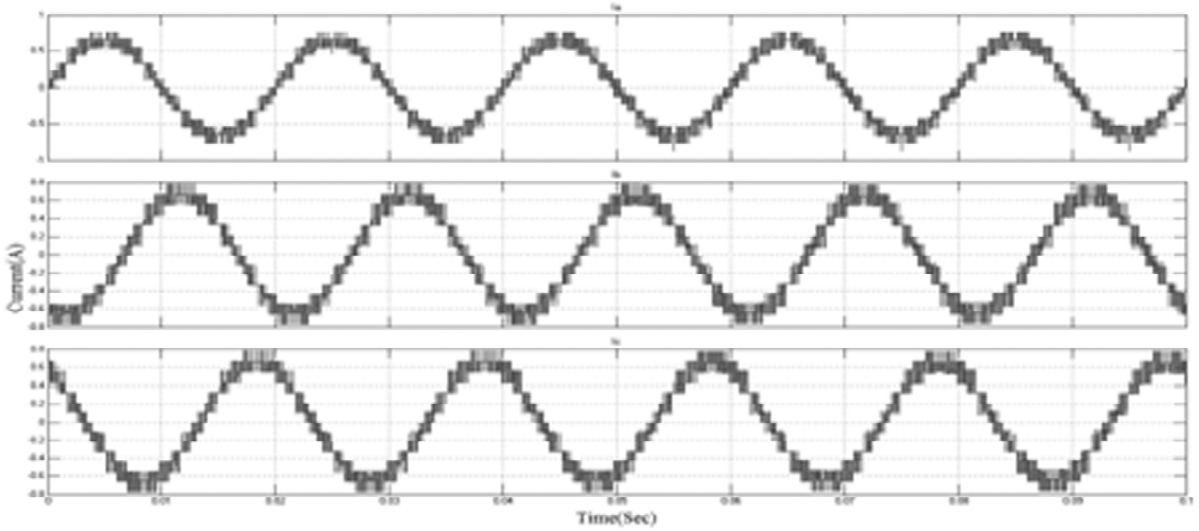

Figure 12: Multilevel inverter output current

4.2. Simulation results with RL load

The simulation results with RL load (R = 150 Ω and L = 28.7 mH) are shown in the following figures. Fig. 13 and Fig. 14 show the boost converter output voltage and dc link capacitor voltages. The dc link capacitor voltage is shown in Fig. 16 and it is clear from the figure that the capacitor voltages obtained with

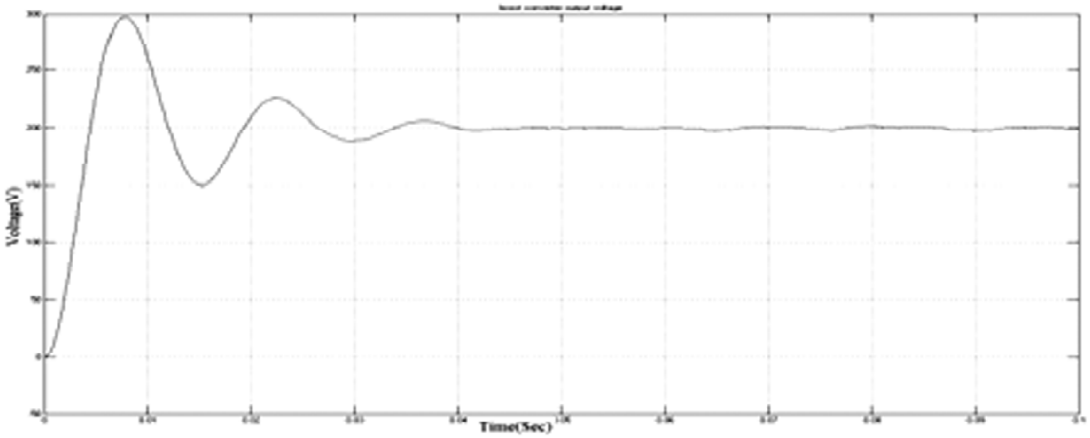

Figure 13: Boost converter output voltage

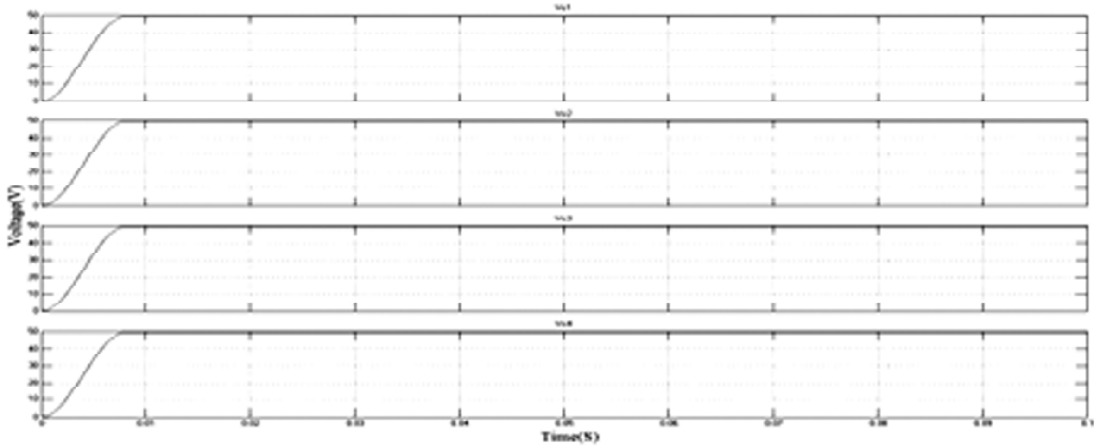

Figure 14: DC-link capacitor voltages

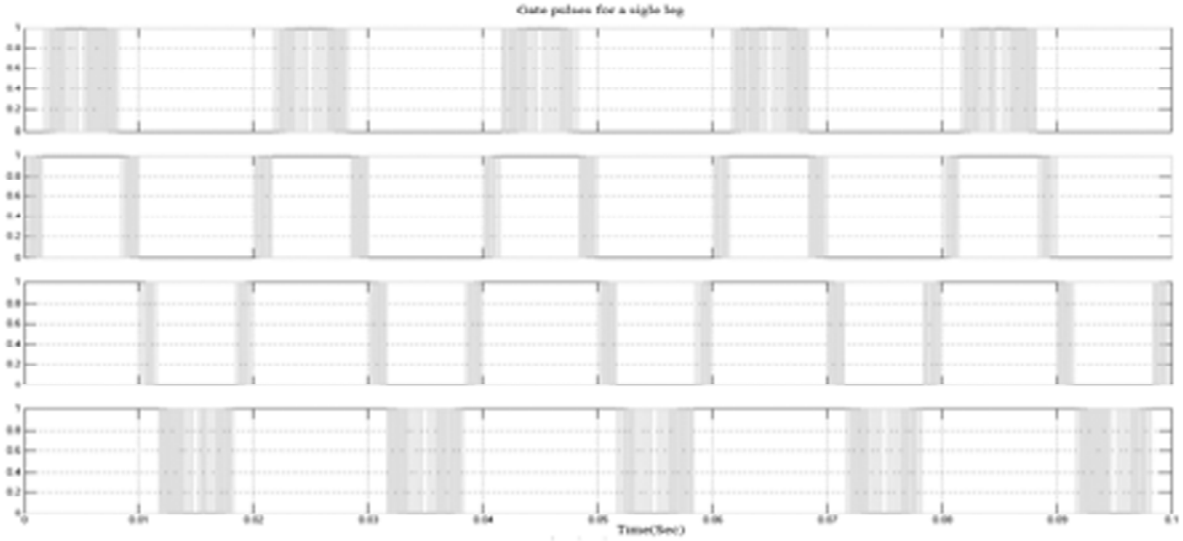

Figure 15: Gate pulses for multilevel inverter

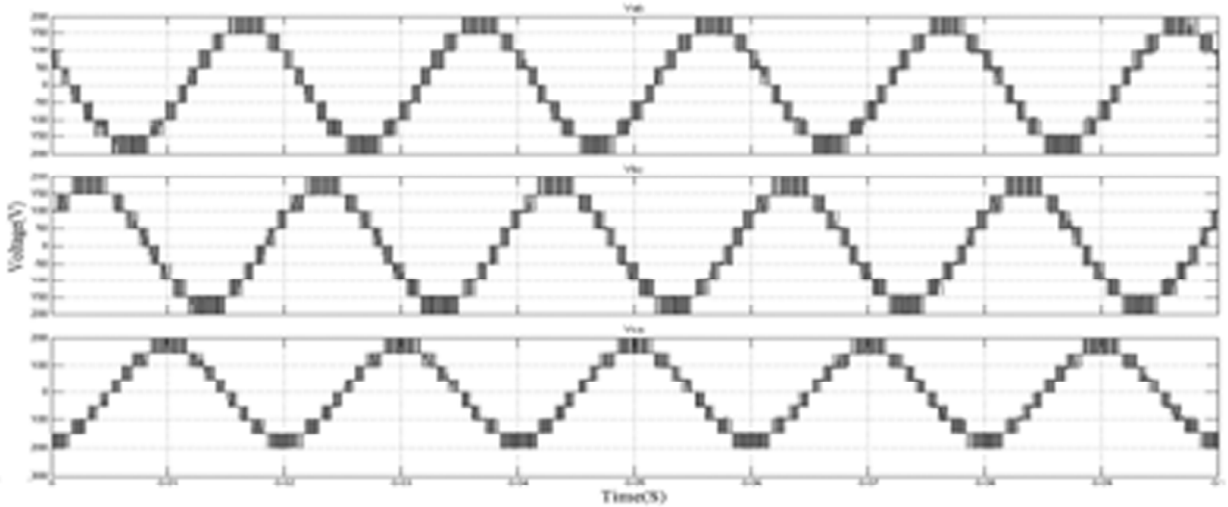

Figure 16: Multilevel inverter output line voltages

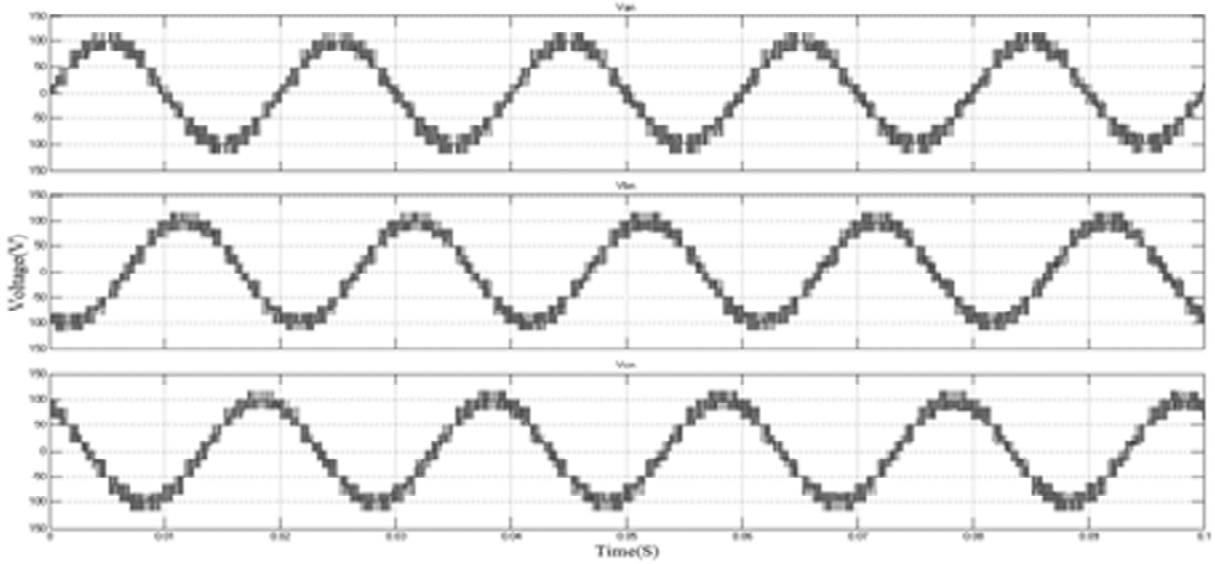

Figure 17: Multilevel inverter output phase voltages

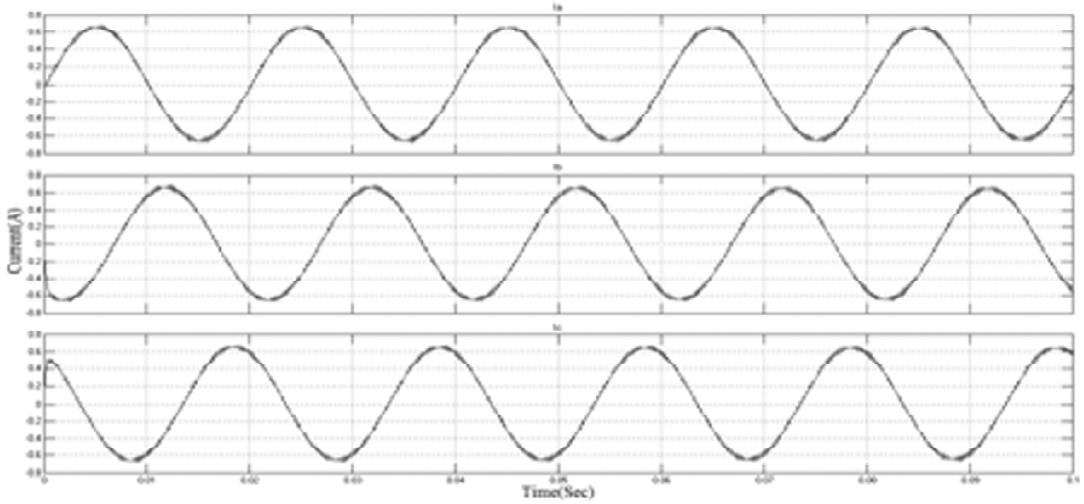

Figure 18: Multilevel inverter output current

R load and RL load are same. From Fig. 16 and Fig. 17, it is observed that the multilevel inverter output voltage is 200 V. Fig.15 shows the gate pulses for the multilevel inverter. The switching frequency of the carrier wave is taken as 2 kHz.

4.3. FFT Analysis

FFT analysis is done and the results are illustrated in the following figures. Fig. 19 to Fig. 21 show the FFT analysis for R load and Fig. 22 to Fig. 24 show the FFT analysis for RL load. From the analysis with R load the following results are obtained:

THD of phase voltage:	17.69%
THD of line voltage:	17.46%
THD of output current:	17.45%

From the analysis with RL load the following results are obtained:

THD of phase voltage:	17.45%
THD of line voltage:	17.71%
THD of output current:	3.06%

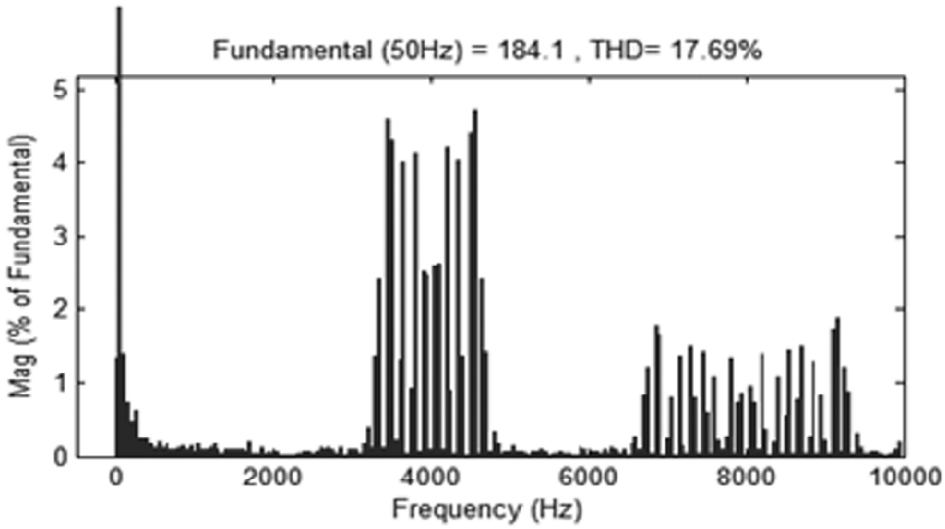

Figure 19: FFT analysis of phase voltage with R load

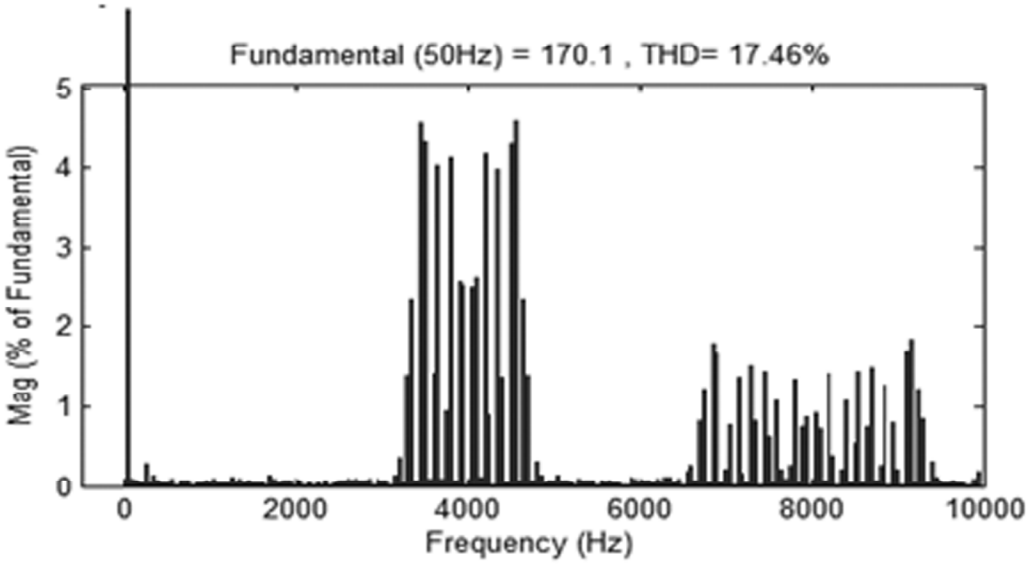

Figure 20: FFT analysis of line voltage with R load

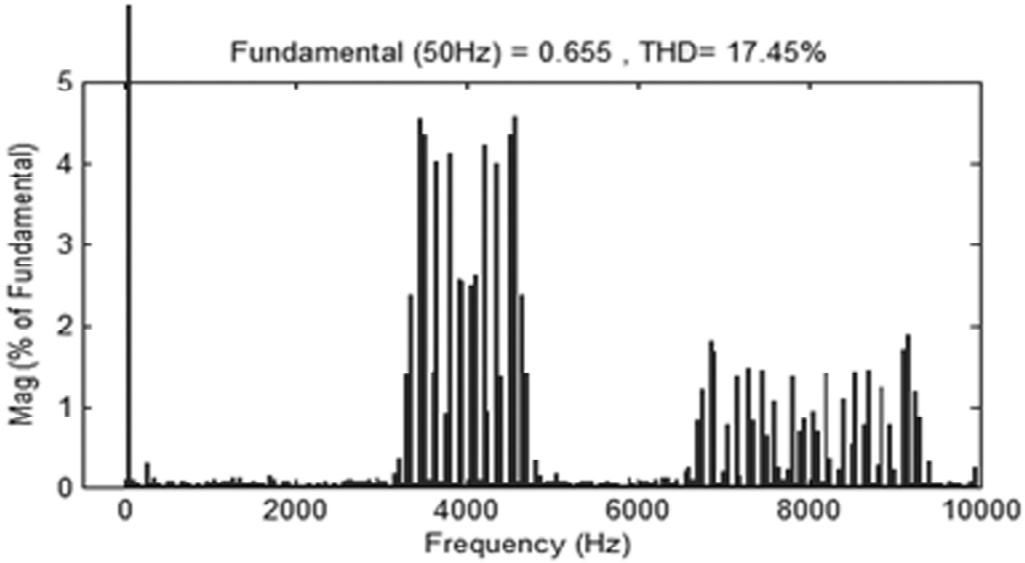

Figure 21: FFT analysis of output current with R load

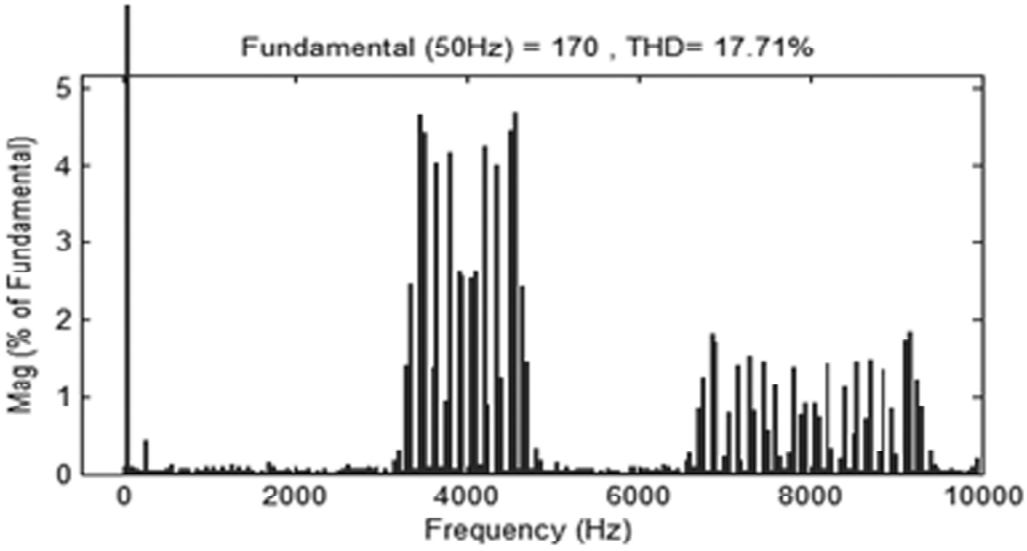

Figure 22: FFT analysis of phase voltage with RL load

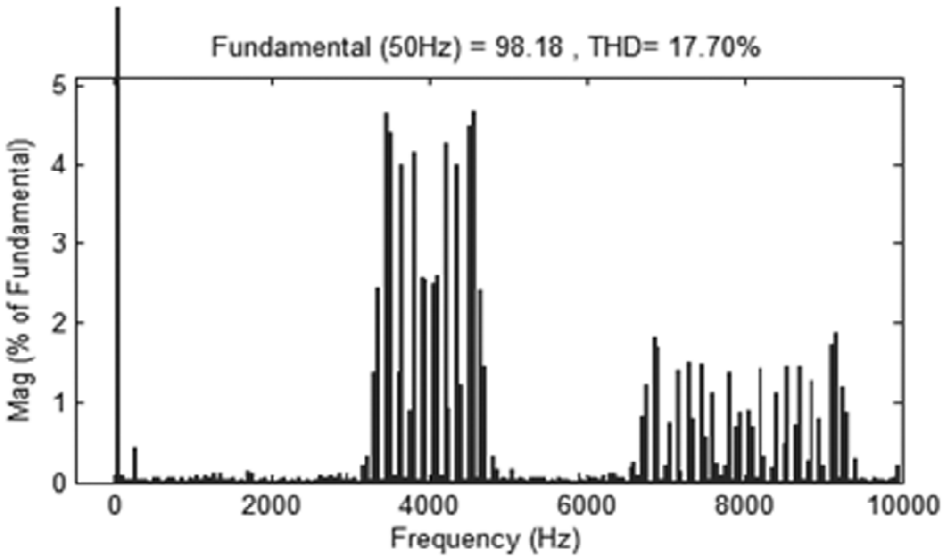

Figure 23: FFT analysis of line voltage with RL load

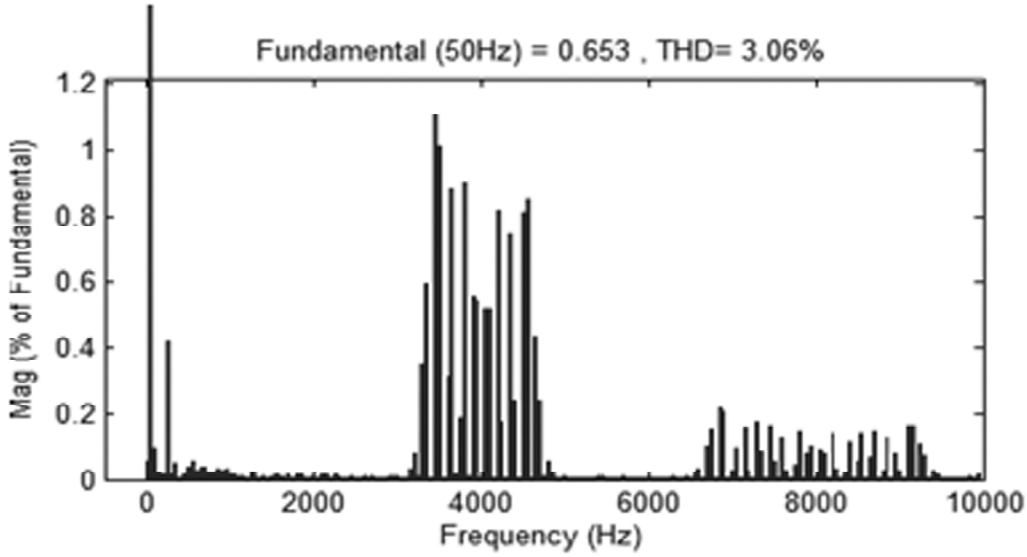

Figure 24: FFT analysis of output current with RL load

5. CONCLUSION

This paper has proposed a new method to solve the dc-link capacitor voltage unbalance of the five level diode clamped multilevel inverter. A five level boost converter is used for this purpose. A separate control circuit that consists of a controller and comparator adjusts the duty ratios of the switches which results equal voltages across the dc-link capacitors.

The results such as boost converter outputs (voltage, current, dc link capacitor voltages) and multilevel inverter outputs (phase voltage, line voltage, output current) are obtained for both R load and RL load respectively and analyzed in detail. From the analysis it is observed that for both R load and RL load the output voltage remains same. That is the proposed method is well suited for all power factor conditions. FFT analysis is done for both output voltage and current of the multilevel inverter and the results are verified.

This circuit can be effectively used in photovoltaic applications where high voltage and power is required. Also by varying the modulation technique for multilevel inverter, an analysis can be done by comparing the harmonics.

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