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Performance Analysis of Adaptive Neuro-Fuzzy Controller In Transient Modes of Positive Output KY Voltage Boosting Converter

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Abstract: The importance of the high voltage gain, non-isolated, voltage-boosting converters is unquestionable in recent days. Among the diversified variety of such converters Positive Output KY Voltage Boosting Converter (POKYVBC) has merits such as minimum ripple content in output voltage (in order of few mV), haste dynamic behavior and settling time, and larger voltage conversion ratio while operating in continuous conduction mode (CCM). The challenging part of a power converter system is designing feedback controller to control in steady state and transient state. The paper ascertains a formulaic procedure for designing an adaptive controller for Positive Output KY Voltage Boosting Converter (POKYVBC) system. The proportional-integral controller (PIC) is tuned (the controller coefficients are computed) at different load conditions. This fiend data is involved in training the adaptive neuro-fuzzy inference system (ANFIS) that delivers a robust controller at the dynamics of the POKYVBC in different loading condition. The ANFIS controller is performance validated for the complete range of operating conditions. The MATLAB-Simulink simulation study and the SPARTAN-6 FPGA (XC6SLX45) device based experimental corroboration verify the performance of the ANFIS controller for 28V (output) POKYVBC and compares with PIC.

Key words: Positive output KY voltage boosting converter, adaptive neuro-fuzzy inference systems (ANFIS), continuous conduction mode (CCM).

1. INTRODUCTION

The power supplies of electronic appliances use low voltage batteries to their components. This demands boosting of DC voltages in higher ratios. Starting from the basic categories of DC-DC converters viz. Buck converter, Boost converter and Buck-Boost converter, the family includes hundreds of converters. All above variations were developed to meet the requirements of specific applications [1]-[3]. The evolutionary classification of DC-DC converters has been done only after 2001 and one such systematic classification (hierarchy chart) clusters them into six generations with their family tree for the history of seven decades. KY boost converter is a newly established by K.I.Hwu and Y. T. Yau [4]-[5]. This converter does not possess any has one right-half-plane zero while operating in continuous conduction mode (CCM) in addition to minimal output voltage ripple (mV level), good dynamic response and a larger voltage conversion ratio. The mandatory requirements of any power conversion systems are minimal components count, less volume, lower weight, economic, waned losses, more steadfastness, subtle switching stresses, broad conversion range, improved supply and load side performances etc. The field driven performance requirements such as the larger voltage gain, huge power density, and decreased ripples in load voltage and inductor current

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imposed converter topologies and screwed the research direction. In the open loop system, the structure and the switching strategies contribute to achieve the objectives. In the closed loop systems the feedback controller has to take the responsibility. The DC-DC converter system is a complex structure, which works in different modes in their operating cycle, where the participating switches and components for every mode are unique. The fundamental working in any mode and the transition between modes are variable structure control in nature. Hence it necessitates an effective robust control approach with a goal of designing a controller and confirming stability in every working stage of the converter viz. initial start-up, dynamic responses (line and load variations), and the effect of component variation etc [6]-[7].

The transient behavior of the boost converter has been demonstrated to an improved level with a designed fuzzy logic controller (FLC) in the MATLAB-Simulink simulation study [8]. An inclusive investigation on performance differences resulted by various feedback controllers (PID-like FLCs0 has presented [9]. The involvement of designed adaptive neuro-fuzzy inference system (ANFIS) controller has been served intelligently in power supply units [10]. A maximum power point tracking (MPPT) system employing the ANFIS suitable for a photovoltaic (PV) fed DC-DC buck/boost converter has been discussed [11]. Through a simple study the merits of the neuro-fuzzy controller in enhancing the performance of the boost converter have been proved, where the duty cycle is directly dictated the controller. The conventional PI controllers (PIC) for such converters developed at the worst case of operating condition (maximum load and minimum line condition present a lower loop band width) makes the system response sluggish. The motive establishing the better performance of neuro-fuzzy controller over the conventional PIC and FLC at various operating points of the boost converter has been successful [12].

The detailed literature survey shows the obligation of an inimitable self-adaptive robust controller for high performance system involving power electronic converters is more and more stringent. FLCs have been lucratively developed and employed in different applications. However, in the real-time applications, abnormality coupled with the available information always occurs. This paper develops an ANFIS controller to enhance the transient performance of positive output KY voltage boosting converter (POKYVBC) based power supply units. The membership functions are fine tuned using neural networks and hence it inherits the property of handling the rule qualms when the operation is enormously unsure and/ or designer cannot faithfully culminate the membership gradients. The proposed ANFIS controller is implemented in MATLBA-Simulink schematics first, then corroborated through field programmable gate array (FPGA) based experimentation.

2. POSITIVE OUTPUT KY VOLTAGE BOOSTING CONVERTER

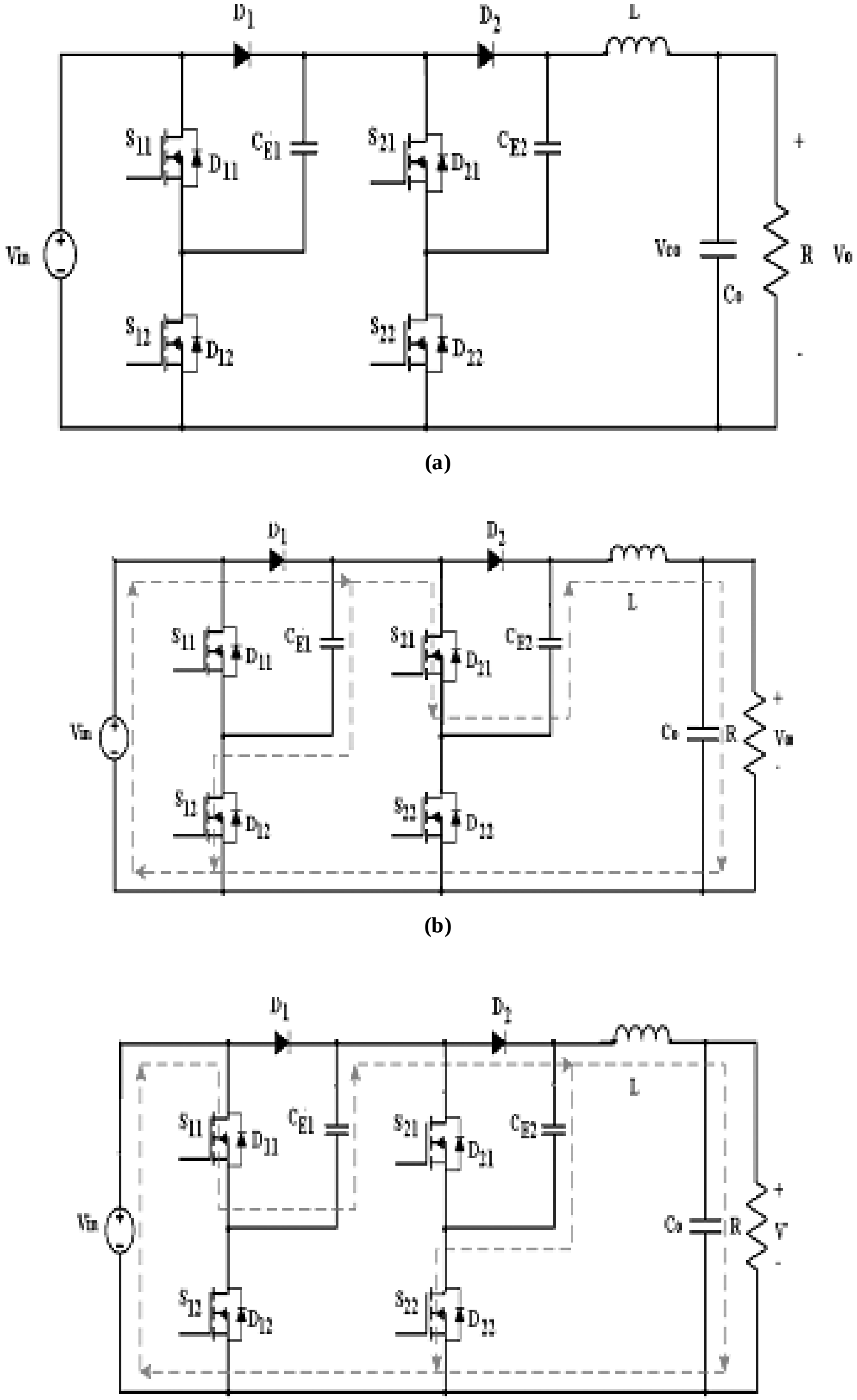
The power circuit of second order-d KY-VBC is depicting in Fig.1 (a). It consists dc input supply voltage V_{in}, four MOSFET power switches S_{11}, S_{12}, $S_{21,}$ and S_{22} along with their corresponding body diodes D_{11}, D_{12}, $D_{21,}$ and D_{22}, energy transferring capacitors C_{E1} and C_{E2}, output inductor L, output capacitor $C_{o,}$ freewheeling diodes D_1 and D_2, output current i_o and load resistance R. The converter is assumed that all the elements are ideal as well as the same converter operates in CCM. Fig.1 (b) and Fig. 1 (c) show the modes of operation of the converter.

During state 1 (refer the Fig. 1(b)), the switches, S_{12} and S_{21} are closed and switches, S_{11} and S_{22} are open, the potential across inductor L is equal to V_{in} (across the C_{E1}) plus $2V_{in}$ (across the C_{E2}) and then subtract $V_{o\text{-}}$ (the output voltage). The current passing through the C_o is equal to $i_L - i_o$. During state 2 (refer the Fig. 1(c)), the switches, S_{12} and S_{21} are open and switches, S_{11} and S_{22} are closed, the potential across the inductor L is equal to $2V_{in}$ (across the C_{E2}) and then subtract the V_o. The current through the C_o is equal to $i_L - i_o$.

The voltage transfer gain of this converter (by applying the voltage balance to states 1 and 2 operation of the converter) is expressed as follows.

$$G = \frac{V_O}{V_{in}} = 2 + d \tag{1}$$

The POKYVBC is designed for 12V input and 28 output and the detailed specification used for the study is catalogued in Table 1.



(a)

(b)

(c)

Figure 1: Power circuit of second order KY-VBC, (a) topology, (b) equivalent circuit-state 1, and (c) equivalent circuit-state 2.

Table 1
Designed POKYVBC

Parameters	*Symbol*	*Value*
Input Voltage	V_{in}	12V
Output Voltage	V_o	28V
Inductor	L	10μH (component change)/20 μH
Capacitors	C_o , $C_{E1,}$ C_{E2}	1000 μF, 680 μF, 100 μF
Switching frequency	f_s	100kHz
Load resistance	R	15ohm
Input Power	P_{in}	56.28W
Output Power	P_o	50.4W
Input Current	I_{in}	4.69A
Output Current	I_o	1.8A
Adopted Value of Duty Ratio	d	0.33

3. ADAPTIVE NEURO-FUZZY INFERENCE SYSTEM (ANFIS) CONTROL

The ANFIS is a type of artificial neural network (ANN), which is based on Takagi–Sugeno fuzzy inference system (FIS). The technique is available since in the early 1990s. As it amalgamates both neural networks and fuzzy logic concepts, it has latent to incarcerate the benefits of both in a single scaffold. Recently, the resurrection of attention in ANNs has infused a new lashing compel into fuzzy domain. The learning capability of ANN is undoubtedly recognized, which can even be leaning to nonlinear parameters into the network architecture. A downside in employing the ANN in control is that it does not have much autonomy in structural accomplishment options. Further, the realization is not at all instinctive and the inner workings of the network are very much imperceptible to the designer. Merging of ANN architectures with FIS has created a influential stratagem known as ANFIS. Some researchers advocate that neural networks and fuzzy control are in fact unique instances of adaptive networks [13]–[16]. Neuro-fuzzy systems such as NEFCON, NEFCLASS and NEFPROX introduced in [17] are some other hybrid neuro-fuzzy adaptive networks based on generic fuzzy perceptron used for control application and classifications [18].

Think about a Sugeno type of fuzzy system having the following rule base

- 1. If x is A_1 and y is B_1, then $f_1 = p_1x + q_1y + r_1$ (2)
- 2. If x is A_2 and y is B_2, then $f_2 = p_2x + q_2y + r_2$ (3)

If the firing strengths of the rules are w_1 *and* $w_{2,}$ respectively$_{,}$ for the particular values of the inputs A_i and integral of B_i, then the output can be computed as weighted average as follows,

$$f = \frac{w_1 f_1 + w_2 f_2}{w_1 + w_2} \tag{4}$$

Let the membership functions of fuzzy sets A_i, B_i, $i = 1, 2$, be μ_{Ai}, μ_{Bi}.

- Layer 1: Each neuron "*i*" in layer 1 is adaptive with a parametric activation function. Its output is the grade of membership function; an example is the generalized bell shape function.

$$\mu(x) = \frac{1}{1 + \left[\frac{x-c}{a}\right]^{2b}} \tag{5}$$

Where [a, b, c] is the parameter set. As the values of the parameters change, the shape of the bell-shape function varies.

- Layer 2: .Every node in layer 2 is a fixed node, whose output is the product of all incoming signals.

$$W_i = \mu_{Ai}(x)\ \mu_{Bi}(y),\ i = 1, 2 \tag{6}$$

- Layer 3: This layer normalizes each input with respect to the others (The *ith* node output is the *ith* input divided the sum of all the other inputs).

$$\bar{w}_i = \frac{w_i}{w_1 + w_2} \tag{7}$$

- Layer 4: This layer's *ith* node output is a linear function of the third layer's *ith* node output and the ANFIS input signals.

$$\bar{w}_i\ f_i = \bar{w}_i (p_i x + q_i y + r_i) \tag{8}$$

- Layer 5: This layer sums all the incoming signals.

$$f = \bar{w}_1\ f_1 + \bar{w}_2\ f \tag{9}$$

4. SIMULATION STUDY

A detailed simulation study is performed for the designed system in MATLAB R2013a/Simulink platform with ode 45 (Dormand-Prince) solver . The performance of the SMC is obtained first then compared with the typical PI controller (PIC). A PIC with settings $Kp = 0.1205$ and $Ti = 0.00016$s (tuned by the Ziegler-Nichols tuning technique) is used. The verification of the complete model performance is made for various working states through start-up transient, line variation, load variation, steady state region and in addition circuit elements modifications. The complete schematics developed in Simulink environment for PIC shown in Fig.2. A two input and one output ANFIS controller is defined.

Then the voltage error and change in voltage error as constructed above is fed as the input of layer 1 in ANFIS structure and the data obtained from the closed loop of PIC are trained using GUI tool box of ANFIS in MATLAB simulation file. The resultant membership functions for the voltage error and change

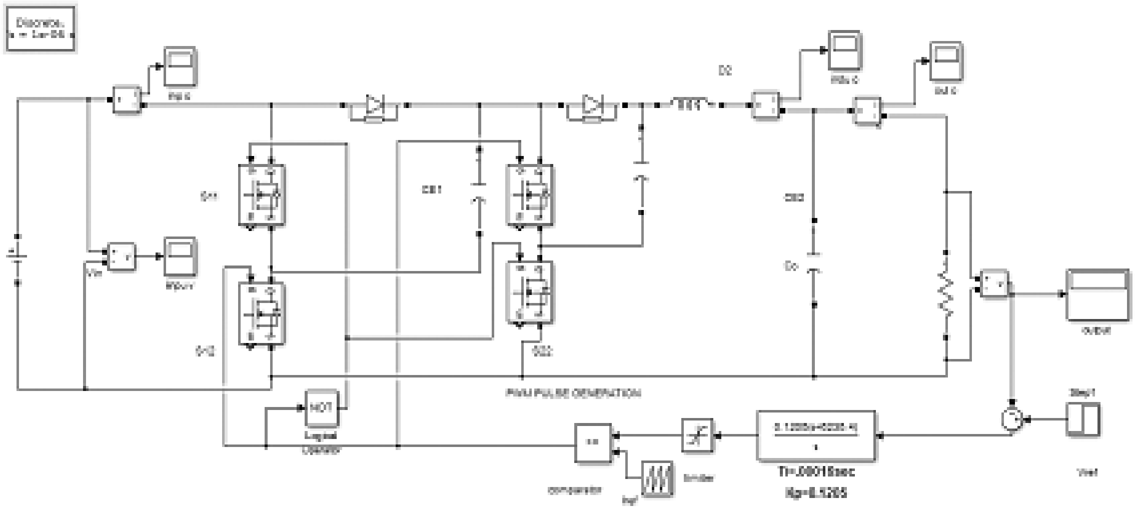


Figure 2: Schematized POKYVBC with PIC

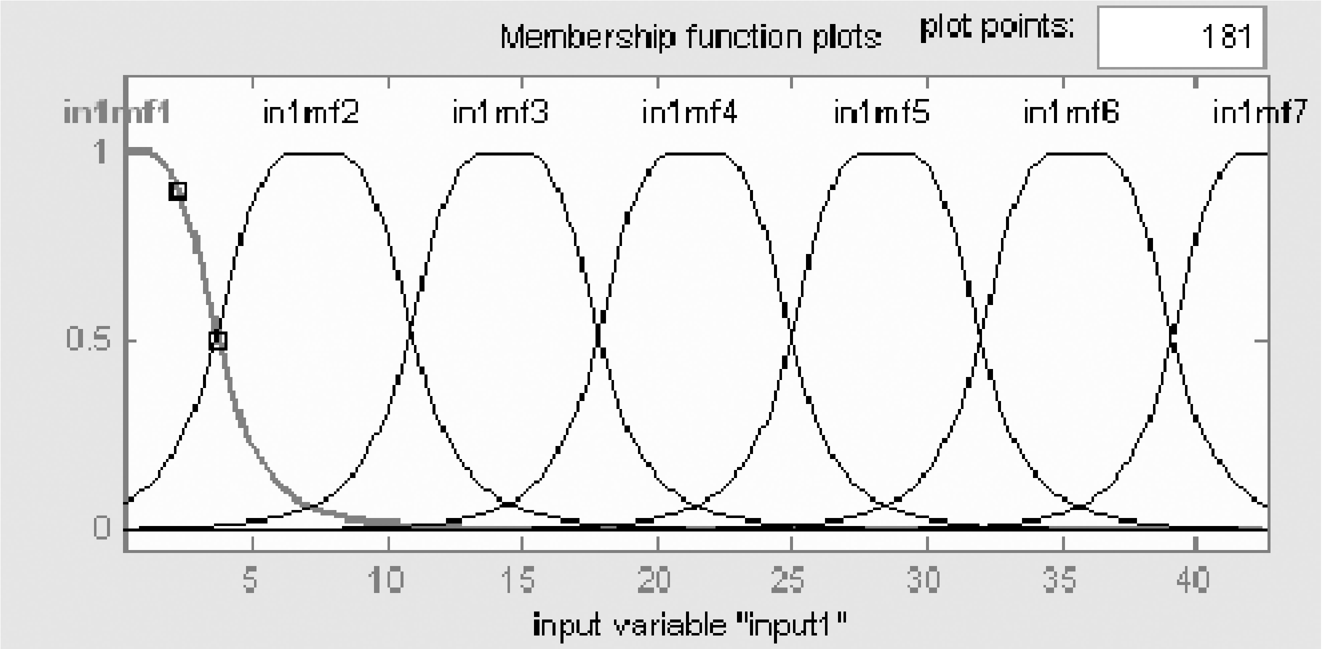


Figure 3: Membership functions of Speed Error after training

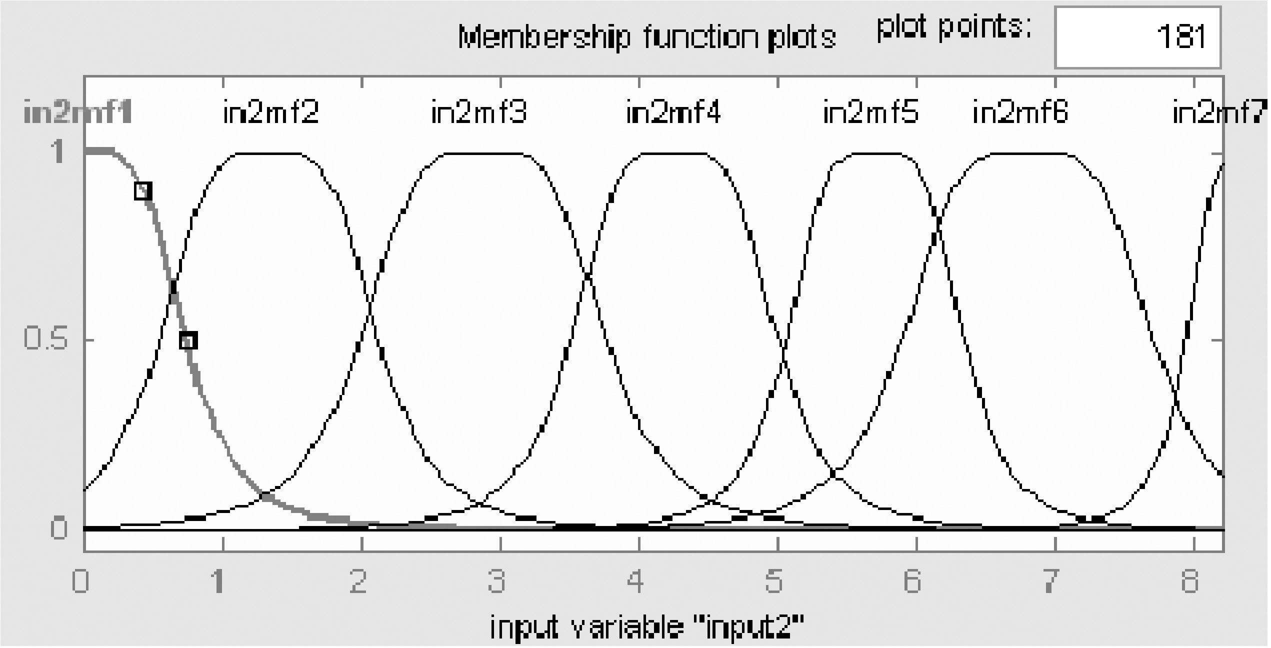


Figure 4: Membership functions of Change in Speed Error after training

in voltage error are as shown in Fig.3 and Fig.4 respectively. The complex ANFIS layer obtained from GUI tool box after training the data as shown in Fig.5.

The triumph properties of the neural network vzi. ability to classify data and find patterns are used ANFIS. From this, it develops a fuzzy expert system that is more translucent to the user and also less likely to produce memorization error than a neural network. ANFIS maintains the advantages of a fuzzy expert system, while eradicating (or at least reducing) the requirement for an expert. The problem with ANFIS design is that large amounts of training data require developing an accurate system.

Fig.6 represents the start up transients caused by both PIC and ANFIS controller for input of 12V. It is well evidenced that developed ANFIS controller provides better results than PIC. Response to step change

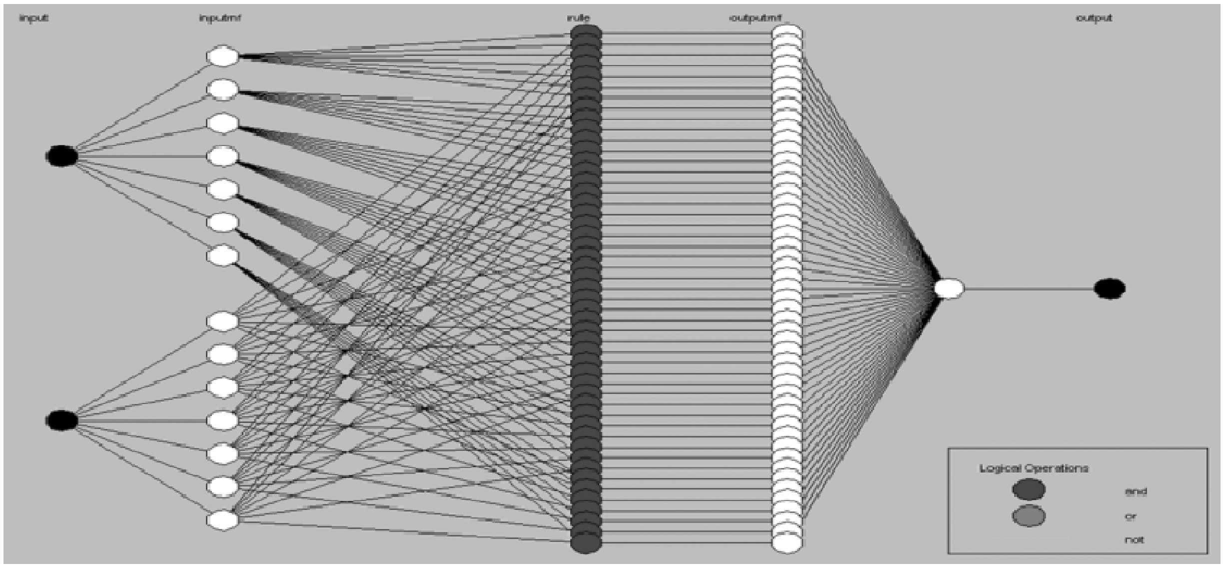


Figure 5: ANFIS Layer Obtained

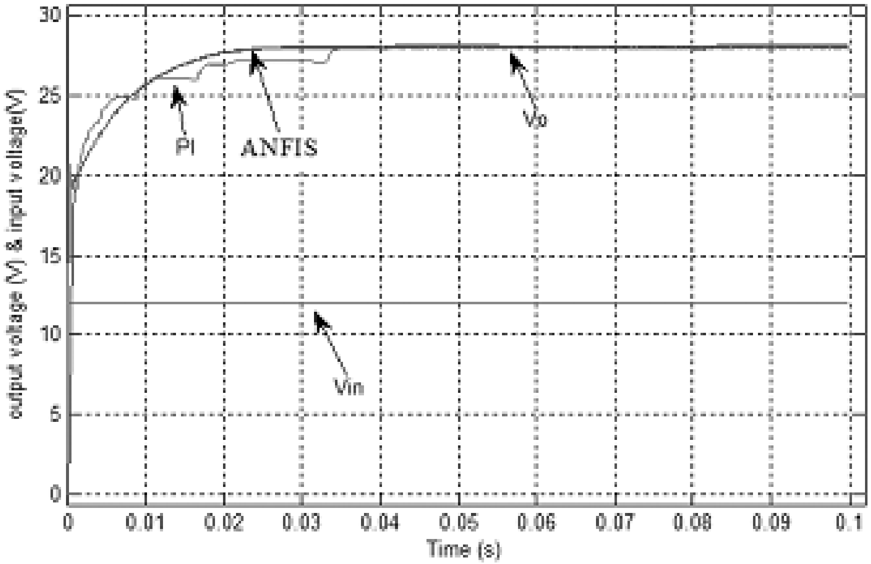
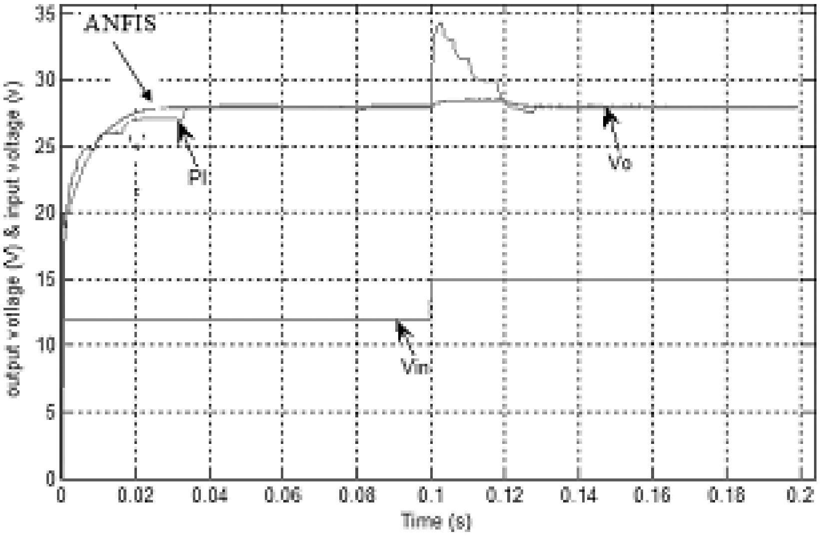
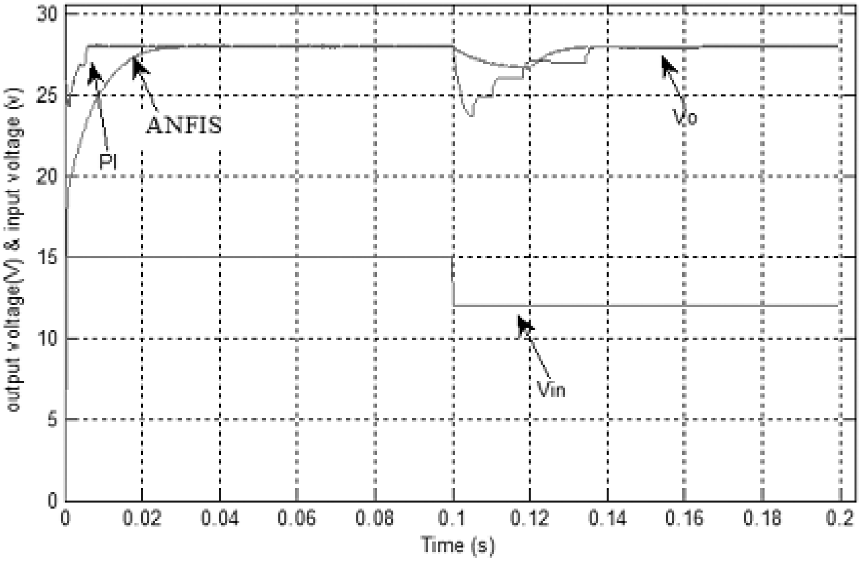


Figure 6: Start up transients in PIC and ANFIS



(a) for input step change from 12V to 15 V



(b) for input step change from 15V to 12 V.

Figure 7: The output voltage with rated load

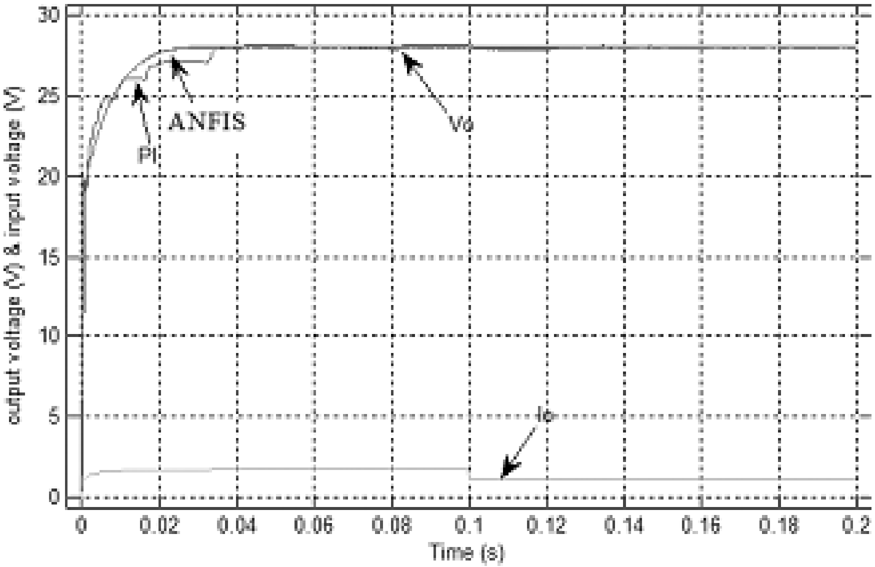


Figure 8: Response to step load change from 15.6&! to 20 &! at 0.05s

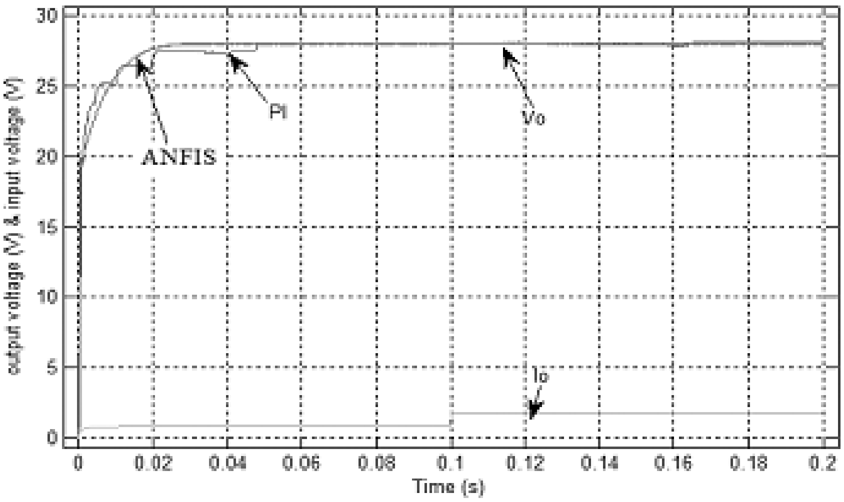


Figure 9: Response to step load change from 15.6Ù to 10Ù at time 0.1s with Vin= 12V.

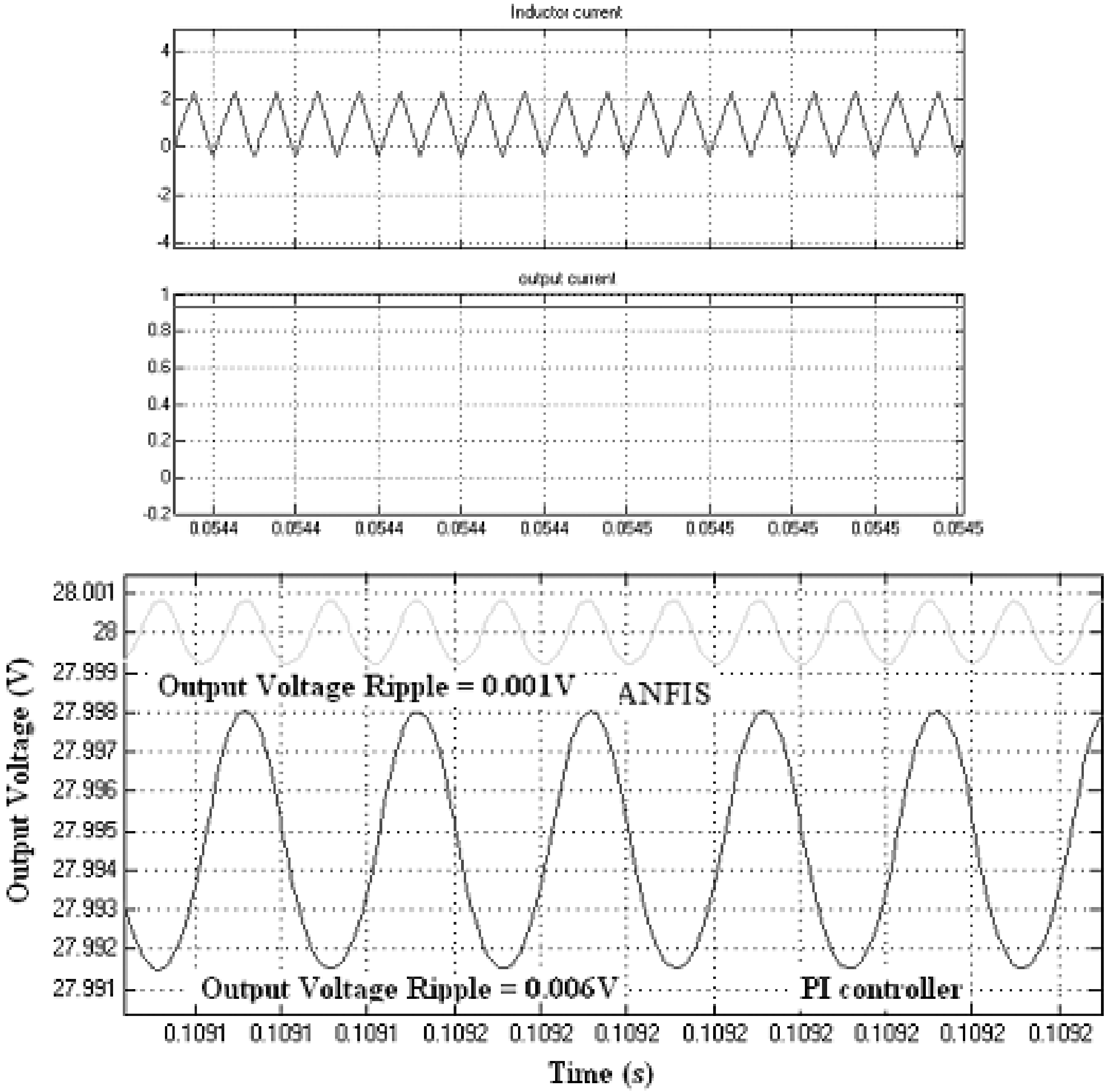


Figure 10: Response of output voltage and inductor current in steady state condition using both controllers

in input from 12V to 18V and 15V to 12V are respectively shown in Fig.7 (a) and (b). The transient response to step load change from 15.6&! to 20 &! at 0.05 ms, is presented in Fig.8 while Fig.9 depicts the response during load step change from 20&! to15.6&! at 0.05 sec.

The component variation and corresponding controller performance is studied in Fig.11 and Fig.12. Table 2 tabulates time domain specifications (TDSs) of different perturbations.

Table 2
TDS in PIC and ANFIS controller

	Start up-Region		Line variations				Load Variations			
			Vin=12Vto 15V		Vin=15Vto 12V		R=15.6 Ω to 20 Ω		R=15.6 Ω to 10 Ω	
	Mp	**Ts**	Mp	**Ts**	Mp	**Ts**	Mp	**Ts**	Mp	**Ts**
ANFIS	-	0.025	2.3V	0.0112	1.22V	0.005	-	-	0.05V	0.0012
PI	-	0.04	7V	0.022	4V	0.04	-	-	0.5V	0.028

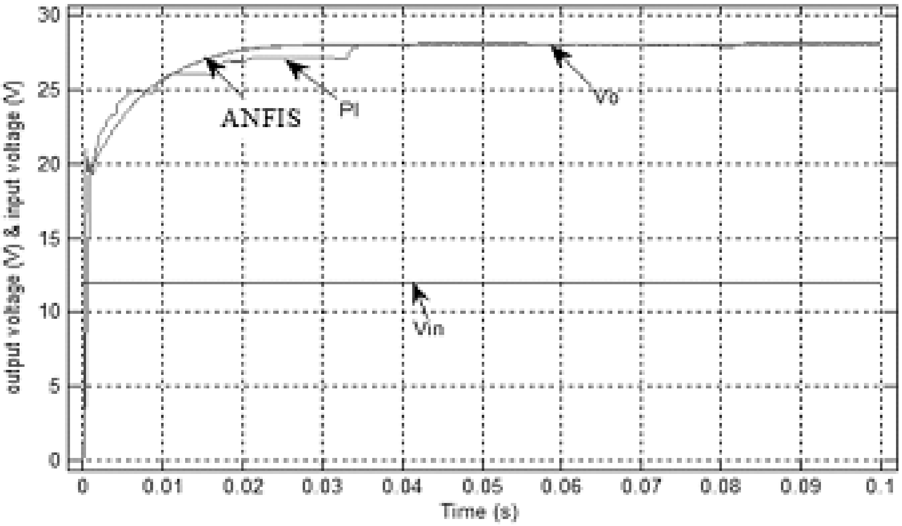


Figure 11: Output voltage using ANFIS and PIC when inductor variation from 10ìH to 15ìH.

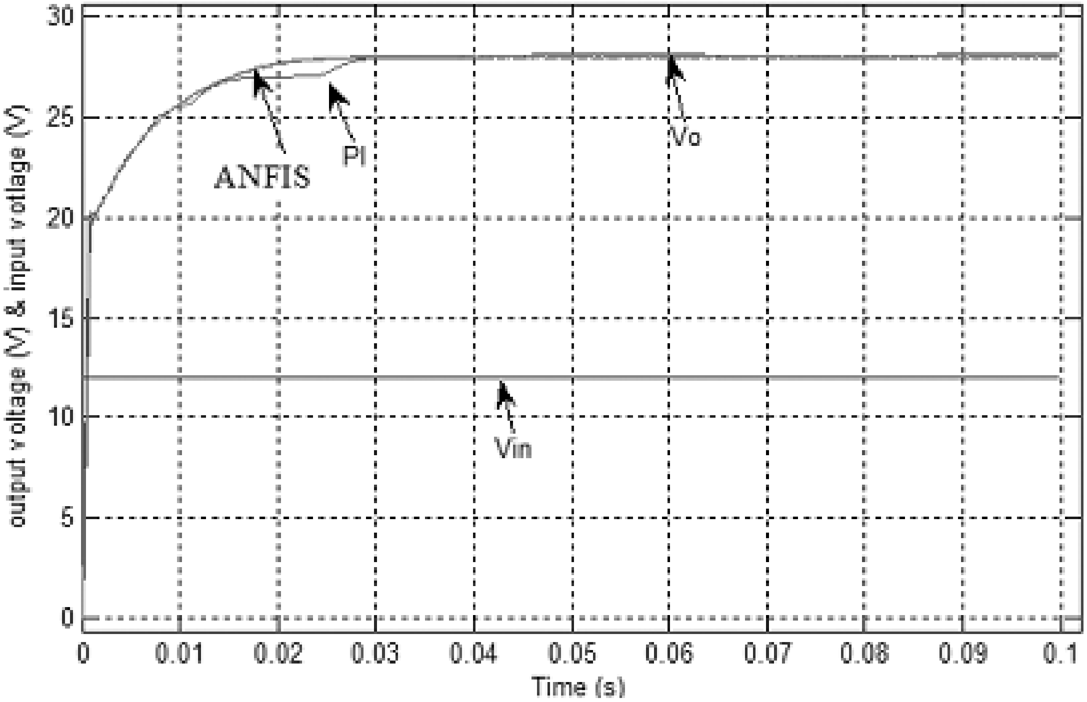


Figure 12: The output voltage when capacitance varied from 1000ìF to 1500ìF.

4. EXPERIMENTAL STUDY

The simulation results are verified in an experimental investigation. A proto type POKYVBC is developed for the specification given in Tale 1. MOSFET IRFN 540 is taken as power switch, the D_{1}-D_{2} are FR306, Capacitors C_O, C_{E1} and C_{E2} are respectively with 1000μF, 680μF and 100μF and 100V, Electrolytic and plain polyester type, and the inductor is 20μH (variable)/5A (Ferrite Core). The complete experimental setup is detailed in Fig.13.

The proposed ANFIS controller is implemented using the very high speed integrated circuit (VHSIC) hardware description language (VHDL). The functional simulation study of the architecture is done using the tool Modelsim 6.3. The Register Transfer Level (RTL) substantiation and implementation are performed using the synthesize tool Xilinx ISE 13.2. Then the designed architecture has been configured to the SPARTAN-6 FPGA (XC6SLX45) device. The functionality of each block in the architecture is simulated

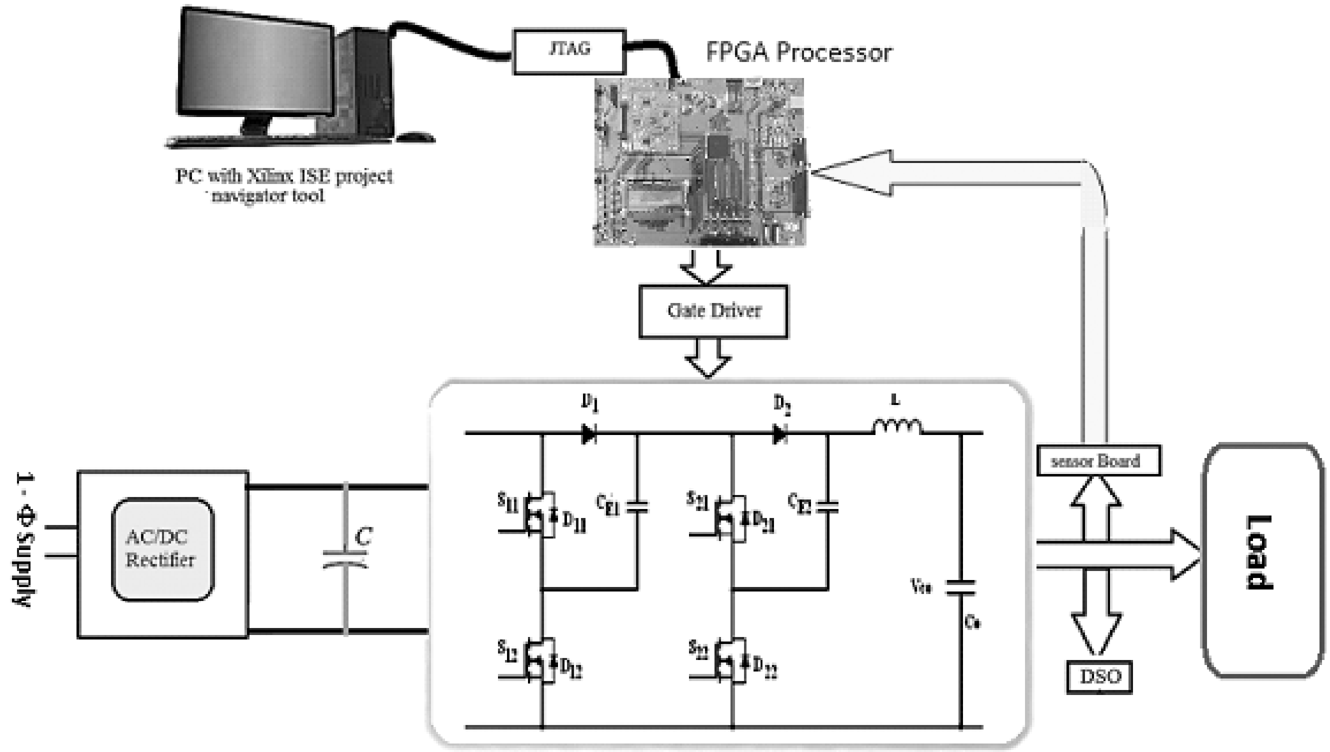


Figure 13: Experimental setup

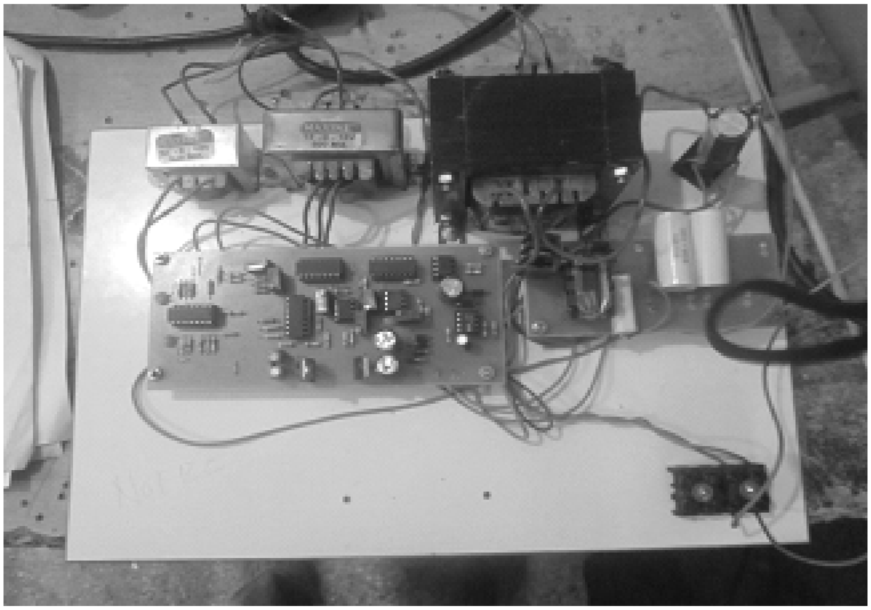


Figure 14: Photograph of POKYVBC using FLC

thoroughly using the Modelsim software. The detailed flow is represented in the Fig.15 as a flow chart. The simulated VHDL design architecture is synthesized using Xilinx ISE software. The RTL verification and logic implementation of the design are carried out here. The corresponding synthesis results are shown in Fig.16 and Fig.17. Representative load regulation response is pictured in Fig.18.

5. CONCLUSION

An intelligent non-linear controller, adaptive network-based fuzzy inference system (ANFIS), is developed to enhance the dynamic behavior of the Positive Output KY Voltage Boosting Converter (POKYVBC).

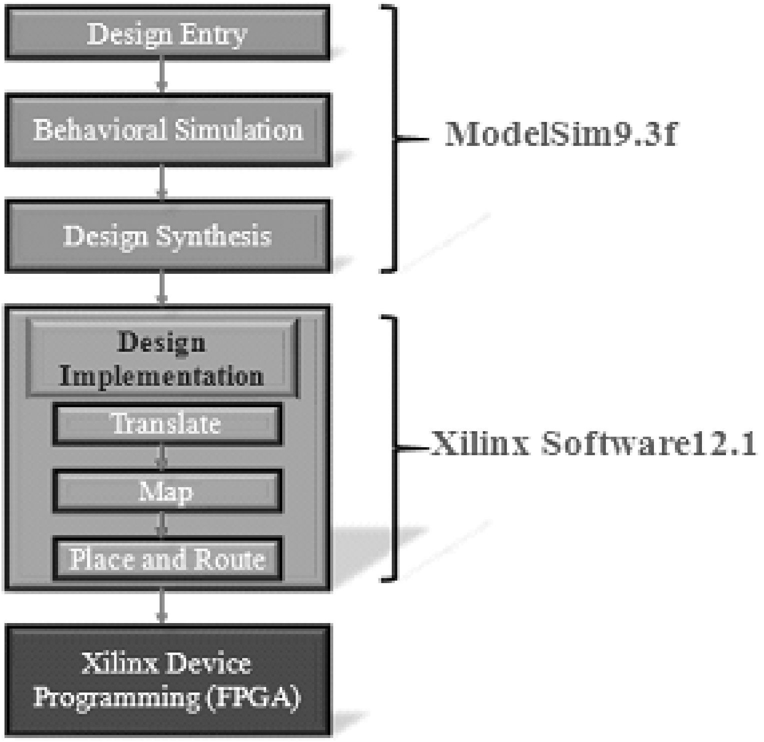


Figure 15: FPGA Design flow

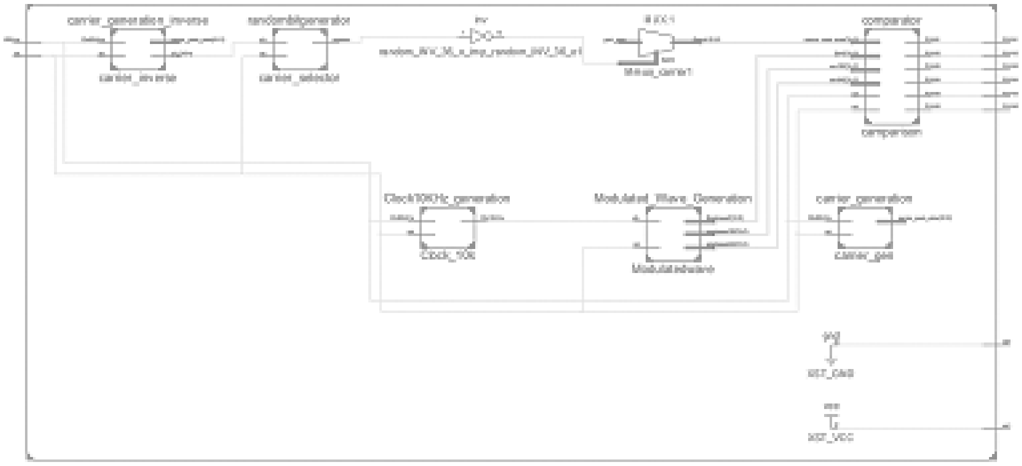


Figure 16: RTL Diagram for RPWM 8-bit PRBS

Device Utilization Summary (estimated values) [-]

Logic Utilization	*Used*	*Available*	*Utilization*
Number of Slice Registers	325	30064	1%
Number of Slice LUTs	793	15032	5%
Number of fully used LUT-FF pairs	228	890	25%
Number of bonded IOBs	10	186	5%
Number of BUFG/BUFGCTRLs	5	16	31%
Number of DSP48A1s	3	38	7%

Figure 17: Device utilization summary

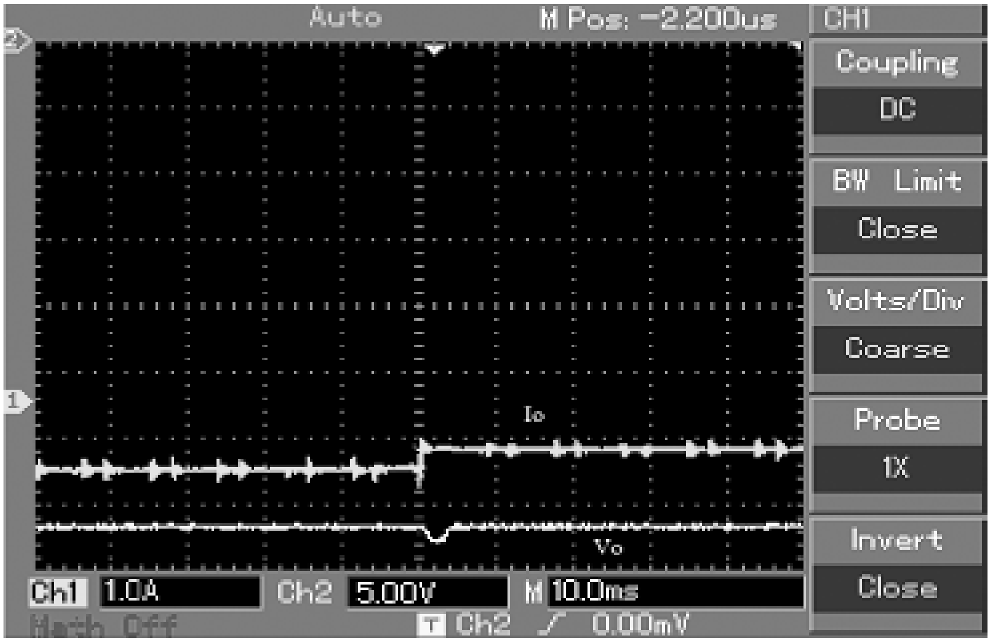


Figure 18: Representative output voltage response of ANFIS for load regulation

The dynamic performances during start-up over shoot, line and load perturbations and component variations are investigated in detail. The developed system is simulated in MATLAB-Simulink environment and later verified in an laboratory proto-type supported by SPARTAN-6 FPGA (XC6SLX45) device. The results shows that all the time domain specifications are improved with ANFIS controller for all kind of perturbations.

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