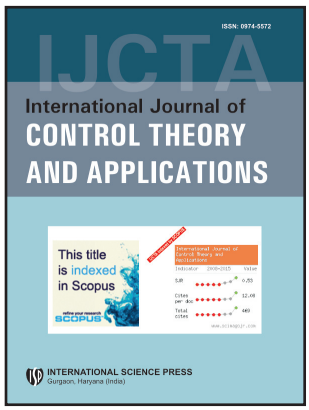

International Journal of Control Theory and Applications

ISSN : 0974-5572

Volume 9 • Number 44 • 2016

Design and FPGA Performance Analysis of 2D and 3D Router in Mesh NoC

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Abstract: Network on Chip (NoC) architecture is the efficient and flexible infrastructure for multiprocessor System on Chip (MPSoC). NoC has been recognized most viable communication infrastructure, fast and scalable structures. Router plays the important role for inter-chip communication in the NoC. The research article presents the design and FPGA implementation of 2D and 3D NoC router and its application to mesh network. The cluster size of the configured mesh NoC is 2D (3×3) and 3D ($3 \times 3 \times 3$). The 2D router follow 5×5 crossbar switch and 3D NoC (7×7) crossbar switch. The XY and XYZ routing is used to address the routers in 2D and 3D mesh NoC. The design is developed in Xilinx ISE 14.2 with the help of VHDL programming and synthesis is carried on Virtex-5 FPGA. The inter communication among the nodes is verified on the same FPGA. The hardware and timing performance parameters of the 2D and 3D NoC routers are compared.

Keywords: Network on Chip (NoC), Multiprocessor System on Chip (MPSoC), NoC Router.

1. INTRODUCTION

The design and development of integrated system technology is increasing the on chip transistors very rapidly and the performance of the whole system depends on interconnections. Network on chip (NoC) [1, 2] is the method on chip communication that provides the scalable architecture, low latency, and high throughput. NoC is the on chip network solution in which multiple processors can communication in a specific network structure. The technology scaling permits to increase the system on chip (SoC) [3, 4] complexity in terms of components counts. The multiple processors system on chip (MPSoC) [1, 9] has the challenges in the management of resources, interconnects and power requirements in the complete chip integration. The computing resources in SoC are increasing enormously because VLSI technology supports the integration of transistors in single chip

and enhances computations logic and applications but the system requirements of high performance is also mandatory to meet. The SoC system followed shared bus connections and arbitration is requited to address the serial requests from other integrated processing elements. It makes system slower, limited and less scalable [5, 6], due to one master is following all the requests and utilizing the same bus several times. Moreover, the multiple requests need larger bandwidth for the interconnections. The conventional bus based system is not good to support latest MPSoC, due to high latency, low throughput, larger power dissipation, scalability issues and parallelism integration.

NoC is the promising solution to overcome all these issues for system integration. NoC provides scalable and reconfigurable structure in which custom designs, memories, processor and controllers can be integrated in a single chip. The data is transferred on hop by hop with the help of packet switching technique. The complexity of the system is increasing day by day and future of chip integration demands optimized architecture, so that large bandwidth [7] can exist to communicate among the processing elements of the NoC. It is very important to design the fast routers and configure the new topological architecture to archive these goals. The concept of NoC is derived from distributed networks and large scale multiprocessors. The scalable bandwidth requirements are fulfilled by NoC, supports on chip interconnects for micro network [6, 7] with packet switched data transfer. The current research on NoC is based on their topology, routing algorithms, switching techniques to provide efficient on chip communication. Topology [8] is the method to connect the communicating nodes, so that the structure will provide optimized time and larger bandwidth. The NoC supports serval topology such as mesh, star, torus, ring, butterfly and several mixed custom topology. Many researchers have analyzed that application specific topology provides the good performance in terms of power consumption and minimal space. The NoC architecture [13] consists of several interconnecting wires and routers. The Network interface (NI) [10] functions to transfer the data packets in processor cores with fixed length under flow control called flits. The flits have the information of tail flit, header flit [11, 12] and existing body of flits. The data packet is transferred from the source node to destination node in hop by hop manner.

2. NOC ROUTER

Router is the main part of the communication network to forward the data packets and provides direction among the communicating entities. In the communication system the data packet is routed from one communication network to the, which constitute the internetwork until the data packet is transferred to the destination node. The router consists of the multiple lines or segment of wires. There exist one processing elements corresponds to one router. The data packet consists of the information of the source and destination network. The router reads the address of the destination and route in the particular direction. The NoC router processes the fixed length data through the processing elements. The NoC router can be configured as 2D and 3D, based on its directional data transfer. The XY routing [11] is followed in 2D and XYZ routing is followed in 3d NoC. The 2D NoC router can process the data in 5 directions or via 5 input/output ports. In the same way the 3D router [6, 12] processes the data with the help of 7 input/output ports. The Figure 1 shows the 3D NoC router that can process the data. The data input packet is controlled through control logic in different possible directions, east_input_port, west_input_port, north_input_port, south_input_port, local_input_port, up_input_port and down_ input_port. The data is stored into directional registers by its corresponding port as east_output_port, west_output_port, north_output_port, south_output_port, local_output_port, up_output_port and down_ output_port. In 2D NoC Router, the 5×5 crossbar switch exists to address the data. In 3D NoC router 7×7 crossbar switches exist to address the input and output. The 2D and 3D NoC crossbar switch are depicted in Figure 2 and Figure 3 respectively.

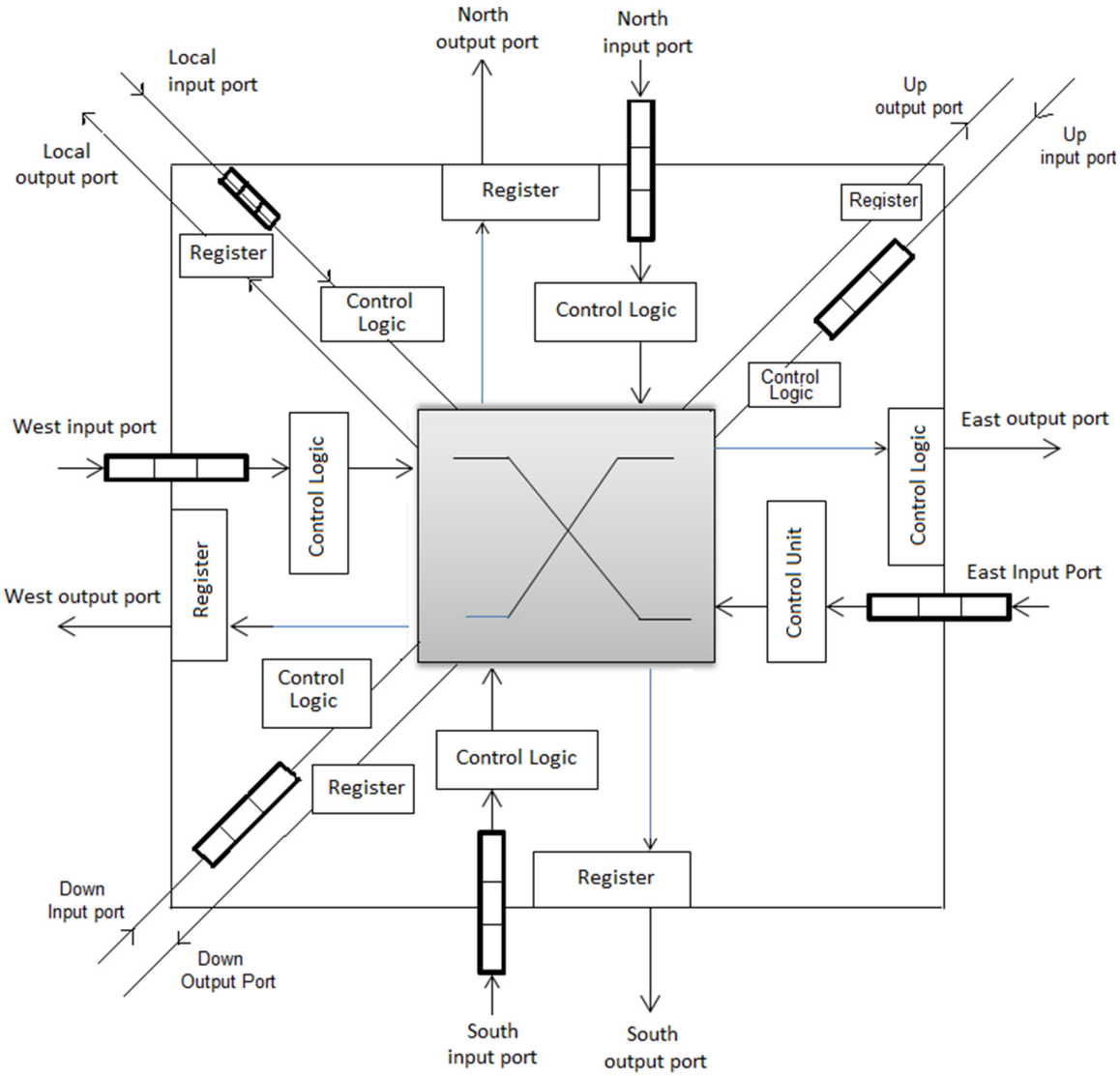


Figure 1: 3D NoC Router

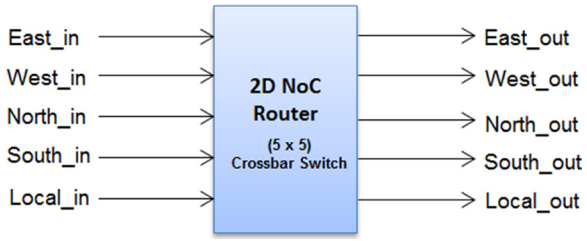


Figure 2: NoC Router input/output ports 2D

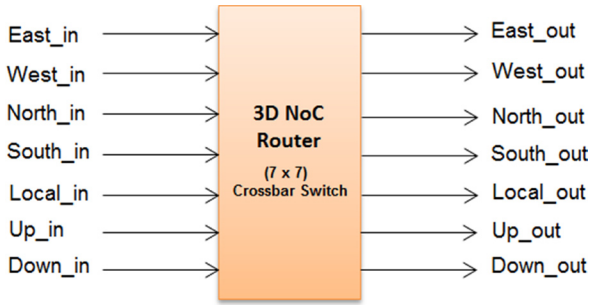


Figure 3: NoC Router input/output ports 3D

System design

The performance of the NoC router can be understood in the application to the NoC topology architectures. The NoC architecture can follow mesh, ring, torus, tree or hybrid topology based on the applications and requirements.

The researchers have proved the mesh topology is the best topology in terms of performance, scalability and consistent shape. The Figure 4 shows the 3 × 3 mesh topology structure in which 9 router have configured to communicate in cases of full available and full utilized network. The XY routing is followed in which node is addressed as X direction first and then Y direction. The 9 router are configured as R0 (000 000), R1 (001 000), R2 (010 000), R3 (000 001), R4 (001 001), R5 (010 001), R6 (000 010), R7 (001 010) and R8 (010 010). The router addressing scheme is also discussed in Table 1. The 3D NoC router with mesh topology (3 × 3 × 3) is shown in Figure 5, in which 27 routers can communicate. The addressing is followed by XYZ routing. The routing can be understood with the help of Table 2.

Table 1
XY routing for 2D mesh (3 x 3) NoC

X_address	*Y_address*	*XY Routing*	*Router Selection*
000	000	(00)	R0, Router
001	000	(10)	R1, Router
010	000	(20)	R2, Router
000	001	(01)	R3, Router
001	001	(11)	R4, Router
010	001	(21)	R5, Router
000	010	(02)	R6, Router
001	010	(12)	R7, Router
010	010	(22)	R8, Router

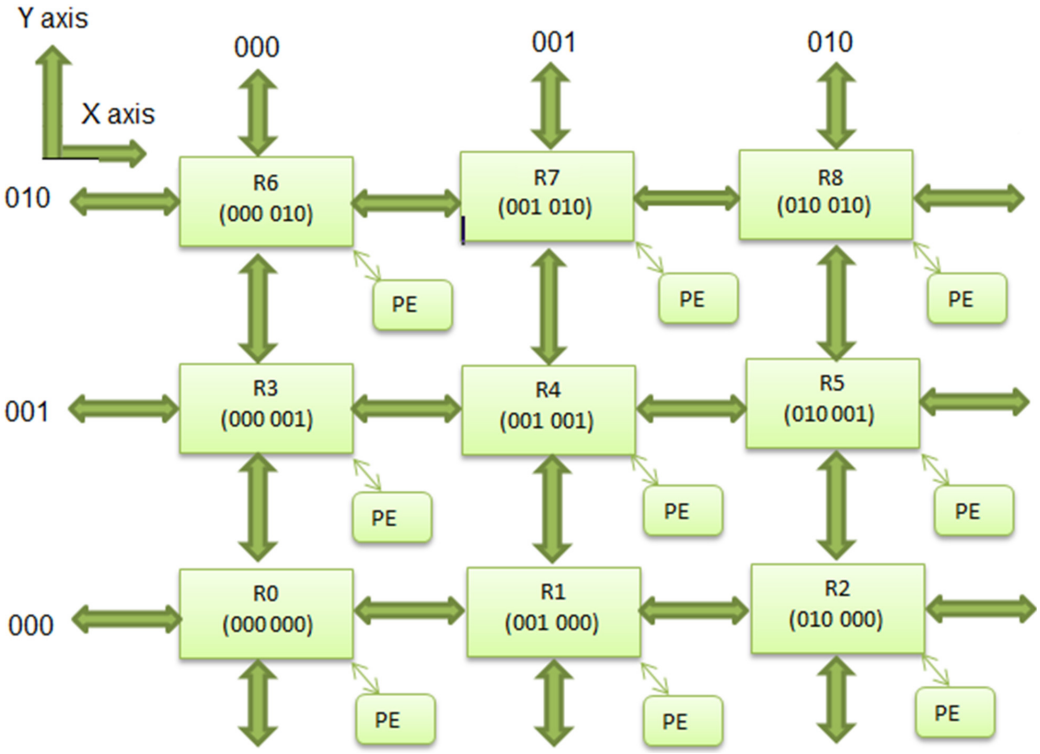


Figure 4: Mesh 2D NoC Design (3 x 3)

Table 2
XYZ routing for 3D mesh (3 × 3 × 3) NoC

X	*Y*	*Z*	*XYZ Routing*	*Router Selection*
000	000	000	(000)	R0, Router
001	000	000	(100)	R1, Router
010	000	000	(200)	R2, Router
000	001	000	(010)	R3, Router
001	001	000	(110)	R4, Router
010	001	000	(210)	R5, Router
000	010	000	(020)	R6, Router
001	010	000	(120)	R7, Router
010	010	000	(220)	R8, Router
000	000	001	(001)	R9, Router
001	000	001	(101)	R10, Router
010	000	001	(201)	R11, Router
000	001	001	(011)	R12, Router
001	001	001	(111)	R13, Router
010	001	001	(211)	R14, Router
000	010	001	(021)	R15, Router
001	010	001	(121)	R16, Router
010	010	001	(221)	R17, Router
000	000	010	(002)	R18, Router
001	000	010	(102)	R19, Router
010	000	010	(202)	R20, Router
000	001	010	(012)	R21, Router
001	001	010	(112)	R22, Router
010	001	010	(212)	R23, Router
000	010	010	(022)	R24, Router
001	010	010	(122)	R25, Router
010	010	010	(222)	R26, Router

The data packet flit is considered of 150 bit from one hop to another and its frame format is shown in Figure 6.

End bit (1 bit): The end bit indicates the status of end of transmission from the source to destination

Layer Identification (3 bit): In case of multiple layers of 2D or 3D NoC router the address indicates the address of specific layer.

Source Router Sxyz (3, 3, and 3): It is the 9 bit address indicates the source router address in X (3 bit), Y(3 bit) and Z (3 bit) direction.

***Destination Router Dxyz (3, 3, 3) (9 bit)*:** It is the 9 bit address indicates the destination router address in X(3 bit), Y(3 bit) and Z (3 bit) direction.

Data (n bit): the data communication is possible of 'n' bit. In the case it is considered as 128 bit data among source and destination routers.

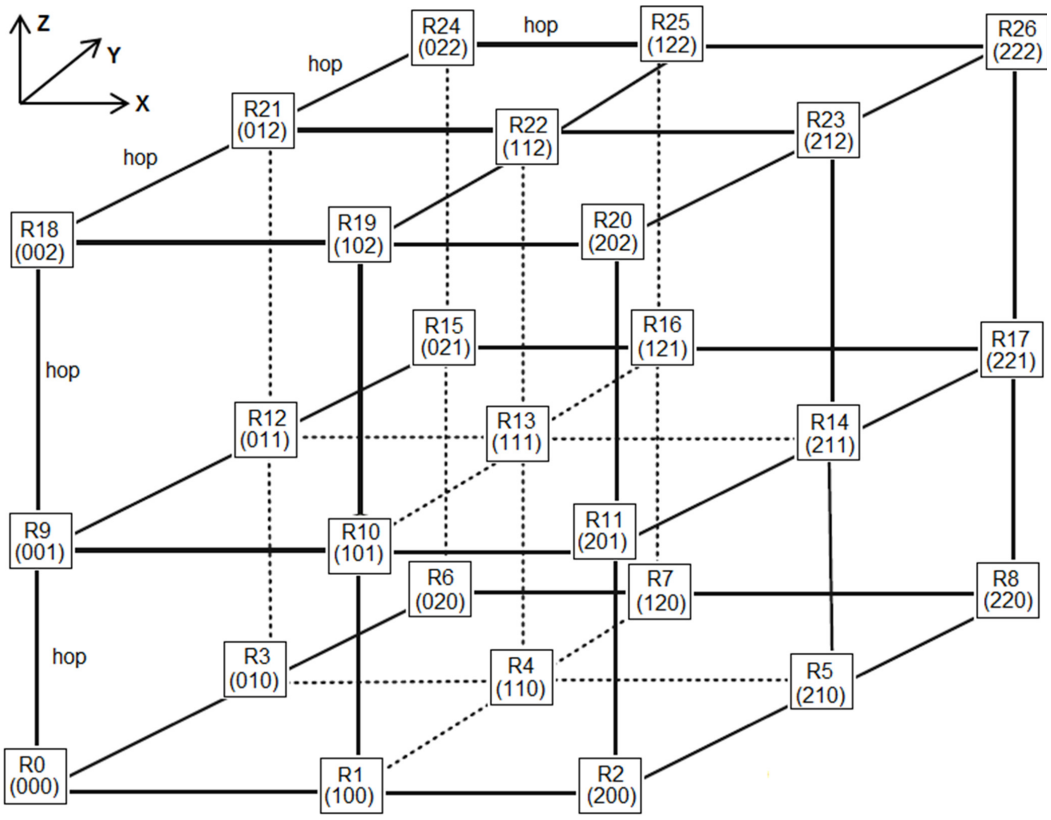


Figure 5: Mesh 3D NoC Design (3 x 3 x 3)

End bit	*Layer Identification*	*Source Router Sxyz (3, 3, 3)*	*Destination Router Dxyz (3, 3, 3)*	*Data (n bit)*
149	148-146	145 137	136 128	127 0
(1 bit)	(3 bit)	(9 bit)	(9 bit)	(128 bit)

Figure 6: Data packet format

3. RESULTS & DISCUSSIONS

The 2D and 3D NoC router is developed in Xilinx ISE 14.2. The RTL View of 3D mesh NoC is shown in Figure 7. The RTL view presents the input and output pin of the developed NoC. The hardware synthesis results are carried targeting virtx-5 FPGA on xc5vlx20t-2-ff323. The RTL consist of details of the pins of developed chip. The *clk* is the default signal and *reset* is used to reset all the contents of node. *Layer_address [3:0]* is the address of nodes layers, *source_XYZ[8:0]* source node address, *destination_XYZ[8:0]* destination node address. Write and read are the control signal for nodes memory. The input and output data corresponding to source and destination node is *packet_data[127:0]* and *packet_out[127:0* respectively. The status of the node status is FIFO_full and FIFO_empty when the nodes are busy and free to communicate. Figure 8 (a) & (b) depicts the functional simulation waveform in modelsim with 4 test cases. The hardware synthesis results and timing values are listed in table 3 and table 4 respectively. The comparative value of timing parameters is also shown by Figure 9.

Test Case-1: Value of reset = '1', then run, Force reset = '1', apply direct clk signal, value of layer_identification = "000", source_xyz = 102, destination_xyz = 222, write = '1' , read= '0' and input_packet_data = "11111110 00000001111111000000001111111100000000111111110000000011111111000000001111111 10000000011111110000000" or "FF00 FF00 FF00 FF00 FF00 FF00 FF00 FF00 (hex)". Then Force write '0' and read = '1' the data is displayed on destination node as packet_data, empty_fifo = '1' and full_fifo = '0'.

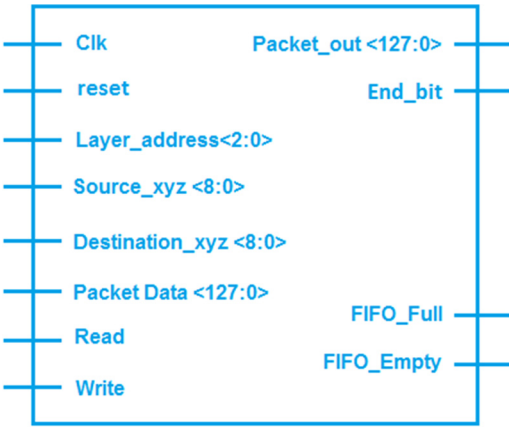
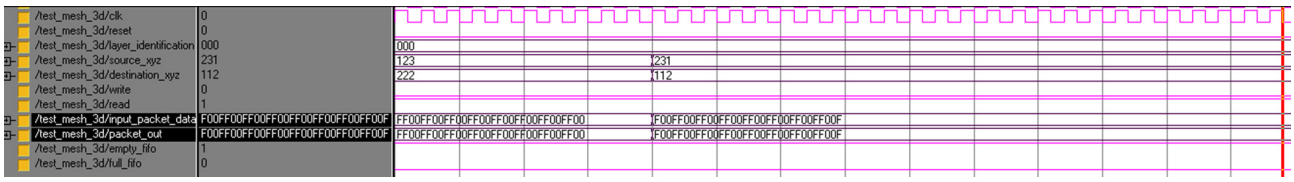
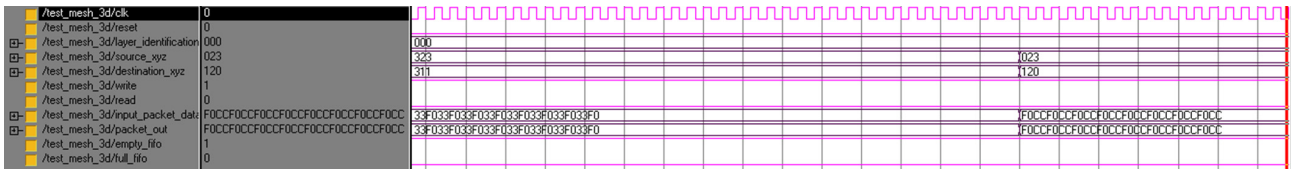


Figure 7: RTL schematic of 3D mesh NoC



(a)



(b)

Figure 8: Simulation result for 128 bit data transfer

Test Case-2: Value of reset = '1', then run, Force reset = '1', apply direct clk signal, value of layer_identification = "000", source_xyz = 231, destination_xyz = 112, write = '1' , read= '0' and input_packet_data = "11100000 00011111110000000011111110000000011111110000000011111110000000011111110000 00000111111100000000 1111" or "F00F F00F F00F F00F F00F F00F F00F F00F (hex)". Then Force write '0' and read = '1' the data is displayed on destination node as packet_data, empty_fifo = '1' and full_fifo = '0'.

Test Case-3: Value of reset = '1', then run, Force reset = '1', apply direct clk signal, value of layer_identification = "000", source_xyz = 323, destination_xyz = 311, write = '1' , read= '0' and input_packet_data = "00110011 11110000001100111111000000110011111100000011001111110000001100111111000000 00110011111100000011001111110000" or "33F0 33F0 33F0 33F0 33F0 33F0 33F0 33F0 (hex)". Then Force write '0' and read = '1' the data is displayed on destination node as packet_data, empty_fifo = '1' and full_fifo = '0'.

Test Case-4: Value of reset = '1', then run, Force reset = '1', apply direct clk signal, value of layer_identification = "000", source_xyz = 023, destination_xyz = 120, write = '1' , read= '0' and input_packet_data = "11110000 11001100111100001100110011110000110011001111000011001100111100001100110011 11110000110011001111000011001100" or "F0CC F0CC F0CC F0CC F0CC F0CC F0CC F0CC" (hex). Then Force write '0' and read = '1' the data is displayed on destination node as packet_data, empty_fifo = '1' and full_fifo = '0'.

Table 3
Device utilization summary

Parameter	*Utilization*	
	(3 × 3) 2D NoC	*(3 × 3 × 3) 3D NoC*
Use of Slices	190 out of 12480, 1.52%	284 out of 12480, 2.27%
Use of Flip Flops, Slices	230 out of 12480, 1.84 %	324 out of 12480, 2.6 %
Use of Number of LUTs (4 input)	56 out of 330, 16.96%	85 out of 330, 25.75%
Use of bonded IOBs	30 out of 172 12.20 %	30 out of 172 17.64 %
Use of GCLKs	1 out of 32 3.0 %	1 out of 32 3.0 %

Table 4
Timing parameters values

Parameter	*Value*	
	2D Mesh NoC (3 × 3)	*3D Mesh NoC (3 × 3 × 3)*
Value of Minimum Period	0.998 ns	1.418 ns
Frequency Value Maximum	235 MHz	400 MHz
Input arrival time (Minimum) before clock	1.145 ns	1.526 ns
Output time required (maximum) after clock	1.967 ns	2.101 ns
Total Memory usage	885432 kB	112562 kB

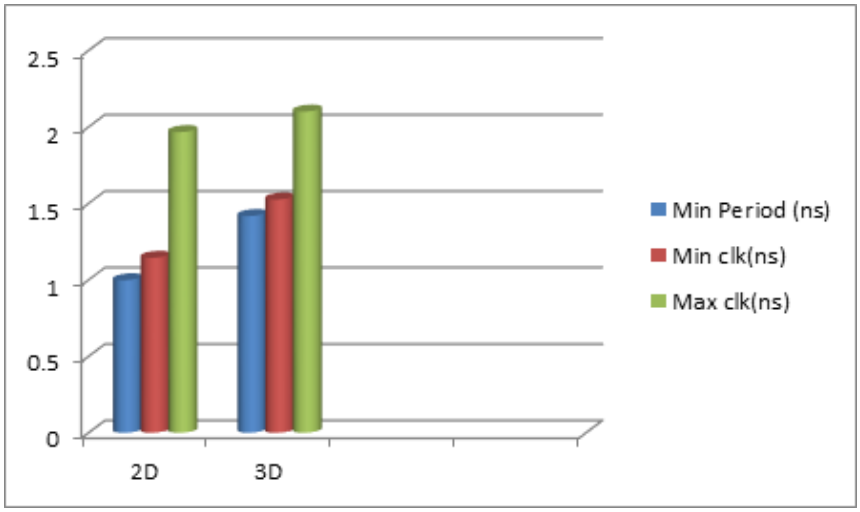


Figure 9: Timing values for 2D and 3D mesh NoC

4. CONCLUSIONS

The design of 2D and 3D NoC router is done successfully with the help of VHDL programming. The routers are used to configure the mesh NoC 2D (3 × 3) and 3D (3 × 3 × 3) and data communication is verified on Virtex-5 FPGA. The hardware parameters of 2D and 3D mesh NoC extracted directly by the synthesis report generated by the Xilinx ISE software and compared. The comparison result shows that 3D NoC utilizes more hardware and timing in comparison to 2D NoC. Such scalable and modular approach is helpful in the implementation of larger scale networks. In future, the further work can be directed in the secured data transfer and adding the feature of network security with encryption and description.

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